High Efficiency 3-Channel LED Backlight Driver

Features

- Wide input range: 2.7V~5.5V
- High efficiency step-up 3-Channel LED driver
- 3-Ch current sinks, up to 8-LEDs per string
  - Up to 29.8mA/Ch
  - +/-0.6% current matching at 20.2mA
  - +/-1.5% current accuracy at 20.2mA
- I²C/PWM dual dimming control scheme
  - 11-bit I²C exponential or linear mapping with programmable transition ramp time
  - Wide range PWM dimming with programable transition ramp time
    - 100Hz to 100kHz frequency
    - 0.2% to 100% duty cycle at 20kHz
- Programmable current sink turn on/off ramp time and shape
- Selectable boost converter switching frequency 1MHz or 500kHz with 20% shift up option
- Programmable input PWM hysteresis to minimize jitter at low PWM duty cycle
- Programmable OVP (25.9V/32V) and current limit (2.6A/1.8A)
- LED open/short protection
- Status reporting through I²C interface

Applications

- Smartphone/Tablet Backlight

Brief Description

KTD3136 is the ideal power solution for LED backlighting in medium to large size LCD panels. It is a highly integrated step-up DC-DC converter operating with an input voltage from 2.7V to 5.5V, accommodating 1-cell lithium ion batteries or 5V supply. It includes a high voltage power NMOS, as well as three current sinks, resulting in a simpler and smaller solution with fewer external components. High switching frequency allows the use of a smaller inductor and capacitor.

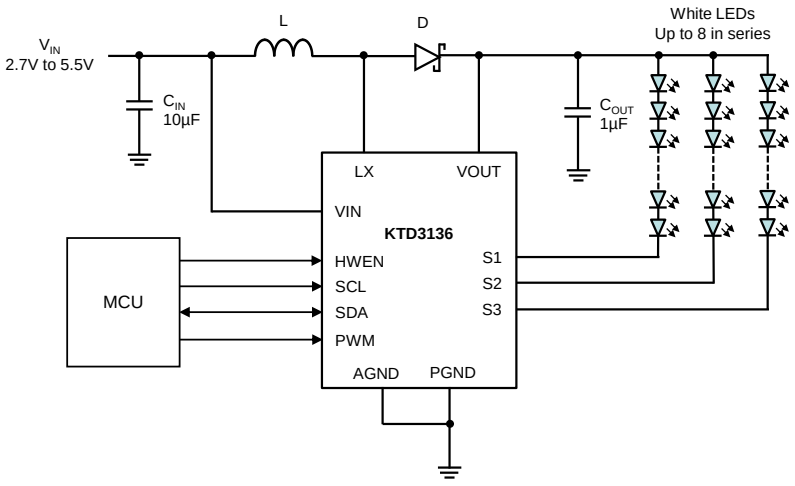
Each of the three regulated current sinks can regulate up to 29.8mA. With a maximum of 32V at the output of the step-up converter, each string can connect up to 8-LED in series for a 24-LED application.

KTD3136 is equipped with I²C interface for various controls. For additional flexibility, PWM dimming with wide range frequency and duty cycle is included to support Content Adaptive Brightness Control (CABC).

Various protection features are built into KTD3136, including cycle-by-cycle inductor current limit protection, output overvoltage protection, LED fault (open or short) protection and thermal shutdown protection.

KTD3136 is available in a RoHS compliant 12-ball 1.22mm x 1.67mm WLCSP or a 16-lead 3mm x 3mm x 0.75mm Thin-QFN package.

Typical Application

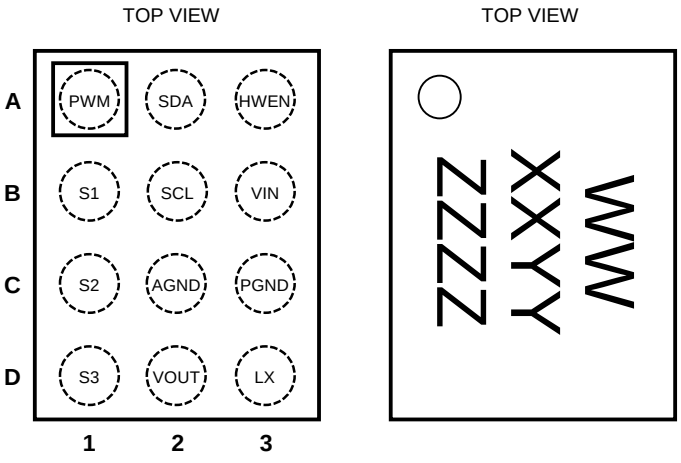


Pin Description

Pin #		Name	Function
WLCSP34-12	TQFN33-16		
A1	13	PWM	PWM dimming input pin. There is an internal 400kΩ pull-down resistor at this pin to GND.
A2	14	SDA	Bi-directional data pin of the I^2C interface.
A3	16	HWEN	Active high hardware enable pin. There is an internal 400kΩ pull-down resistor at this pin to GND.
B1	10	S1	Regulated output current sink #1.
B2	15	SCL	Clock input pin of the I^2C interface.
B3	1	VIN	Input supply pin for the IC.
C1	11	S2	Regulated output current sink #2.
C2	2, 3, 8	AGND	Analog ground pin.
C3	4	PGND	Power ground pin.
D1	9	S3	Regulated output current sink #3.
D2	7	VOUT	Output voltage sense pin of the step-up converter.
D3	5, 6	LX	Switching pin of the step-up converter.
	MC		Metal chassis. Connect to ground for electrical and thermal usage. MC is internally connected to AGND pin.

WLCSP34-12

Top View

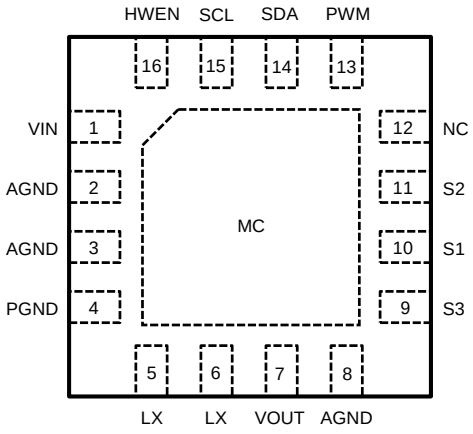


12-ball 1.22mm x 1.67mm x 0.62mm
WLCSP Package

Top Mark
WW = Device ID Code = LK
XX = Date Code, YY = Assembly Code
ZZZZ = Serial Number

TQFN33-16

Top View



16-Lead 3mm x 3mm x 0.75mm
TQFN Package

Top Mark
XX = Device ID Code = LK
YY = Date Code, Z = Assembly Code

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VIN	Input Voltage	-0.3 to 6	V
LX, VOUT	High Voltage Nodes	-0.3 to 35	V
S1, S2, S3	High Voltage Nodes	-0.3 to 22	V
SCL, SDA, PWM, HWEN	Control Pins	-0.3 to VIN+0.3	V
T_J	Junction Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C
ESD	HBM Electrical Static Discharge	2.0	kV

Thermal Capabilities[2]

Symbol	Description	Value	Units
WLCSP-12			
θ_{JA}	Thermal Resistance – Junction to Ambient	89	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	1410	mW
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-11.3	mW/°C
TQFN33-16			
θ_{JA}	Thermal Resistance – Junction to Ambient	42	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	2976	mW
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	23.8	mW/°C

Ordering Information

Part Number	Marking[3]	Operating Temperature	Package
KTD3136EUS-TR	LKXXYYZZZZ	-40°C to +85°C	WLCSP34-12
KTD3136EFJ-TR	LKYYZ	-40°C to +85°C	TQFN33-16

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
3. "XXYYZZZZ" / "YYZ" are the date code, assembly code and serial number / the date code and assembly code.

Electrical Characteristics[4]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of –40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
IC Supply						
V_{IN}	Input operating range		2.7		5.5	V
UVLO	Input under voltage lockout	Rising edge	2.27	2.45	2.65	V
$UVLO_{HYST}$	UVLO hysteresis			0.1		V
I_Q	IC operating V_{IN} current	Switching		1.9	2.4	mA
I_{SHDN}	IC shutdown V_{IN} current	Vin = 5.5V, HWEN = GND		0.5	0.8	µA
I_{SB}	IC standby V_{IN} current	Standby, V_{IN} = 4.2V, HWEN = SDA = SCL = 1.8V		7	12	µA
Step-Up Converter						
$R_{DS(ON)}$	NMOS on-resistance			0.2		Ω
I_{LIM}	Peak NMOS current limit	Default setting		2.6		A
F_{SW}	Oscillator frequency	Default setting	0.9	1.0	1.1	MHz
D_{MAX}	Maximum duty cycle	FSW = 1MHz		94		%
V_{OVP}	OVP threshold	Default setting	30	32	34	V
Current Sink						
I_{SINK}	Output current accuracy	Current setting = 1mA, T_A = 25°C	-4		4	%
		Current setting = 20.2mA, T_A = 25°C	-1.5		1.5	%
	Output current matching[5]	Current setting = 1mA, T_A = 25°C	-1.2		1.2	%
		Current setting = 20.2mA, T_A = 25°C	-0.8		0.8	%
V_{SOV}	Current sink over voltage threshold		11	12	13	V
T_{FAULT}	Current sink fault delay			6	9	µs
Logic Control						
V_{TH-L}	HWEN/PWM logic low threshold				0.4	V
V_{TH-H}	HWEN/PWM logic high threshold		1.4			V
F_{PWM}	PWM dimming frequency		0.1		100	kHz
T_{PWM_ON}	PWM on time		0.1			µs
T_{PWM_OFF}	PWM off pulse low width		20			ms
$R_{Pull-Down}$	HWEN/PWM pull down resistors			400		kΩ

4. KTD3136 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

5. The current matching among channels is defined as $|I_{SINK}-I_{AVG}|_{MAX}/I_{AVG}$.

Electrical Characteristics[6]

Symbol	Description	Conditions	Min	Typ	Max	Units
I²C-Compatible Voltage Specifications (SCL, SDA)						
V_{IL}	Input Logic Low Threshold				0.4	V
V_{IH}	Input Logic High Threshold		1.4			V
V_{OL}	SDA Output Logic Low	I_{SDA} = 3mA			0.4	V
I²C-Compatible Timing Specifications (SCL, SDA), see Figure 1						
t_1	SCL clock period		2.5			µs
t_2	Data in setup time to SCL high		100			ns
t_3	Data out stable after SCL low		0			ns
t_4	SDA low setup time to SCL low (Start)		100			ns
t_5	SDA high hold time after SCL high (Stop)		100			ns
Thermal Shutdown						
T_{J-TH}	IC thermal shutdown threshold			150		°C
	IC thermal shutdown hysteresis			15		°C

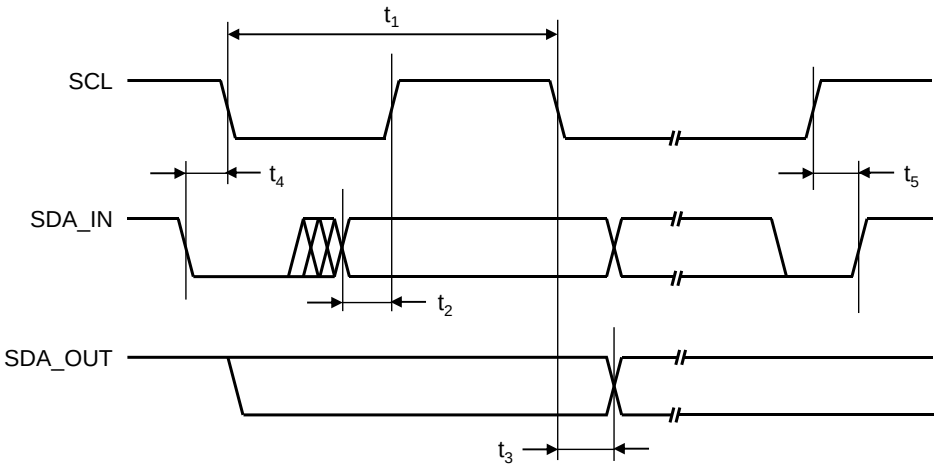


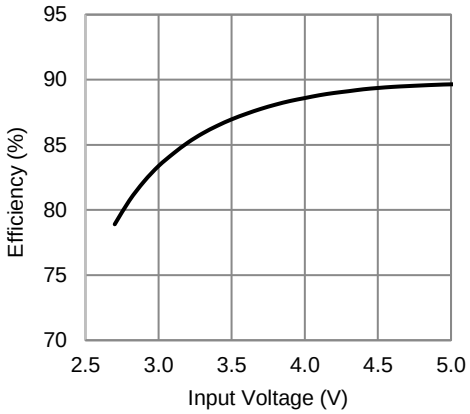
Figure 1. I²C Compatible Interface Timing

6 KTD3136 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

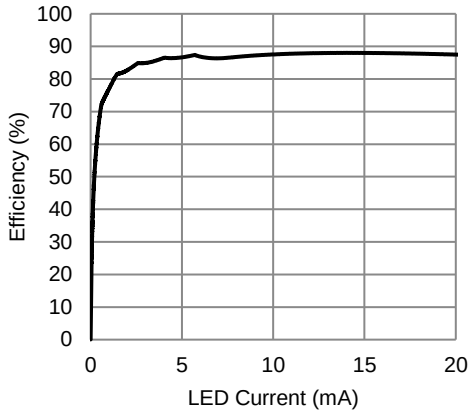
Typical Characteristics

V_{IN} = 3.6V, 3P7S LEDs, I_{LED} = 20.2mA, L = 10µH (Murata LQH3NPN100MJR), C_{IN} = 10µF, C_{OUT} = 1µF, I^2C register default settings, Temp = 25°C unless otherwise specified.

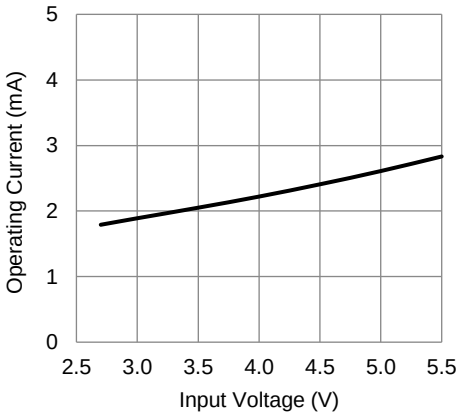
LED Driver Efficiency vs. VIN (I_{LED} = 20.2mA)



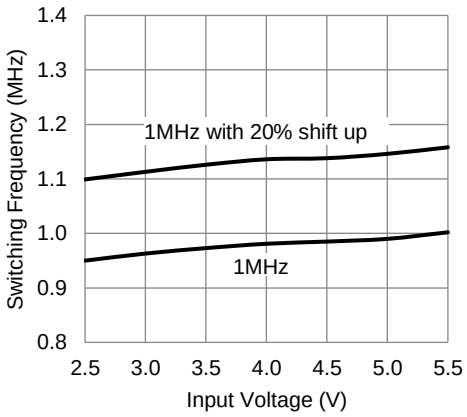
LED Driver Efficiency vs. LED Current (3P7S)



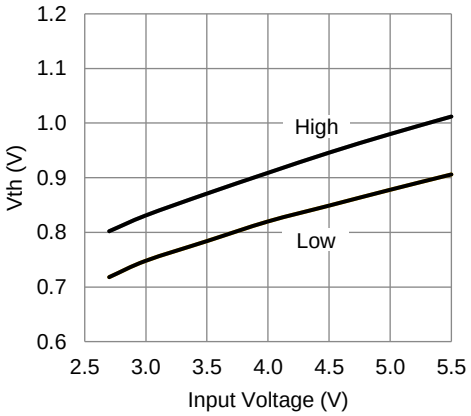
Operating Current (Switching)



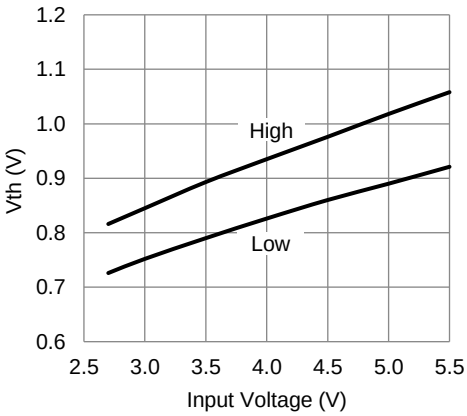
Switching Frequency vs. VIN



HWEN Logic Threshold Voltage



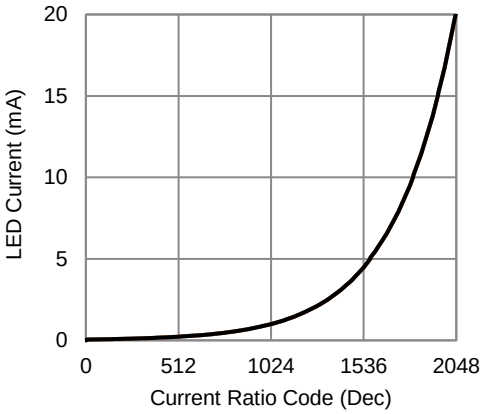
PWM Logic Threshold Voltage



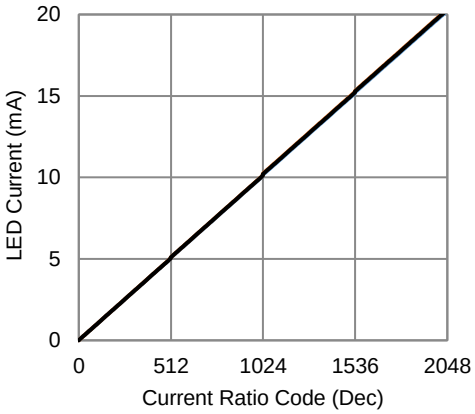
Typical Characteristics

V_{IN} = 3.6V, 3P7S LEDs, I_{LED} = 20.2mA, L = 10µH (Murata LQH3NPN100MJR), C_{IN} = 10µF, C_{OUT} = 1µF, I^2C register default settings, Temp = 25°C unless otherwise specified.

LED Current vs. Current Ratio Code (11 bits, Exponential)

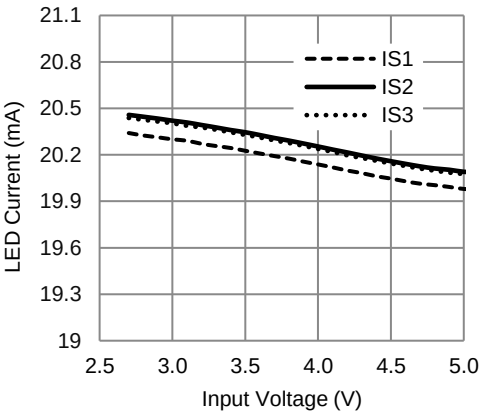


LED Current vs. Current Ratio Code (11 bits, Linear)



LED Current vs. PWM Duty Cycle (20kHz)

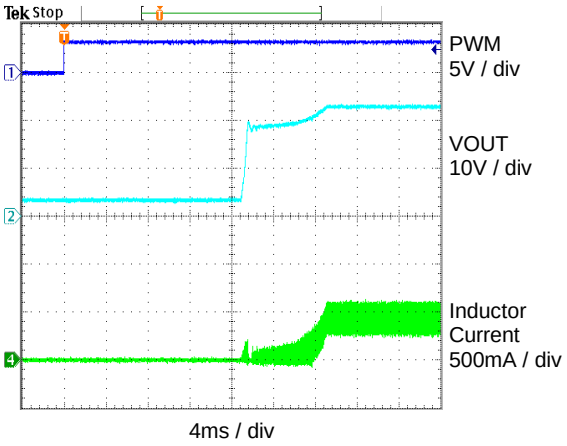
LED Current Line Regulation



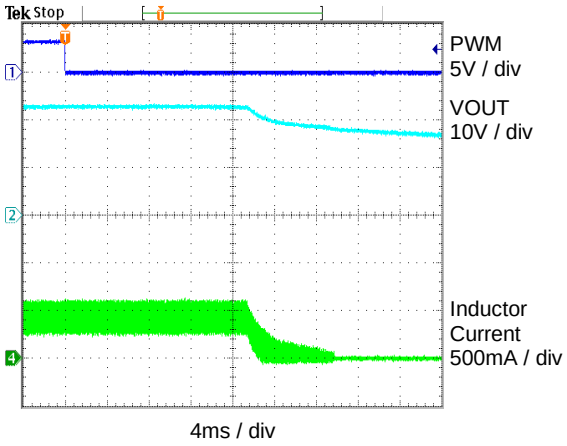
Typical Characteristics

V_{IN} = 3.6V, 3P7S LEDs, I_{LED} = 20.2mA, L = 10µH (Murata LQH3NPN100MJR), C_{IN} = 10µF, C_{OUT} = 1µF, I^2C register default settings, Temp = 25°C unless otherwise specified.

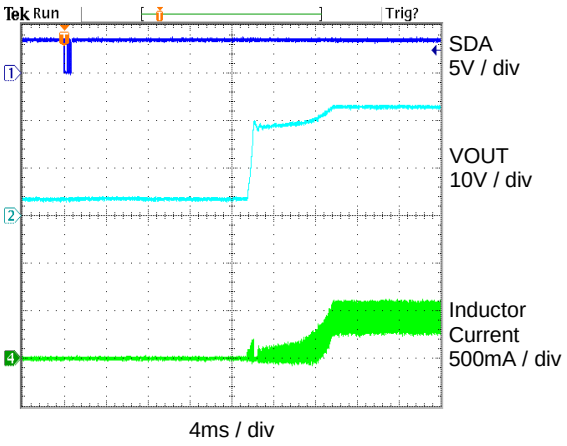
Turn On by PWM



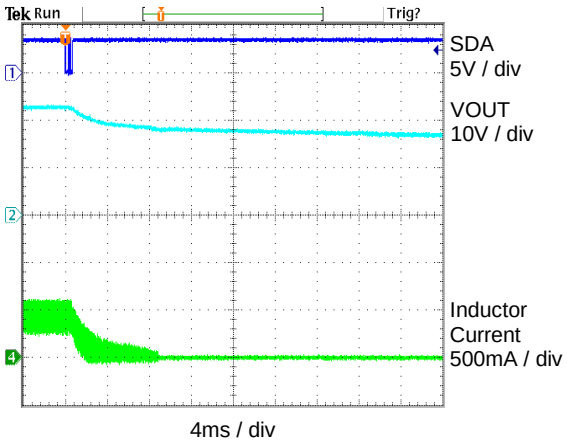
Turn Off by PWM



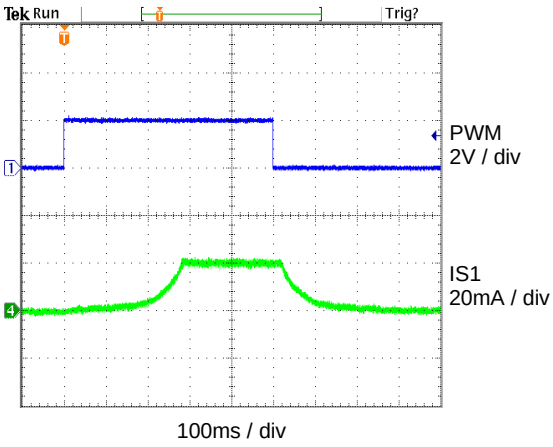
Turn On by I^2C



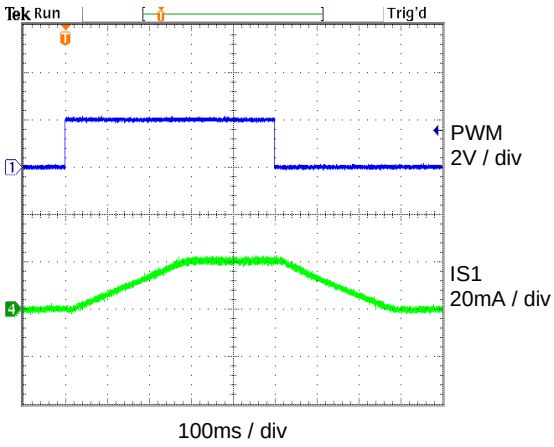
Turn Off by I^2C



Ramp Up/Down Exponential (256ms)



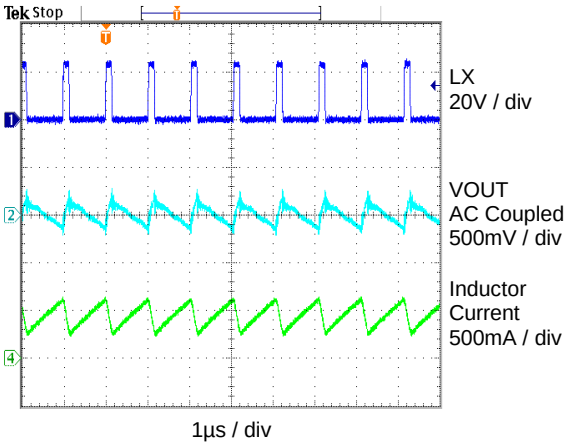
Ramp Up/Down Linear (256ms)



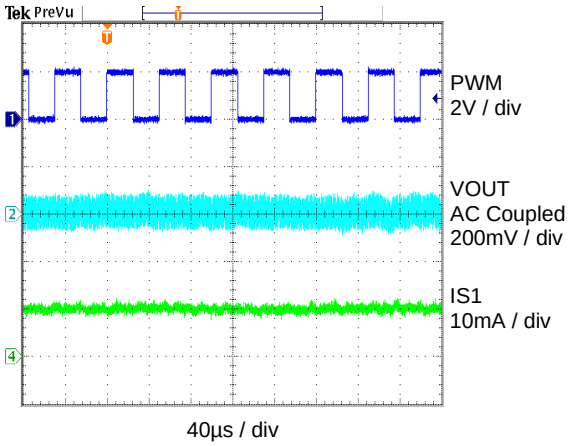
Typical Characteristics

V_{IN} = 3.6V, 3P7S LEDs, I_{LED} = 20.2mA, L = 10µH (Murata LQH3NPN100MJR), C_{IN} = 10µF, C_{OUT} = 1µF, I^2C register default settings, Temp = 25°C unless otherwise specified.

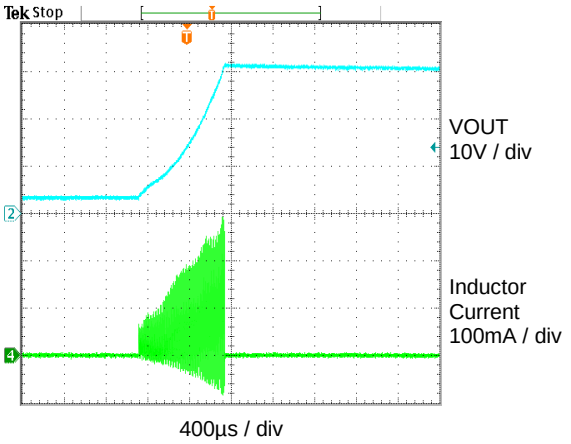
Steady State Switching



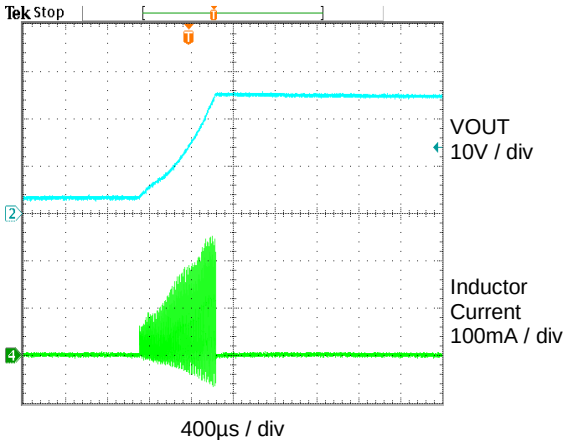
PWM Dimming (20kHz)



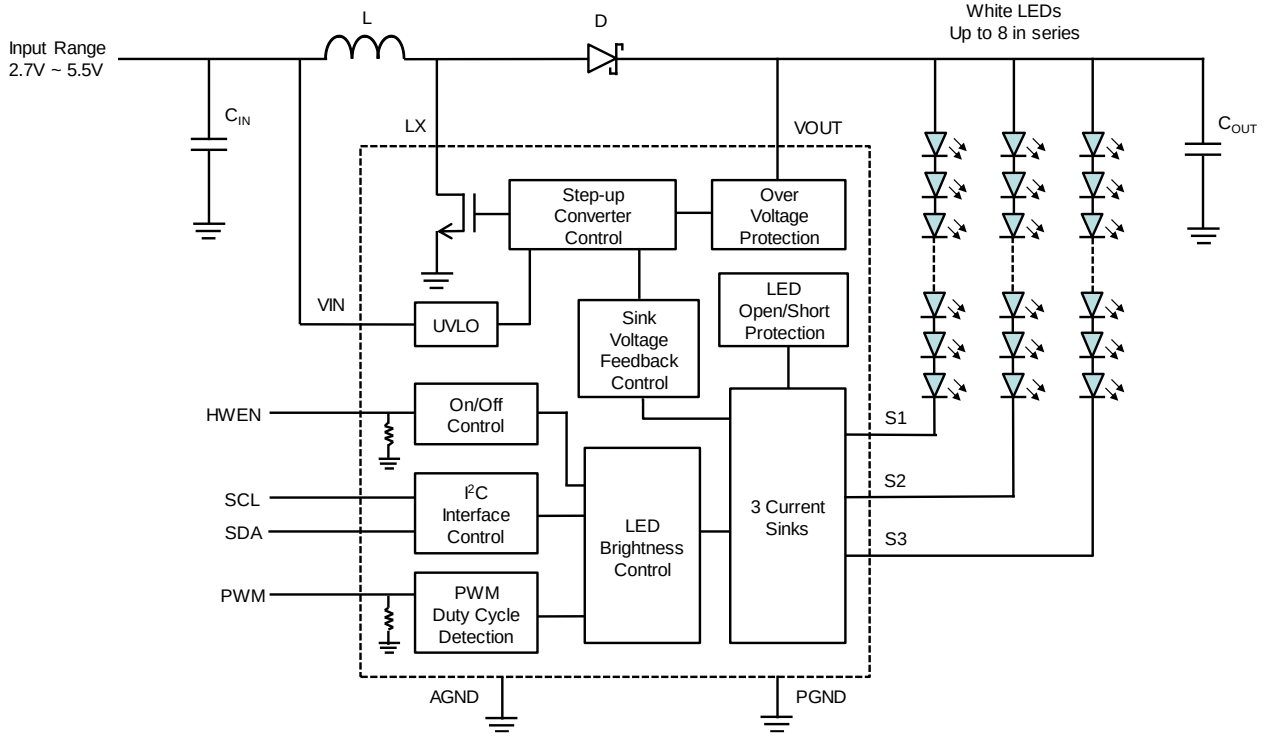
Turn On with LED Open (OVP = 32V)



Turn On with LED Open (OVP = 25.9V)



Functional Block Diagram



Functional Description

KTD3136 is a unique current regulated step-up (boost) converter. Three current sinks are integrated to drive 3 strings of LEDs with good current matching and accuracy.

The voltage step-up is accomplished by a boost topology, using an inductor-based DC-DC switching converter, in which the inductor serves as an energy storage device in the system. Unlike a traditional DC-DC boost converter with a fixed output voltage, the KTD3136 dynamically changes its output voltage depending on the load. The use of unique control schemes maintains accurate current regulation in each of the three current sinks while leaving the output voltage at a minimum, increasing the overall conversion efficiency. The internal step-up converter dynamically controls the voltage at the output high enough to drive the LED string with the highest total forward voltage.

Hardware Enable & Standby Mode

KTD3136 has a logic input HWEN pin to enable/disable the device. When HWEN is set low, the device goes into shutdown mode, all I^2C registers are reset to default, and the I^2C interface is disabled. Under this condition, the device does not respond to any I^2C command. Even when SCL/SDA's pull up voltage is much less than VIN voltage, it will not cause any extra leakage current.

When HWEN is set high, the device goes into standby mode, the I^2C interface is enabled, and the device can respond to I^2C command. Under this condition, if SCL/SDA's pull up voltage is much less than VIN voltage, it can cause a small leakage current. For example, if VIN = 4.2V and SCL/SDA's pull up voltage is 1.8V, there will be around 7µA additional leakage current from VIN in this standby mode.

Based on HWEN's connection, there are two kinds of power-up sequences, shown in Figure 2 and Figure 3.

- If HWEN is tied to VIN, once VIN goes above around 2.0V, HWEN should stay high for at least t_{wait} = 150µs time before any I^2C command can be accepted.
- If HWEN is driven by a GPIO, once HWEN goes from low to high, HWEN should stay high for at least t_{wait} = 150µs time before receiving any I^2C command.

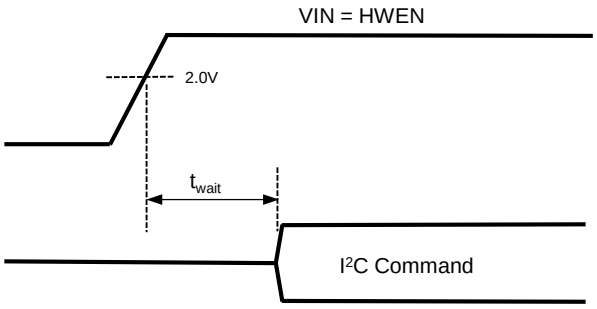


Figure 2. Power Up Sequence with HWEN Tied to VIN

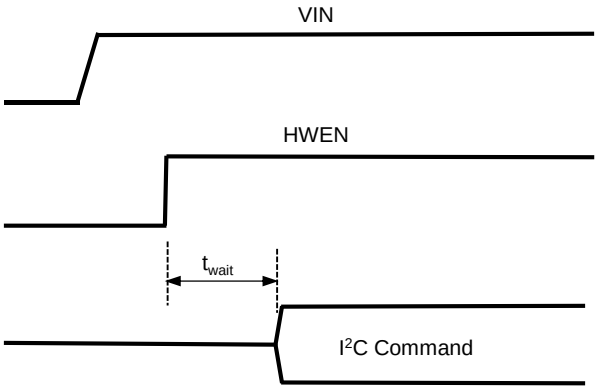


Figure 3. Power Up Sequence with HWEN Driven by GPIO

Either HWEN input or I²C command can be used to turn off the part, but there are some differences.

- If setting HWEN input low to turn off the part, the LED current will be turned off immediately without any ramp down control. After that, the I²C interface is disabled.
- If using an I²C command to turn off backlight mode while keeping HWEN high, the LED current will have ramp down control. After the LED current ramp down is finished, the I²C interface is still alive waiting for new command.

Backlight Mode

Once HWEN is set high, I²C Mode Register 0x02 Bit[0] (see Table 6) is used to enable/disable backlight mode.

Backlight Full-scale LED Current

The backlight mode's full-scale LED current I_{LED_FS} is defined as the LED current in backlight mode when PWM dimming duty cycle D_{PWM} is 100% and the LED current ratio $RATIO_{LED}$ is also 100%. I_{LED_FS} is programmed by the Mode Register 0x02 Bits[7:3] (see Table 6). Full scale current ranges from 5mA to 29.8mA with 0.8mA/step and 20.2mA as the default.

Backlight PWM Dimming

In backlight PWM mode, the input PWM duty cycle is converted internally to produce a DC output sink current (not pulsing). Backlight PWM dimming can be enabled or disabled by the PWM Register 0x06 Bit[7] (see Table 10), with enabled as default. When PWM is disabled, KTD3136 uses 100% as the dimming duty cycle for sink current calculation. When PWM is enabled, it can be programmed as either active high or active low by PWM Register 0x06 Bit[6], with active high as default. When PWM dimming is enabled, KTD3136 uses internal 20MHz sampling clock to detect the PWM duty cycle. It is recommended to have the minimum PWM on time as 0.1μs. For the example of 20kHz dimming frequency, the PWM duty cycle range can be 0.2%~100%. The PWM dimming frequency range can be as wide as 100Hz to 100kHz. When the input PWM duty cycle has a sudden change, there is a programmable transition ramp time controlled by Register 0x08 Bits[6:4] to make the LED current change smoother.

Backlight PWM Hysteresis

In backlight mode, if PWM dimming frequency is high and PWM dimming duty cycle is low, even the internal fast 20MHz sampling clock's sampling error can be sufficient to cause the output LED current jitter. KTD3136 implements PWM hysteresis control to minimize the jitter. It can be programmed by PWM Register 0x06 Bits[5:3] (see Table 10). The input PWM duty cycle is converted to an internal 11-bit digital value, this PWM hysteresis decides how many LSBs of this 11-bit digital value is changed before the output LED current can follow the change. When PWM duty cycle changes in the same direction, no hysteresis exists. Only when the PWM duty cycle's change starts to go in different direction, does the hysteresis starts to take effect, and only when the change is larger or equal to the number of LSBs programmed, the output LED current starts to follow the change. Table 1 shows the relationship between the minimum LSB(s) and the PWM duty cycle hysteresis. Table 2 summarizes PWM Register 0x06 Bits[5:3]'s minimum setting to prevent jitter under different input PWM frequency conditions. The drawback of setting PWM hysteresis too high is that the output current becomes less accurate due to the hysteresis.

Table 1. PWM Hysteresis

PWM Register 0x06 Bits[5:3]	Minimum LSB(s)	PWM Duty Cycle Hysteresis
000	0	0/2047 = 0%
001	2	2/2047 = 0.10%
010	4	4/2047 = 0.20%
011	6	6/2047 = 0.29%
100	8	8/2047 = 0.39%
101	10	10/2047 = 0.48%
110	12	12/2047 = 0.59%
111	14	14/2047 = 0.68%

Table 2. Register 0x06 Bits[5:3]'s Minimum Setting

PWM Dimming Frequency (kHz)	Sampling Error	Register 0x06 Bits[5:3]'s Minimum Setting to Prevent Jitter
0.1	0.0005%	001
1	0.005%	001
5	0.025%	001
10	0.05%	001
20	0.1%	010
40	0.2%	011
100	0.5%	110

Backlight LED Current

The LED current is always a DC current. It can be programmed for either exponential mapping mode or linear mapping mode by Register 0x03 Bit[1]. These two modes determine the transfer characteristic of dimming code to LED current. It also has 11-bit control, including the 8-bit MSBs from LED Current Ratio MSB Register 0x05 Bits[7:0] (see Table 9) and the 3-bit LSBs from LED Current Ratio LSB Register 0x04 Bits[2:0] (see Table 8). If only 8-bit dimming is needed, the 3-bit LSBs should be kept as '111' while the 8-bit MSBs are programmed. If 11-bit dimming ratio is needed, the 3-bit LSBs should be programmed first, then the 8-bit MSBs are programmed. Only programming the 3-bit LSBs doesn't change the current ratio until the 8-bit MSBs are programmed.

In linear mapping 8-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} \times D_{PWM} \times \frac{Code+1}{256} \qquad (Code = 0 \sim 255)$$

where I_{LED_FS} is the backlight full-scale LED current, D_{PWM} is the input PWM duty cycle if PWM dimming is enabled, otherwise D_{PWM}=1.

In linear mapping 11-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} \times D_{PWM} \times \frac{Code+1}{2048} \qquad (Code = 1 \sim 2047)$$

For linear mapping 11-bit dimming's Code 0, current sink and boost converter will be disabled, LED will be turned off.

In exponential mapping 8-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} \times D_{PWM} \times \frac{1.002931237^{\ Code \times 8+7}}{400} \qquad (Code = 0 \sim 255)$$

In exponential mapping 11-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} \times D_{PWM} \times \frac{1.002931237^{\ Code}}{400} \qquad (Code = 1 \sim 2047)$$

For exponential mapping 11-bit dimming's Code 0, current sink and boost converter will be disabled, LED will be turned off.

Turn On/Off Ramp

When backlight mode is enabled from standby mode or disabled to standby mode, the LED current waveform's turn on/off time is controlled by Turn On/Off Ramp Register 0x07 Bits[7:4] and Bits[3:0] respectively (see Table 11). The 16 options range from 512µs to 16384ms, with 8ms as default. The shape of the turn on/off ramp in backlight mode can also be programmed as exponential or linear through the Control Register 0x03 Bit[2], with exponential as default. If the switching frequency shift up by 20% is selected, all ramp times will be decreased by 20%.

I²C Dimming Transition Ramp

After the turn on ramp is finished, if the LED current is changed from one value to the other by I²C dimming Register 0x04 and Register 0x05, the transition ramp time can be programmed by Transition Ramp Register 0x08 Bits[3:0] (see Table 12). For Code 0001~1111, there are 15 programmable options (128ms ~ 1024ms) of the ramp time, it is independent of the I²C dimming code change and will keep the same no matter how big the dimming code change is. For Code 0000, the slope of the ramp is fixed as 1us/step, so the final transition ramp time is dependent on the 11-bit I²C dimming code change. If the switching frequency shift up by 20% is selected, all transition times will be decreased by 20%.

PWM Dimming Transition Ramp

After the turn on ramp is finished, if the LED current is changed from one value to the other by PWM dimming duty cycle, the transition ramp time can be programmed by Transition Ramp Register 0x08 Bits[6:4] (see Table 12). For this transition ramp, its slope is fixed, so the final transition ramp time is dependent on the change of the PWM duty cycle. If the switching frequency shift up by 20% is selected, all transition times will be decreased by 20%.

Channel Enable/Disable

To disable any channel, there are two options.

- Connect the associated sink pin to GND. During the startup, the IC will automatically detect and disable the corresponding channel.
- Program PWM Register 0x06 Bits[2:0] (See Table 10) to enable/disable the channel(s), with enable as default.

Switching Frequency

The step-up converter's switching frequency can be programmed to 1MHz or 500kHz by Control Register 0x03 Bit[6] (See Table 7), with 1MHz as default. The adjustment of the switching frequency can optimize the efficiency under different load current conditions. The frequency can also be programmed to shift up by 20% using the

Control Register 0x03 Bit[7], with no shift as default. The frequency shift function is to prevent noise interference if the selected switching frequency is within the sensitive frequency range of the system.

Over Voltage Protection (OVP)

The output voltage of the step-up converter is protected by OVP, its threshold can be programmed by the Control Register 0x03 Bit[5] (See Table 7) as 32V or 25.9V, with 32V as default.

Inductor Current Limit Protection

The step-up converter is protected by cycle-by-cycle inductor current limit protection, its threshold can be programmed by the Control Register 0x03 Bit[3] (See Table 7) as 2.6A or 1.8A, with 2.6A as default.

Software Reset

All the I^2C registers can be reset to their default settings by writing '1' to the Software Reset Register 0x01 Bit[0] (see Table 5), this bit will be reset to '0' automatically after the software reset.

LED Fault Protection

Each current sink is protected against LED short or open conditions.

If LED short circuit condition arises, the current sink continues to regulate until the sink node voltage goes above V_{SOV} (12V) for more than 6µs, then the Current Sink Fault Protection is triggered, the boost converter will be stopped to prevent VOUT from rising up, and current sink will be kept on to discharge VOUT.

In case of an LED failing open, the current sink voltage of the failed string will go close to ground and dominate the boost converter control loop. As a result, the output voltage will increase until it reaches the overvoltage threshold. Once the overvoltage incident is triggered, the boost converter will be turned off, and all the other healthy channels will be on to discharge VOUT. During the rise of VOUT, if the healthy channels' sink voltages reach V_{SOV} (12V) for 6µs before VOUT reaches its overvoltage threshold, this will trigger LED short protection, not LED open protection.

After LED open or short protection, user needs to restart the IC by toggling HWEN or sending software reset command or resetting backlight mode.

UVLO

Under voltage lock-out (UVLO) featured is included to monitor the input voltage VIN. Once VIN drops below UVLO falling threshold, the current sinks are disabled and the boost converter stops switching. After VIN increases above UVLO rising threshold, the boost converter and the current sinks will resume to their previous setting.

Thermal Shutdown

Thermal shutdown feature is included to monitor the IC's junction temperature. If it reaches 150°C, the current sinks are disabled and the boost converter stops switching. Once it drops 15°C to approximately 135°C, the boost converter and the current sinks will resume to their previous setting.

Status Report

Various status conditions can be reported through I²C interface by the read-only Status Register 0x0A (See Table 13), including channel fault (LED open or short), OVP, UVLO, OCP (inductor current limit) and thermal shutdown. Channel fault, UVLO and thermal shutdown are real-time results when backlight mode is enabled and it can be reset by toggling backlight mode. The remaining faults are latched results and can be reset by reading back Status Register 0x0A through I²C interface or toggling backlight mode. All the status bits can also be reset by VIN power on reset, software reset or toggling HWEN.

Application Information

I²C Serial Data Bus

KTD3136 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. KTD3136 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. KTD3136 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined in Figure 4:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

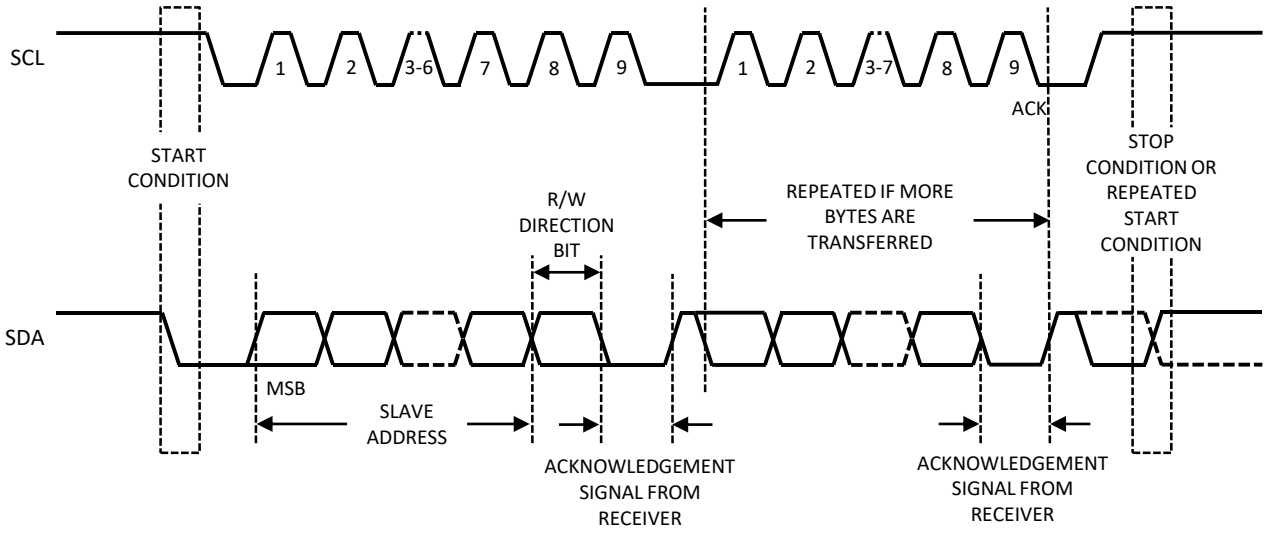


Figure 4. Data Transfer on I²C Serial Bus

KTD3136 7-bit slave device address is 0110110 binary (0x36h).

There are two kinds of I²C data transfer cycles: write cycle and read cycle.

I²C Write Cycle

For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of '0' for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure 5 shows the sequence of the I²C write cycle.

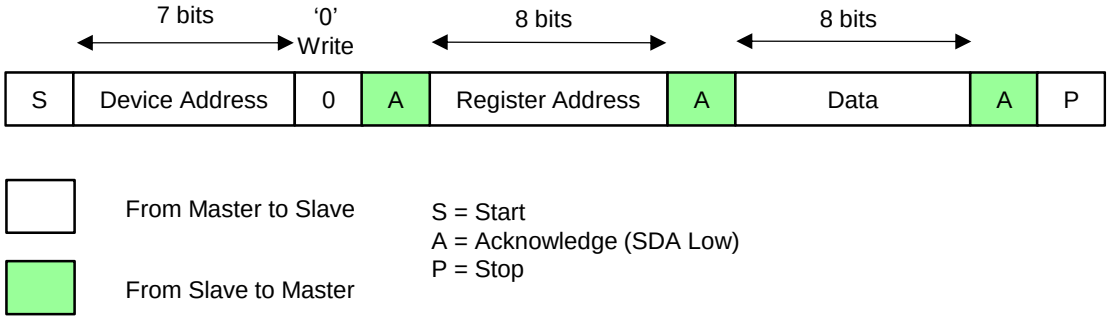


Figure 5. I²C Write Cycle

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0110110 for KTD3136) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generate stop condition to finish the write cycle.

I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register data to read. Figure 6 shows the steps of the I²C read cycle.

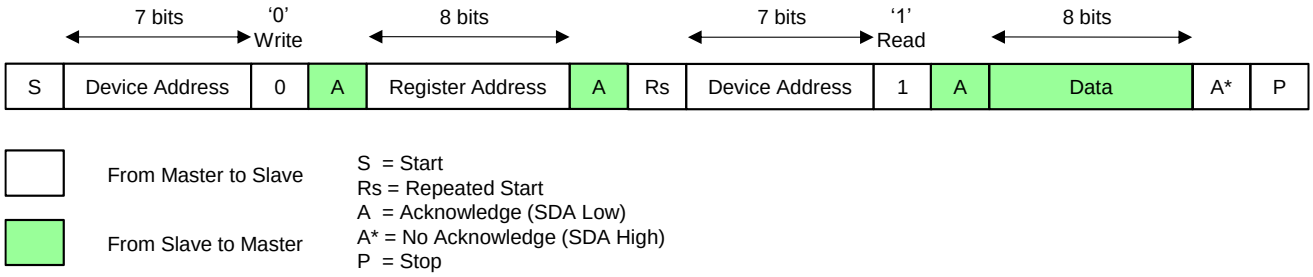


Figure 6. I²C Read Cycle

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0110110 for KTD3136) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address (0110110 for KTD3136) and 1-bit data direction '1' for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.
- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.
- If master sends no acknowledge, the slave will stop sending the data.
- Master generate stop condition to finish the read cycle.

I²C Register Map

Table 3 summarizes KTD3136's 10 I²C registers, their read/write settings and default values. They can be reset to default values by VIN power on reset, toggling HWEN or I²C software reset.

Table 3. I²C Register Map

Register Name	Address (Hex)	R/W	Default Value
Device ID Register	0x00	R	18
SW Reset Register	0x01	R/W	00
Mode Register	0x02	R/W	98
Control Register	0x03	R/W	68
LED Current Ratio LSB Register	0x04	R/W	07
LED Current Ratio MSB Register	0x05	R/W	FF
PWM Register	0x06	R/W	1F
Turning On/Off Ramp Register	0x07	R/W	44
Transition Ramp Register	0x08	R/W	00
Status Register	0x0A	R	00

Table 4. Device ID Register (0x00)

Bits[7:5]	Bits[5:3] Device ID	Bits[2:0]
Reserved	011	Reserved

Table 5. SW Reset Register (0x01)

Bits[7:1]	Bit[0] Software Reset
Reserved	0: Don't reset (Default) 1: Reset

Note: Writing software reset bit to '1' will reset all I^2C registers to their default values, then this bit will be internally reset back to '0'.

Table 6. Mode Register (0x02)

Bits[7:3] Backlight Full-scale LED Current I_{LED_FS}	Bits[2:1]	Bit[0] Backlight Mode
I_{LED_FS} = 5mA + Code x 0.8mA 11111 : 29.8mA …. 10011 : 20.2mA (Default) …. 00001 : 5.8mA 00000 : 5mA	Reserved	0: Disable (Default) 1: Enable

Table 7. Control Register (0x03)

Bit[7] Switching Frequency Shift Up	Bit[6] Switching Frequency	Bit[5] OVP Control	Bit[4]	Bit[3] Inductor Current Limit	Bit[2] Backlight Turn On/Off Ramp Shape	Bit[1] Backlight Current Mapping	Bit[0]
0: No Shift (Default) 1: Shift Up by 20%	0: 500kHz 1: 1000kHz (Default)	0: 25.9V 1: 32V (Default)	Reserved Must be written with "0"	0: 1.8A 1: 2.6A (Default)	0: Exponential (Default) 1: Linear	0 : Exponential (Default) 1 : Linear	Reserved

Note: When Backlight Current Mapping setting is changed, the LED current change will not take effect until Register 0x05 is programmed.

Table 8. Brightness Register LSB (0x04)

Bits[7:3]	Bits[2:0] LED Current Ratio LSBs (3 bits)
Reserved	Lower 3 bits of the 11-bit LED current ratio (Default: 111)

Table 9. Brightness Register MSB (0x05)

Bits[7:0] LED Current Ratio MSBs (8 bits)
Higher 8 bits of the 11-bit LED current ratio (Default: 11111111)

Note:
1. If only using 8-bit current ratio, keep the 3-bit LSBs as '111' and only program the 8-bit MSBs.
2. If using 11-bit current ratio, the 3-bit LSBs should be programmed first, then the 8-bit MSBs can be programmed to take effect. Even if only the 3-bit LSBs need to be changed, the 8-bit MSB should always be programmed next to make the 3-bit LSBs change taking effect.
3. For 11-bit program code 11'b00000000000, both boost converter and current sinks are turned off.

Table 10. PWM Register (0x06)

Bit[7] PWM Enable	Bit[6] PWM Active	Bits[5:3] PWM Hysteresis	Bit[2] CH3 Enable	Bit[1] CH2 Enable	Bit[0] CH1 Enable
0: Enable (Default) 1: Disable	0: High Active (Default) 1: Low Active	000: 0 LSB 001: 2 LSBs 010: 4 LSBs 011: 6 LSBs (Default) 100: 8 LSB 101: 10 LSBs 110: 12 LSBs 111: 14 LSBs	0: Disable 1: Enable (Default)	0: Disable 1: Enable (Default)	0: Disable 1: Enable (Default)

Table 11. Turn On/Off Ramp Register (0x07)

Bits[7:4] Turn On Ramp Time	Bits[3:0] Turn Off Ramp Time
0000: 512µs 0001: 1ms 0010: 2ms 0011: 4ms 0100: 8ms (Default) 0101: 16ms 0110: 32ms 0111: 64ms 1000: 128ms 1001: 256ms 1010: 512ms 1011: 1024ms 1100: 2048ms 1101: 4096ms 1110: 8192ms 1111: 16384ms	0000: 512µs 0001: 1ms 0010: 2ms 0011: 4ms 0100: 8ms (Default) 0101: 16ms 0110: 32ms 0111: 64ms 1000: 128ms 1001: 256ms 1010: 512ms 1011: 1024ms 1100: 2048ms 1101: 4096ms 1110: 8192ms 1111: 16384ms

Note: If the switching frequency shift up by 20% is selected, all the ramp times will be decreased by 20%.

Table 12. Transition Ramp Register (0x08)

Bit[7]	Bits[6:4] PWM Dimming Transition Ramp Time	Bits[3:0] I²C Dimming Transition Ramp Time
Reserved	000 : 2ms (Default) 001 : 4ms 010 : 8ms 011 : 16ms 100 : 32ms 101 : 64ms 110 : 128ms 111 : 256ms	0000 : 1μs/step (Default) 0001 : 128ms 0010 : 192ms 0011 : 256ms 0100 : 320ms 0101 : 384ms 0110 : 448ms 0111 : 512ms 1000 : 576ms 1001 : 640ms 1010 : 704ms 1011 : 768ms 1100 : 832ms 1101 : 896ms 1110 : 960ms 1111 : 1024ms

Note:
1. If the switching frequency shift up by 20% is selected, all the transition times will be decreased by 20%.
2. The PWM Dimming Transition Ramp Time in the table is defined as the time to change between minimum PWM duty cycle and the maximum PWM duty cycle. The final transition time is the multiplication of the time in the table and the change of the PWM duty cycle.
3. For I²C Dimming Transition Ramp Time in the table, all the ramp times are fixed when current ramps from one level to the other except "0000" setting. For "0000" setting, the ramp slope is 1us/step, the final ramp time is proportional to the 11-bit current steps.

Table 13. Status Register (0x0A)

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0: Normal (Default) 1: CH3 Fault	0: Normal (Default) 1: CH2 Fault	0: Normal (Default) 1: CH1 Fault	Reserved	0: Normal (Default) 1: OVP	0: Normal (Default) 1: UVLO	0: Normal (Default) 1: OCP	0: Normal (Default) 1: Thermal Shutdown

Note:
1. CH1/2/3 fault, UVLO and thermal shutdown are real-time results when backlight mode is enabled and can be reset by toggling backlight mode.
2. OVP and OCP are latched results and can be reset by reading back Status Register 0x0A through I²C or toggling backlight mode.
3. All the status bits can be reset by VIN power on reset, software reset or toggling HWEN.

Capacitor Selection

Small size ceramic capacitors with low ESR are ideal for all applications. A 10μF input capacitor and a 1μF~2.2 μF output capacitor are suggested. The voltage rating of these capacitors should exceed the maximum possible voltage at the corresponding pins, and these capacitors should be as close as possible to the IC. Table 14 shows the recommended capacitor vendors.

Table 14. Recommended Capacitor Vendors

Manufacturer	Website
Murata	www.murata.com
AVX	www.avx.com
Taiyo Yuden	www.t-yuden.com

Inductor Selection

An inductor of 4.7µH to 10µH with low DCR can be selected for the boost converter. To decide the current rating of the inductor required for the application, the following equation can be used to estimate the peak inductor current I_{PEAK} in continuous conduction mode (CCM):

$$I_{PEAK} = \frac{V_{OUT(MAX)} \times I_{OUT(MAX)}}{V_{IN(MIN)} \times \eta} + \frac{V_{IN(MIN)}}{2L \times F_{SW}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}\right)$$

where $V_{OUT(MAX)}$ is the maximum output voltage, $V_{IN(MIN)}$ is the minimum input voltage, $I_{OUT(MAX)}$ is the maximum output current, F_{SW} is the boost converter's switching frequency, L is the inductor value, η is the boost converter's efficiency under that condition. Table 15 shows recommended inductors under different application conditions.

Table 15. Recommended Inductors

Application	Inductor Part Number	Value (µH)	DCR (mΩ)	Saturation Current (A)	Dimensions (mm)	Manufacturer
3P7S (Max. 20mA/Ch)	LQH3NPN100MJR	10	240 typ	0.810	3.0 x 3.0 x 1.1	Murata

Schottky Diode Selection

Using a schottky diode is recommended because of its low forward voltage drop and fast reverse recovery time. The average current rating of the schottky diode should exceed the maximum output current, and its peak current rating should exceed the peak inductor current. Its voltage rating should also exceed the OVP setting. Table 16 shows the recommended schottky diode.

Table 16. Recommended Schottky Diode

Application	Schottky Diode Part Number	Forward Voltage (V)	Forward Current (A)	Reverse Voltage (V)	Manufacturer
All	PMEG4010B	0.54	1	40	NXP

Recommended PCB Layout

PCB layout is very important for high frequency switching regulators in order to keep the loop stable and minimize noise. The input capacitor (C_{IN}) should be very close to the IC's VIN pin and PGND pin in order to get the best decoupling. The path between the inductor, LX pin, schottky diode and the output capacitor (C_{OUT}) should be kept as short as possible to minimize noise and ringing. To reduce power loss, the trace through the inductor, LX pin, schottky diode and C_{OUT} should be as short and wide as possible. Both input and output capacitors' GND terminals should be connected together on the PCB top layer and on the bottom layer GND plane. Figure 7 shows the WLCSP-12 recommended PCB layout and Figure 8 shows the TQFN-16 recommended PCB layout.

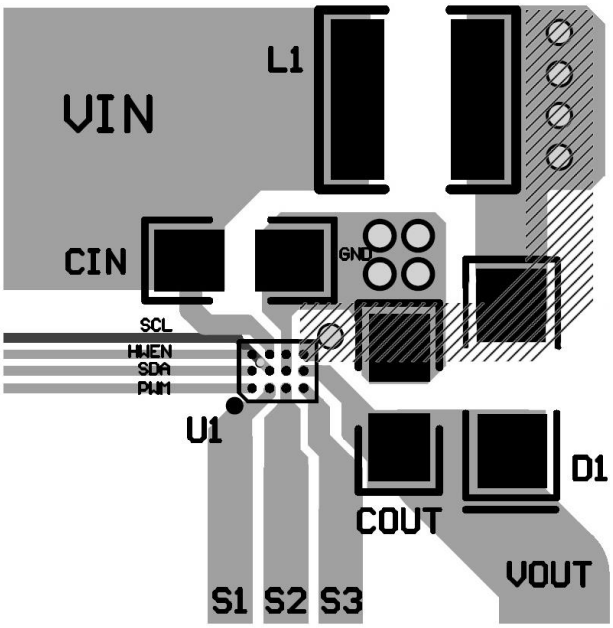


Figure 7. WLCSP-12 Recommended PCB Layout

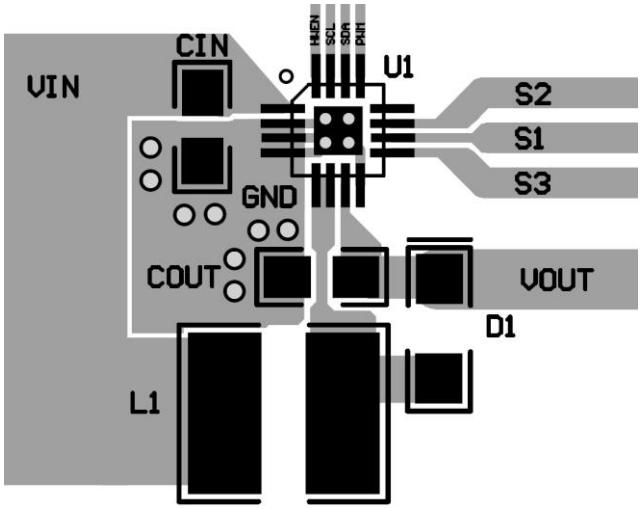
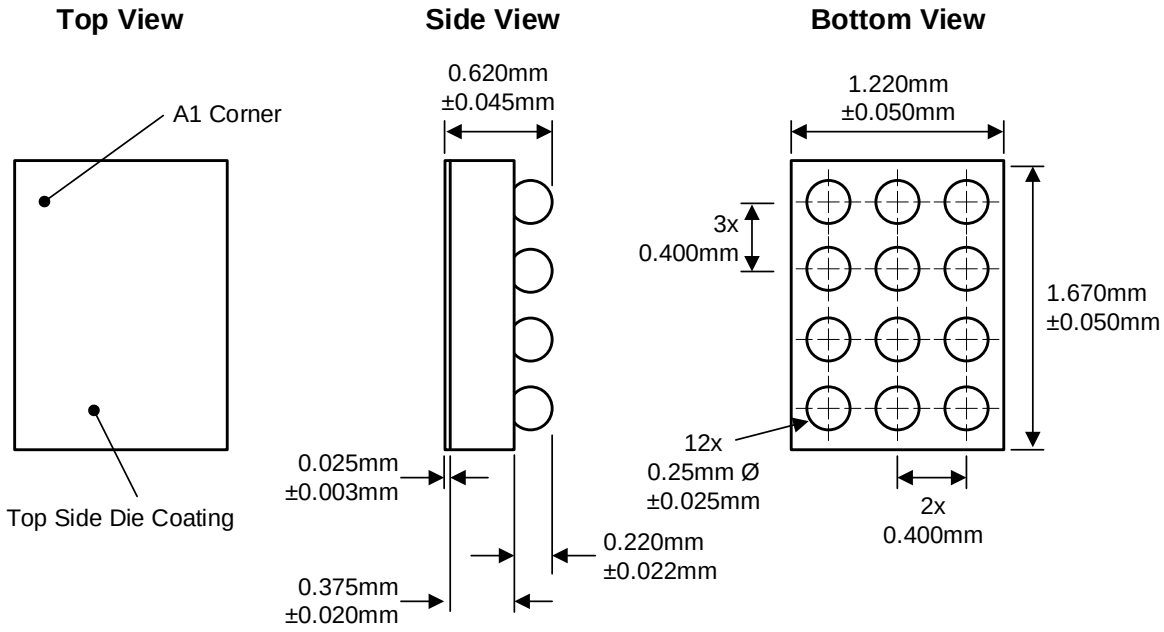


Figure 8. TQFN-16 Recommended PCB Layout

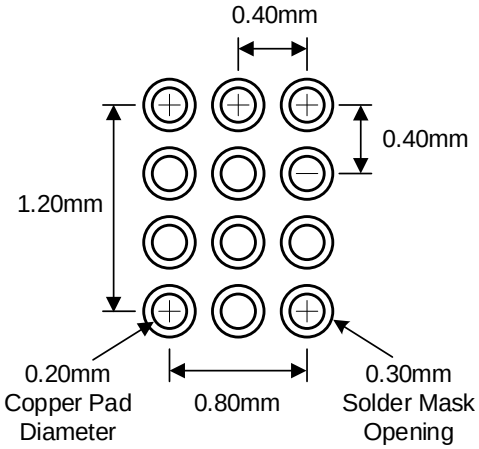
Packaging Information

WLCSP34-12 (1.220mm x 1.670mm x 0.620mm)

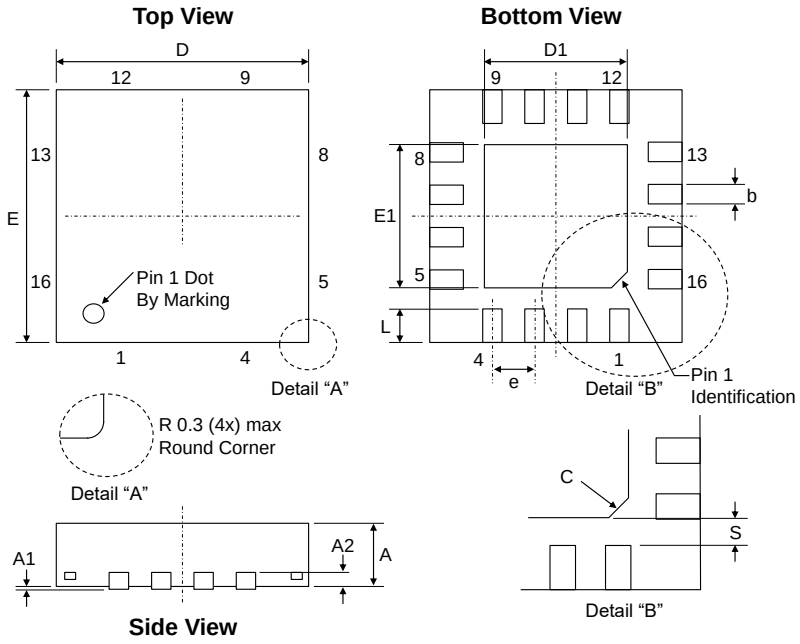


Recommended Footprint

(NSMD Pad Type)

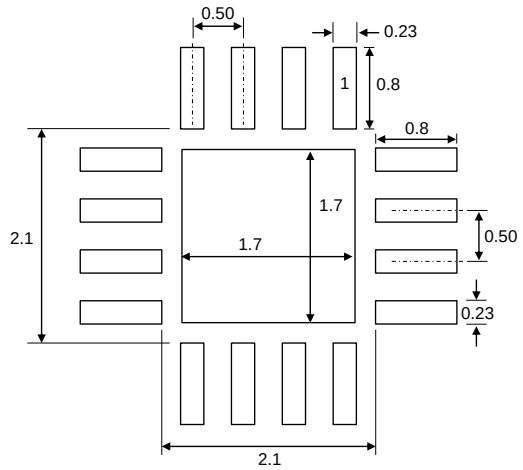


TQFN33-16 (3.00mm x 3.00mm x 0.75mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.65	0.75	0.85
A1	0.000	0.025	0.050
A2	0.154	0.203	0.280
b	0.18	0.23	0.30
C		0.3REF	
D	2.95	3.00	3.05
D1		1.7REF	
E	2.95	3.00	3.05
E1		1.7REF	
e	0.45	0.50	0.55
L	0.30	0.40	0.50
S		0.25REF	

Recommended Footprint



* Dimensions are in millimeters.