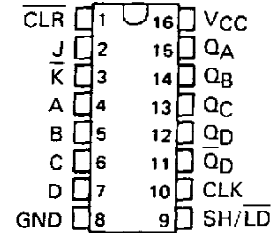


**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**
MARCH 1974—REVISED MARCH 1988

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and $\bar{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High Performance:
Accumulators/Processors
Serial-to-Parallel, Parallel-to-Serial
Converters

SN54195, SN54LS195A, SN54S195 . . . J OR W PACKAGE
SN74195 . . . N PACKAGE
SN74LS195A, SN74S195 . . . D OR N PACKAGE

(TOP VIEW)



description

These 4-bit registers feature parallel inputs, parallel outputs, J- $\bar{K}$ serial inputs, shift/load (SH/LD) control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

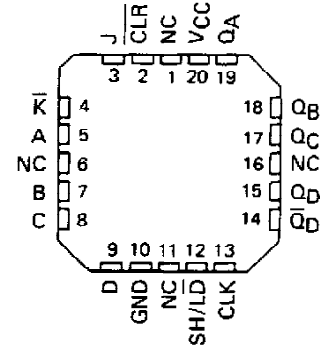
Parallel loading is accomplished by applying the four bits of data and taking SH/LD low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when SH/LD is high. Serial data for this mode is entered at the J- $\bar{K}$ inputs. These inputs permit the first stage to perform as a J- $\bar{K}$, D-, or T-type flip-flop as shown in the function table.

The high-performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

SN54LS195, SN54S195 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'195	39 MHz	195 mW
'LS195A	39 MHz	70 mW
'S195	105 MHz	350 mW

FUNCTION TABLE

INPUTS				OUTPUTS					
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL	PARALLEL	Q_A	Q_B	Q_C	Q_D	$\bar{Q}_D$
			J $\bar{K}$	A B C D					
L	X	X	X X	X X X X	L	L	L	L	H
H	L	↑	X X	a b c d	a	b	c	d	$\bar{d}$
H	H	L	X X	X X X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\bar{Q}_{D0}$
H	H	↑	L H	X X X X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	L L	X X X X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	H H	X X X X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	H L	X X X X	$\bar{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at A, B, C, or D, respectively

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established

Q_{An} , Q_{Bn} , Q_{Cn} = the level of Q_A , Q_B , or Q_C , respectively, before the most-recent transition of the clock

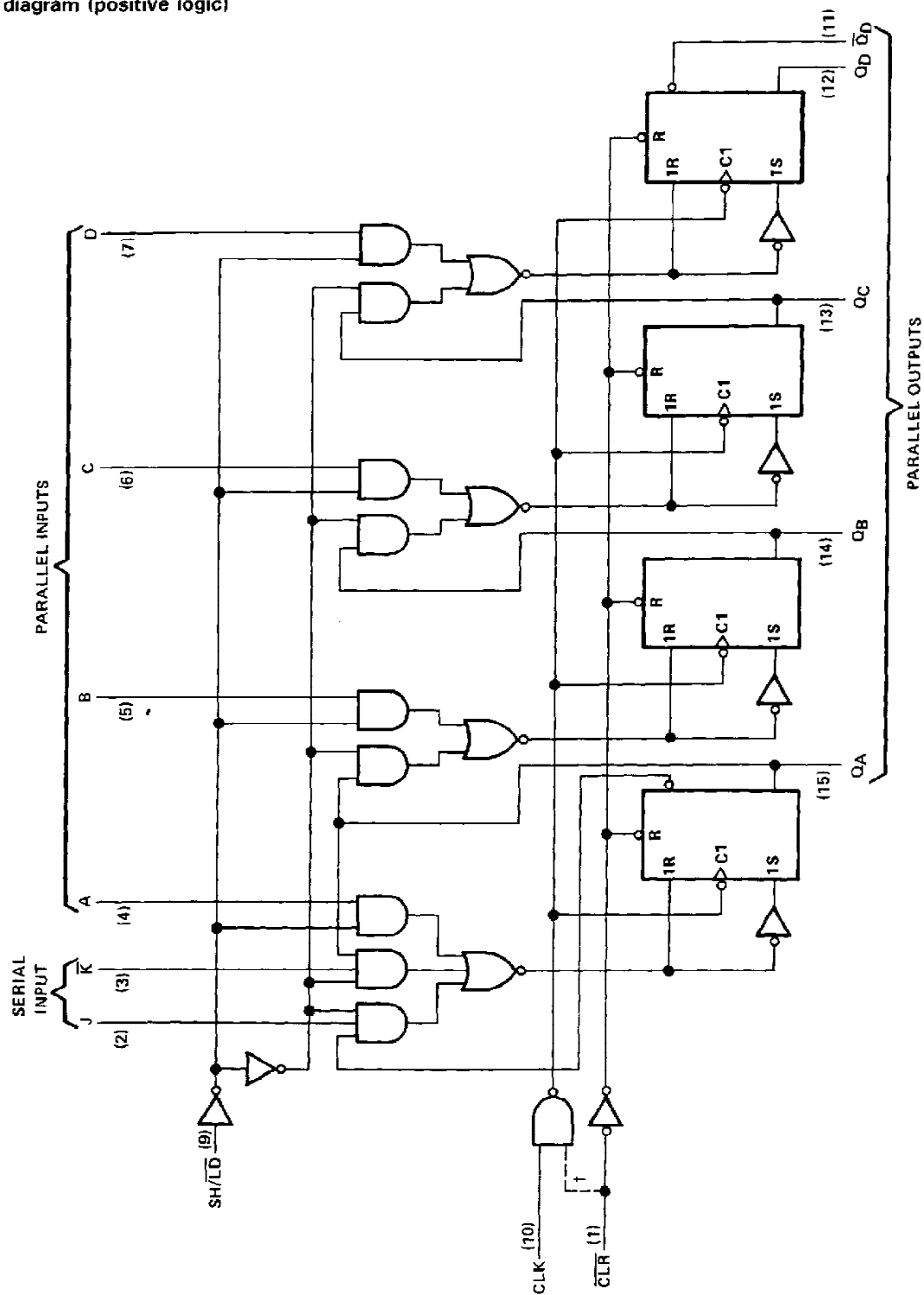
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

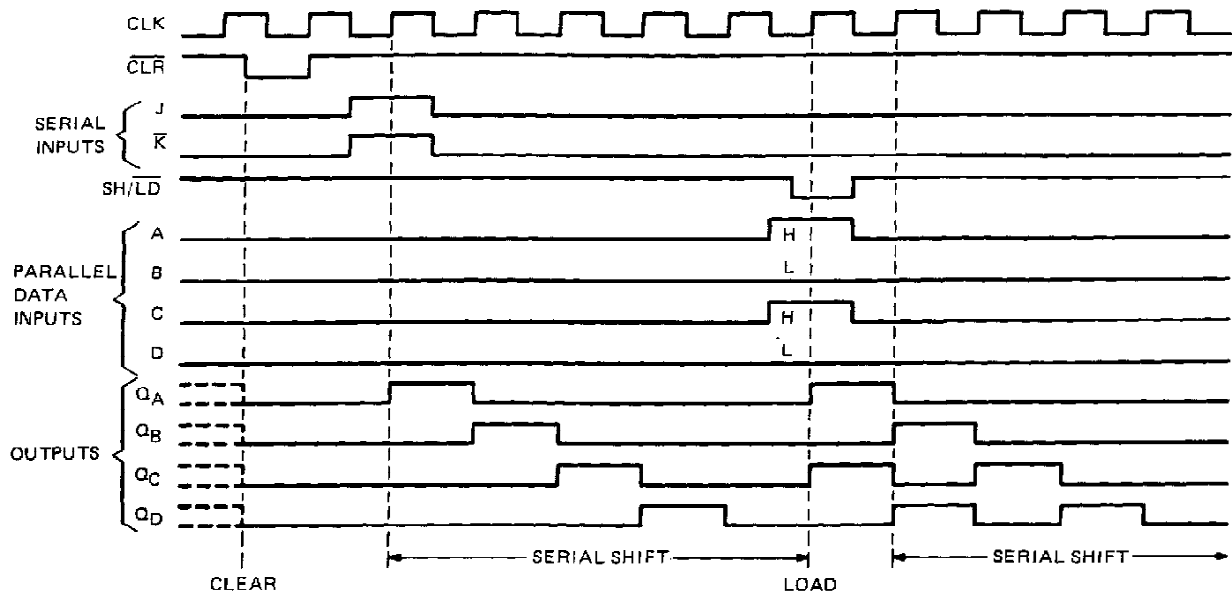
logic diagram (positive logic)



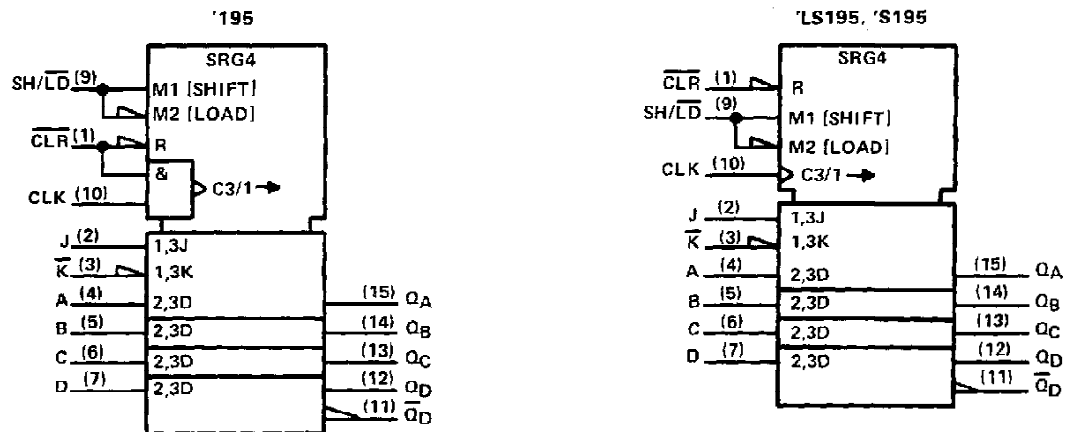
† This connection is made on '195 only.
Pin numbers shown are for D, J, N, and W packages.

**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

typical clear, shift, and load sequences



logic symbols†

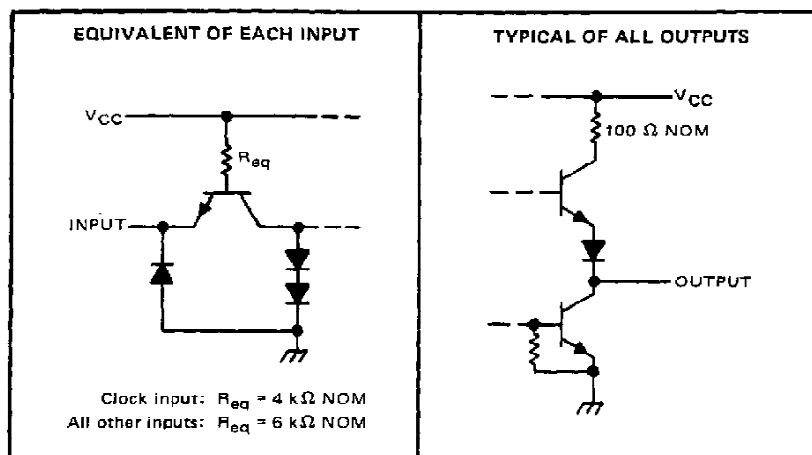


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers are for D, J, N, and W packages.

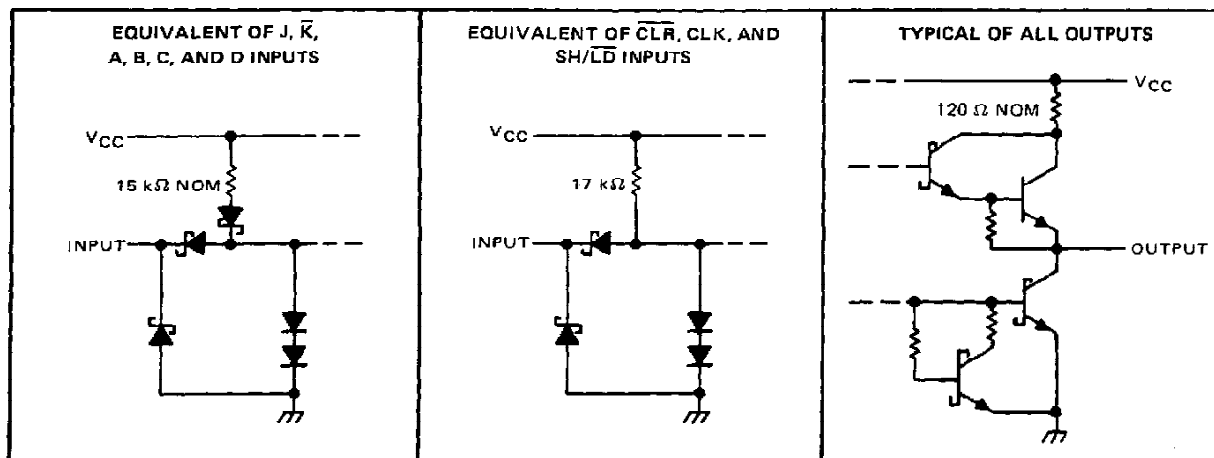
SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

schematics of inputs and outputs

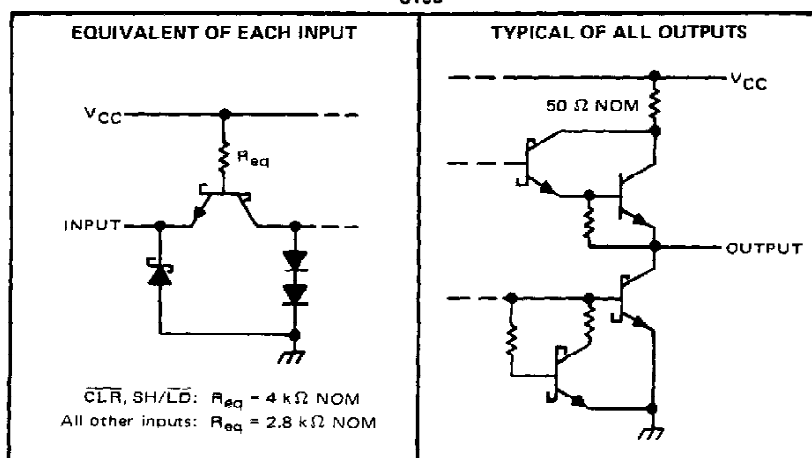
'195



'LS195A



'S195



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SN54195, SN74195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54195	-55°C to 125°C
SN74195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54195			SN74195			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}			-800			-800			μ A	
Low-level output current, I_{OL}			16			16			mA	
Clock frequency, f_{clock}			0	30		0	30		MHz	
Width of clock input pulse, $t_{w(clock)}$			16			16			ns	
Width of clear input pulse, $t_{w(clear)}$			12			12			ns	
Setup time, t_{su} (see Figure 1)	Shift/load		25			25			ns	
	Serial and parallel data		20			20				
	Clear inactive-state		25			25				
Shift/load release time, $t_{release}$ (see Figure 1)			10			10			ns	
Serial and parallel data hold time, t_H (see Figure 1)			0			0			ns	
Operating free-air temperature, T_A			-55			125		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54195	-20	-57	mA
		SN74195	-18	-57	
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		39	63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1	30	39		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	26	ns

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SN54LS195A, SN74LS195A

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS195A	-55°C to 125°C
SN74LS195A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS195A			SN74LS195A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}		-400			-400			μA
Low-level output current, I _{OL}		4			8			mA
Clock frequency, f _{clock}		0	30		0	30		MHz
Width of clock or clear pulse, t _w (clock)		16			16			ns
Width of clear input pulse, t _w (clear)		12			12			ns
Setup time, t _{su} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, t _{release} (see Figure 1)		10			20			ns
Serial and parallel data hold time, t _h (see Figure 1)		0			0			ns
Operating free-air temperature, T _A		-55 125			0 70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS195A			SN74LS195A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.7			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 μA	2.5	3.4		2.7	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA		0.25	0.4	0.25 0.4		V
		I _{OL} = 8 mA				0.35 0.5		
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS} Short-circuit output current §	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2		14	21		14	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figure 1	30	39		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	26	ns

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SN54S195, SN74S195

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S195	-55°C to 125°C
SN74S195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S195			SN74S195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-1			-1			mA
Low-level output current, I_{OL}		20			20			mA
Clock frequency, f_{clock}		0		70	0		70	MHz
Width of clock input pulse, $t_w(clock)$		7			7			ns
Width of clear input pulse, $t_w(clear)$		12			12			ns
Setup time, t_{su} (see Figure 1)	Shift/load	11			11			ns
	Serial and parallel data	5			5			
	Clear inactive-state	9			9			
Shift/load release time, $t_{release}$ (see Figure 1)		2			6			ns
Serial and parallel data hold time, t_h (see Figure 1)		3			3			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V _{IH}	High-level input voltage				2			V
V _{IL}	Low-level input voltage						0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA				-1.2	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V,	SN54S195	2.5	3.4		V
			I _{OH} = -1 mA	SN74S195	2.7	3.4		
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 20 mA				0.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 5.5 V				1	mA
I _{IH}	High-level input current	V _{CC} = MAX,	V _I = 2.7 V				50	µA
I _{IL}	Low-level input current	V _{CC} = MAX,	V _I = 0.5 V				-2	mA
I _{OS}	Short-circuit output current §	V _{CC} = MAX			-40		-100	mA
I _{CC}	Supply current	V _{CC} = MAX,	See Note 2	SN54S195	70	99		mA
				SN74S195	70	109		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}.$

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

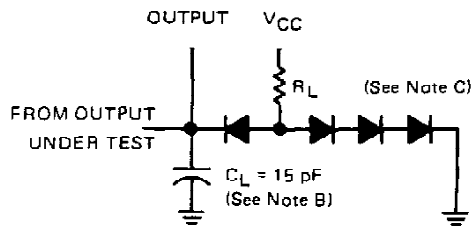
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF},$ $R_L = 280 \Omega,$ See Figure 1	70	105		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			11	16.5	ns

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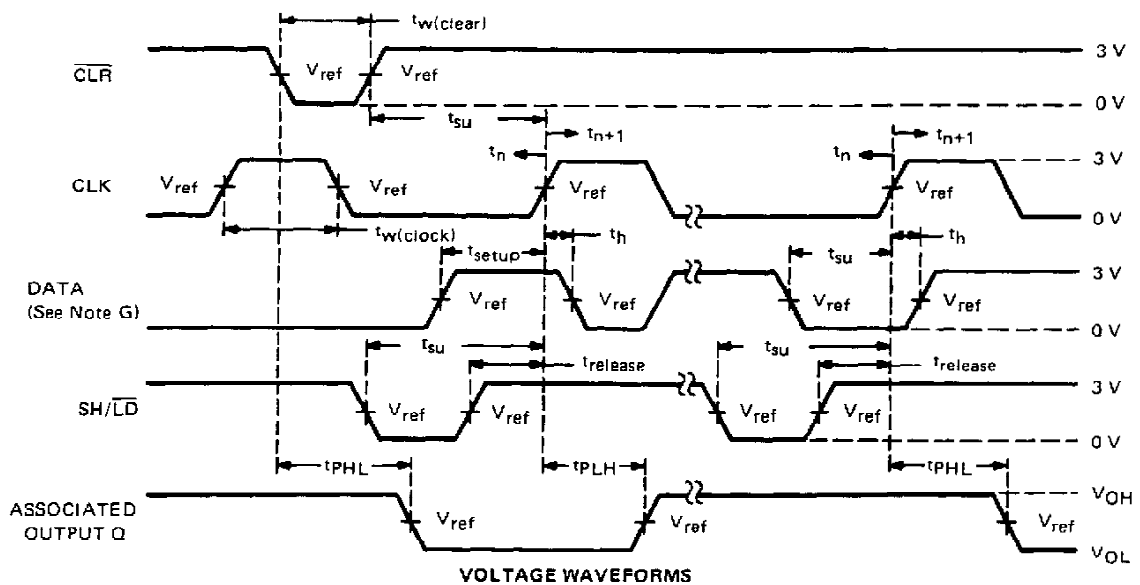
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**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



- NOTES: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and $PRR \leq 1 \text{ MHz}$. For '195, $t_r \leq 7 \text{ ns}$ and $t_f \leq 7 \text{ ns}$. For 'LS195A, $t_r \leq 15 \text{ ns}$ and $t_f \leq 6 \text{ ns}$. For 'S195, $t_r = 2.5 \text{ ns}$ and $t_f = 2.5 \text{ ns}$. When testing f_{max} , vary the clock PRR.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. A clear pulse is applied prior to each test.
- E. For '195 and 'S195, $V_{ref} = 1.5 \text{ V}$; for 'LS195A, $V_{ref} = 1.3 \text{ V}$.
- F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- G. J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
- H. t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/30602B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30602BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30602BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30602BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/30602BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54LS195AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS195AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54S195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS195AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS195AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS195ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS195ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS195AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS195AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS195AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS195AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS195AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS195AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S195D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74S195D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74S195N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S195N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S195N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S195N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54LS195AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS195AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS195AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS195AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS195AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS195AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54S195FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54S195FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54S195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54S195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54S195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SNJ54S195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

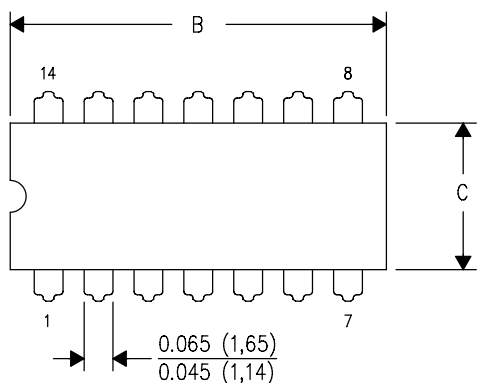
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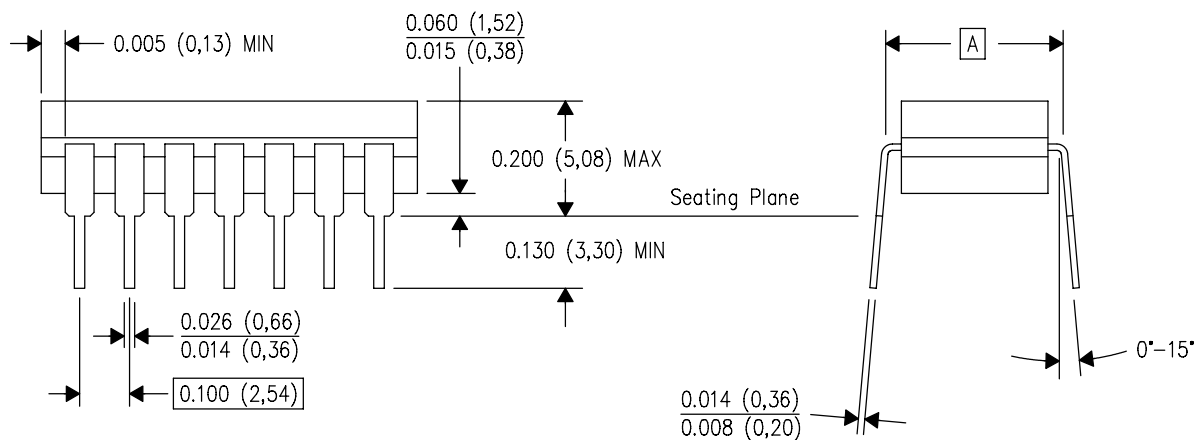
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

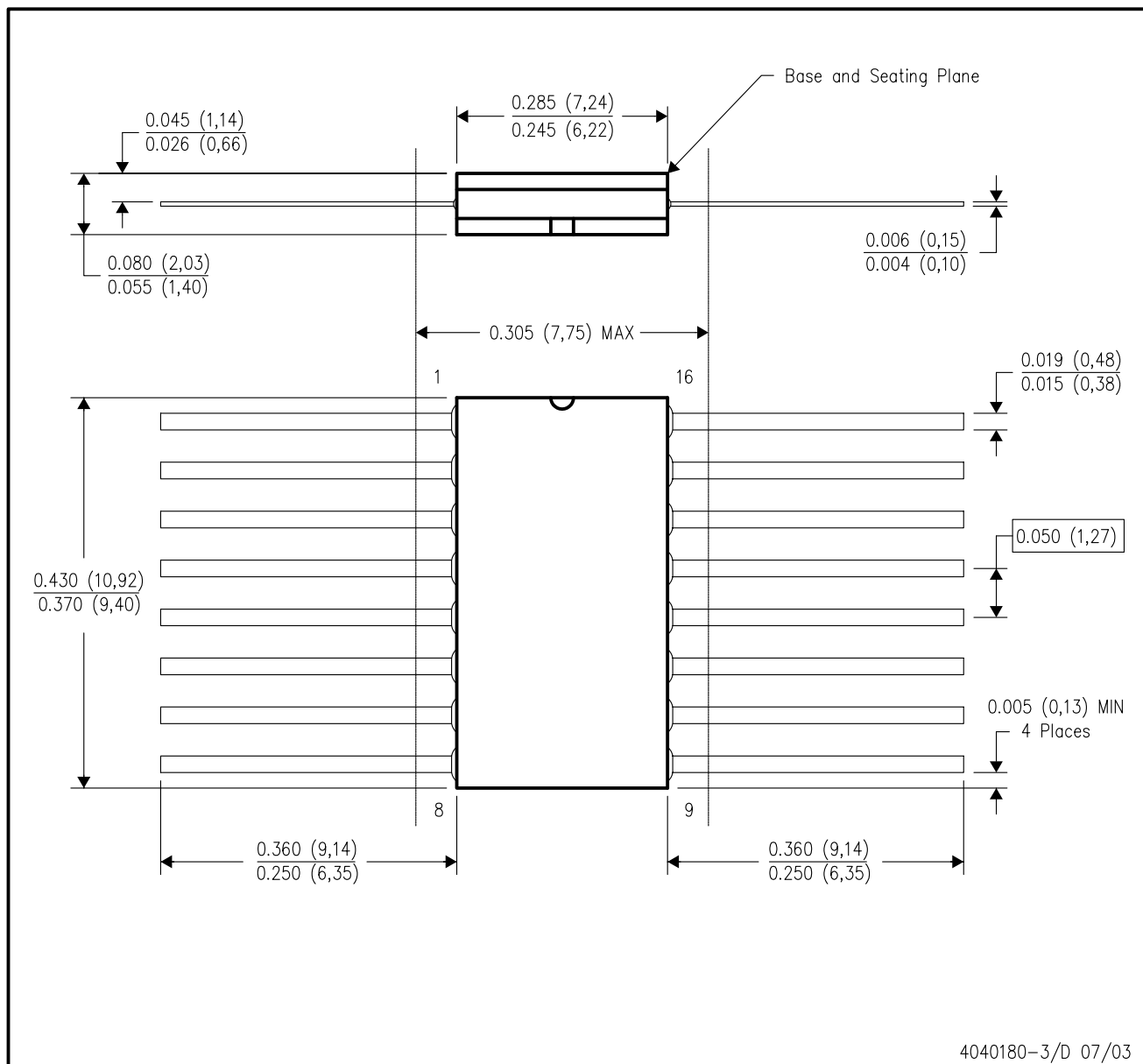


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

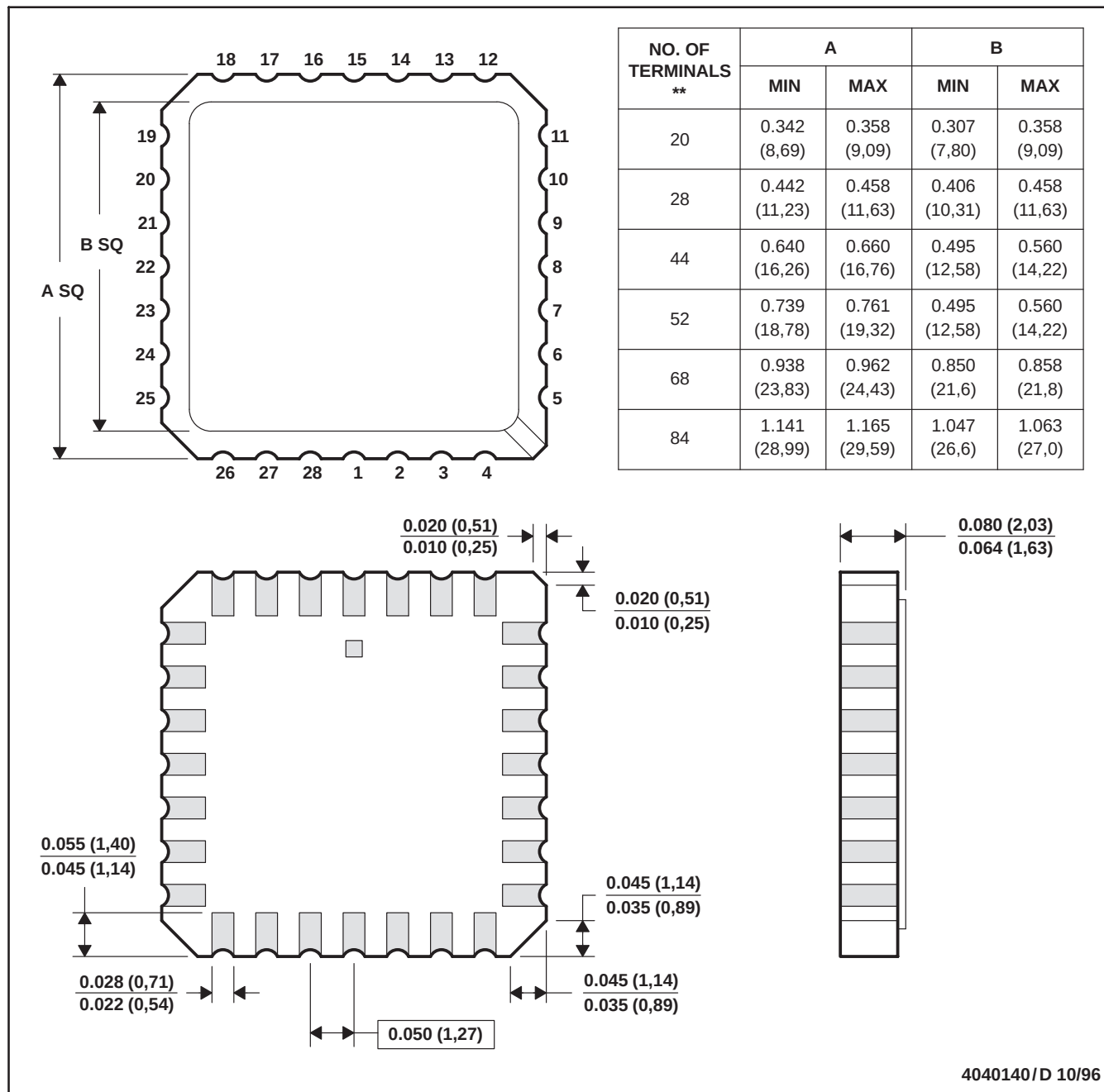


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

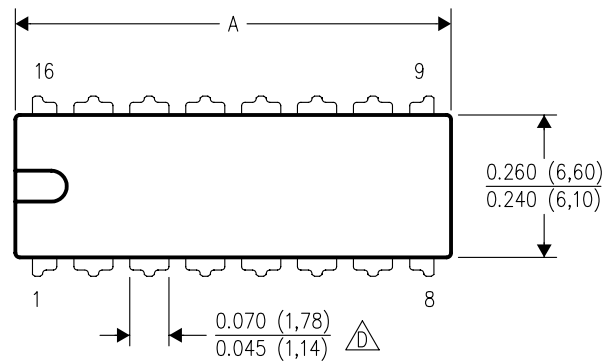


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

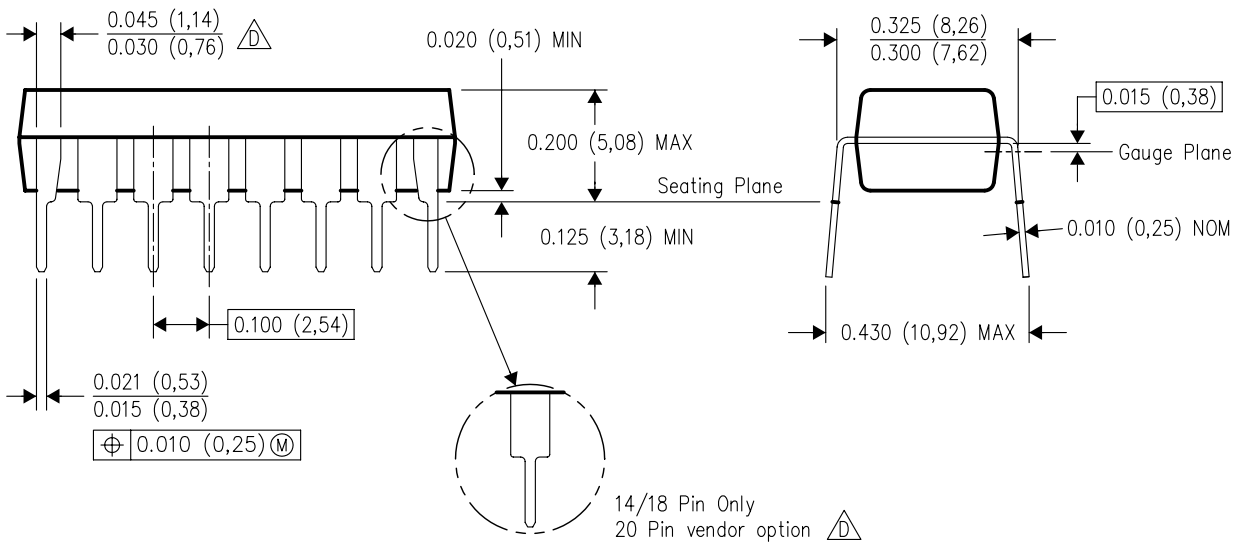
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



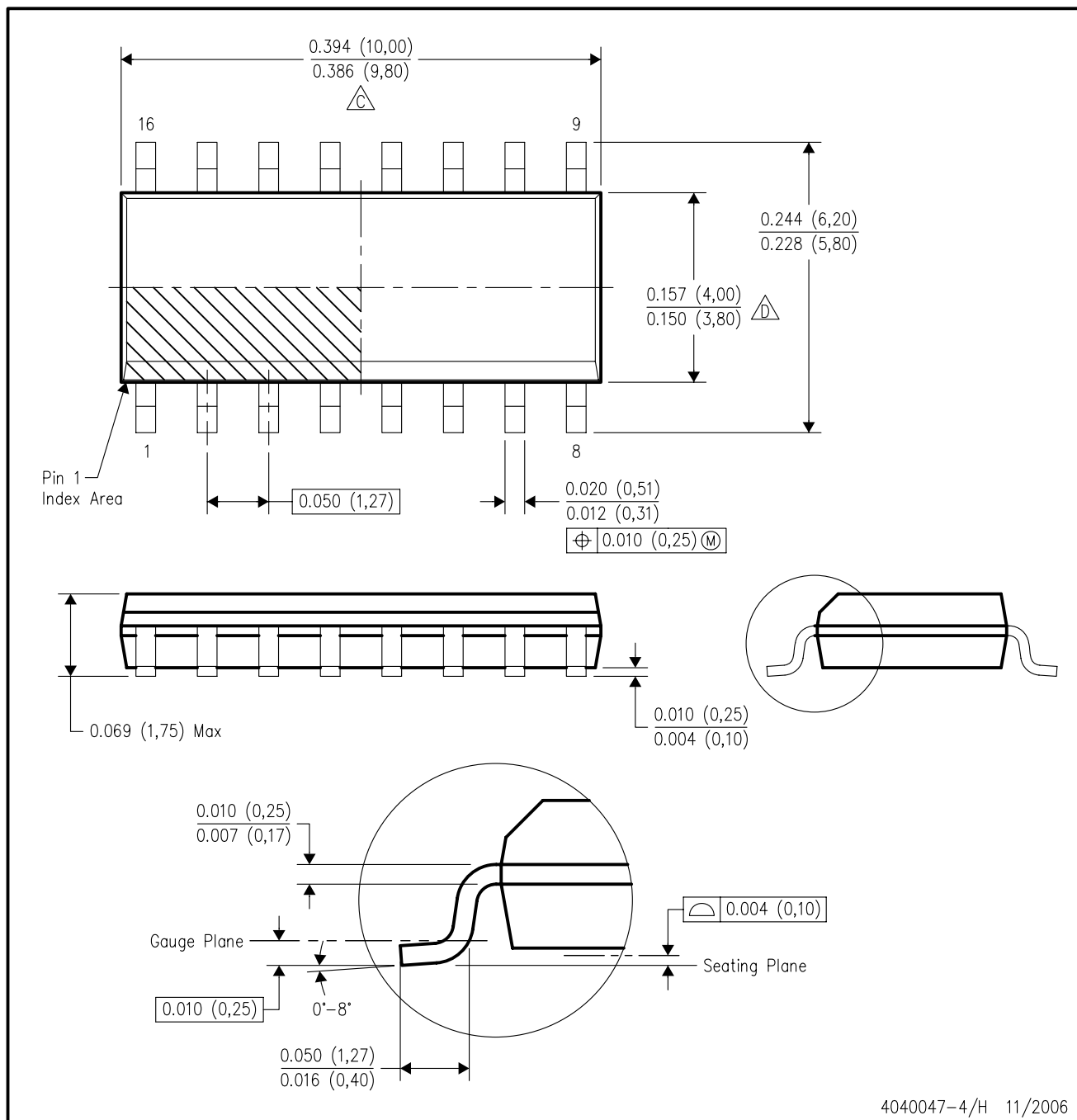
14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/30602B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30602BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30602BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30602BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/30602BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54LS195AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS195AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54S195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS195AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS195AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS195ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS195ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS195AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS195AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS195AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS195AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS195AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS195AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S195D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74S195D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74S195N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S195N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S195N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S195N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54LS195AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS195AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS195AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS195AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS195AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS195AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54S195FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54S195FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54S195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54S195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54S195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SNJ54S195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

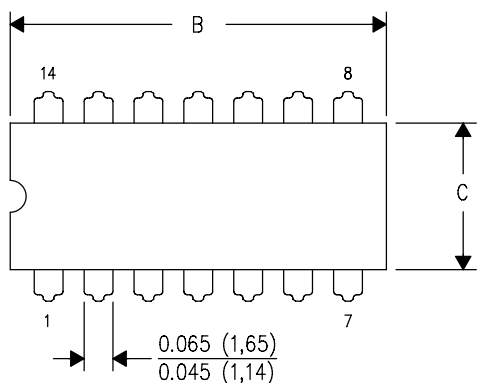
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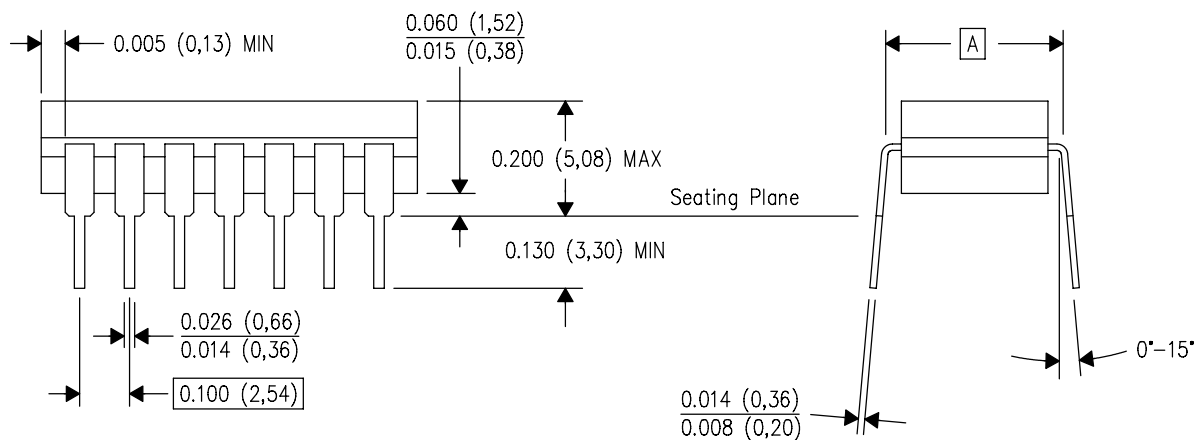
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

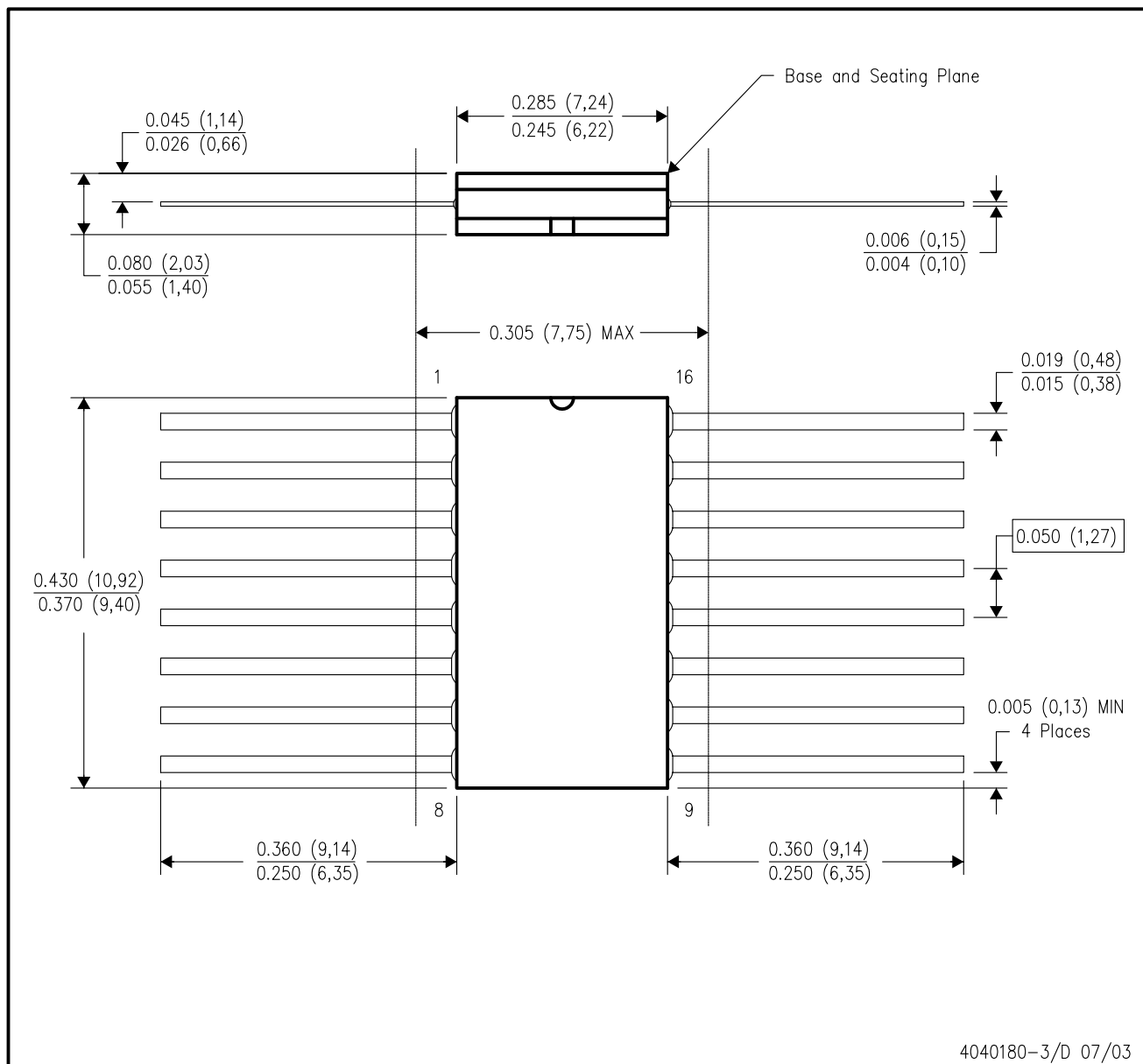


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

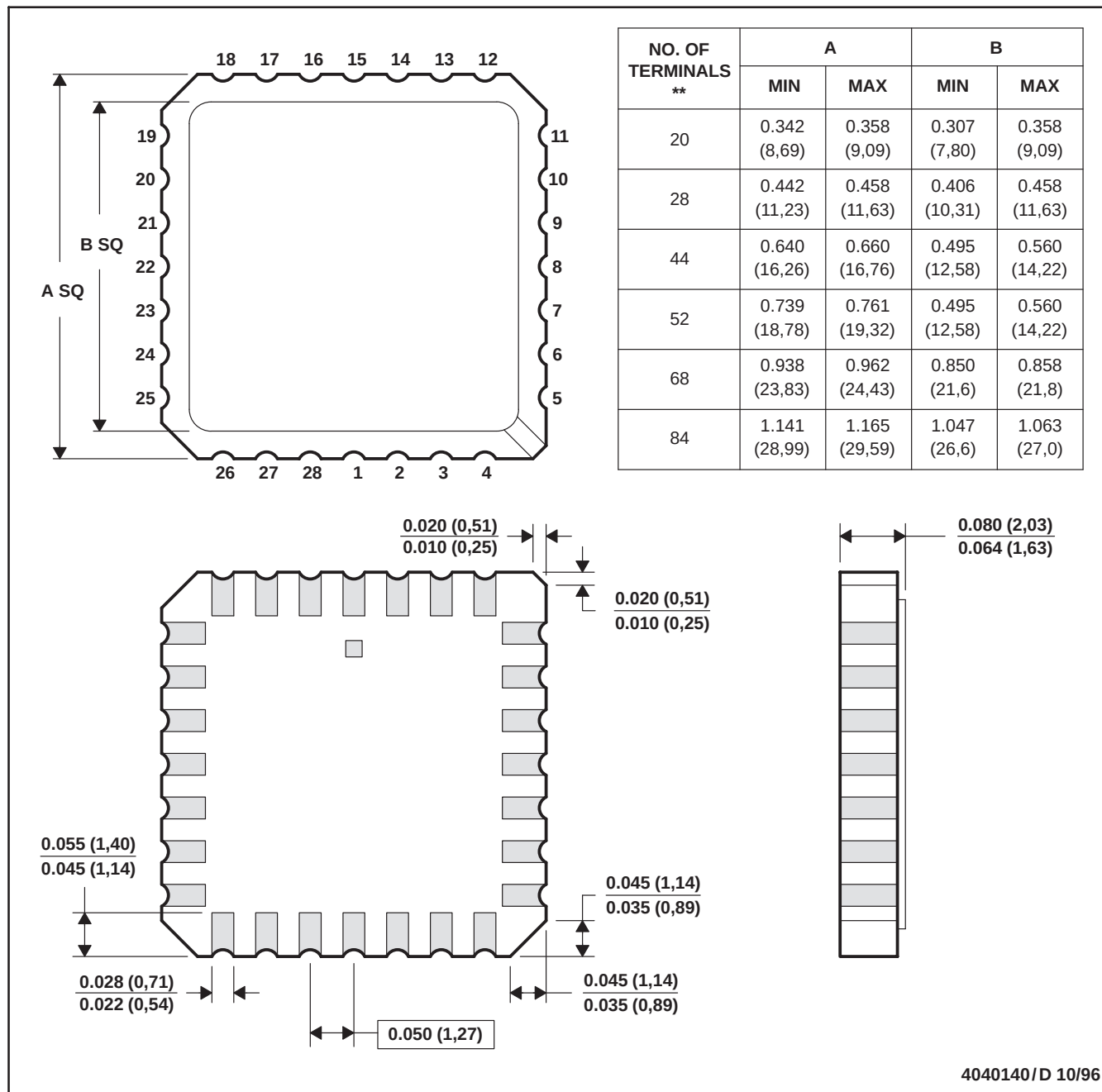


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

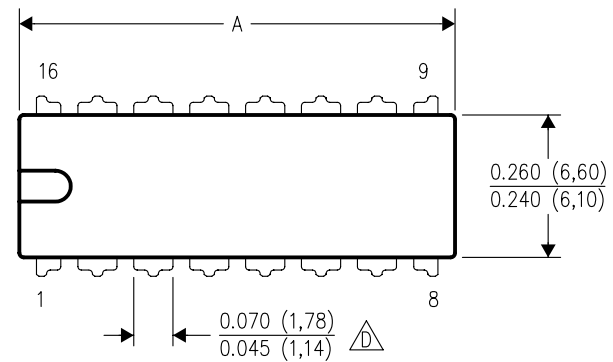


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

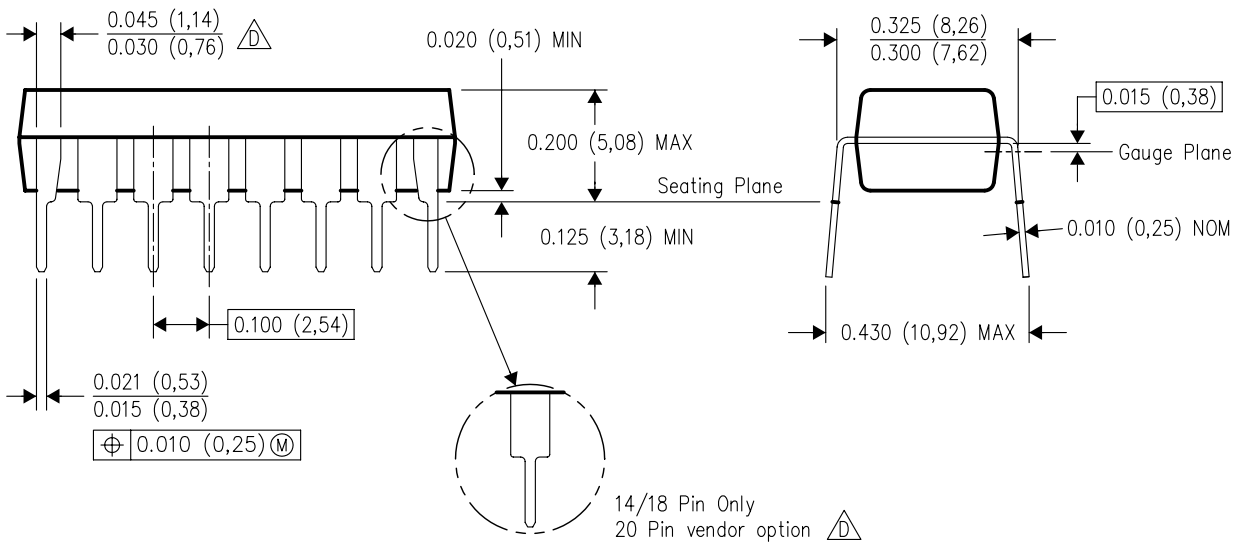
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



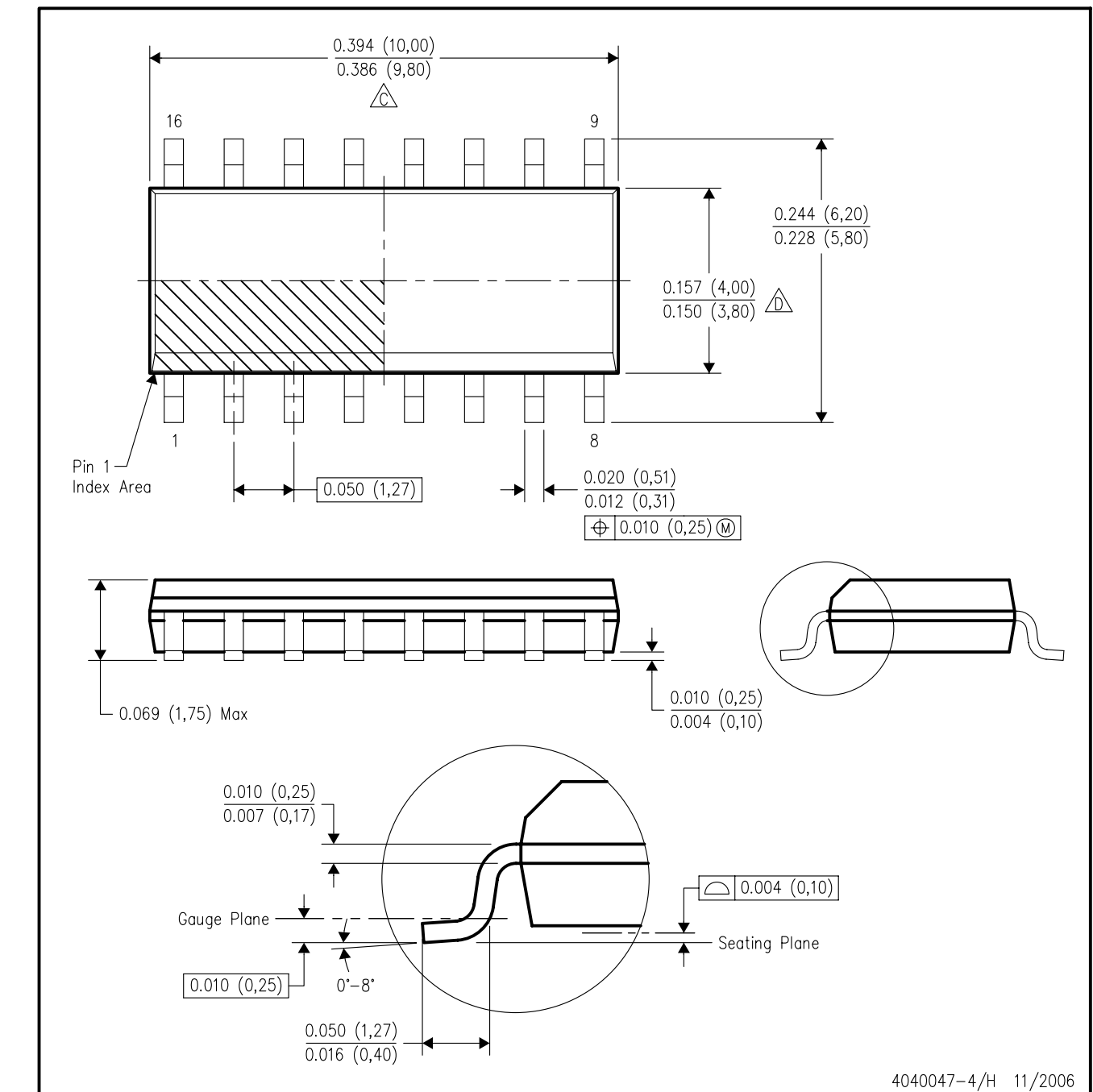
14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDS0-G16) PLASTIC SMALL-OUTLINE PACKAGE

D (R-PDS0-G16) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

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