HV7321

4-Ch. 5-Level ±80V High-Voltage Ultrasound Pulser with T/R Switches

Features

- Power Sequencing Free 5 Output Levels including RTZ (Return-to-Zero)
- -44 dB Single-Cycle Pulse-Inversion Second Harmonic Distortion (HD2) at 5 MHz
- Output Voltage up to ±80V
- ±2.5A Peak Output Current
- ±300 mA Current from V_{PP1}/V_{NN1} in CW Mode-0
- Integrated T/R Switch & RX Damper Switch
- Bleeder Switches Achieve True Zero during RTZ
- Supports Both Transparent and Re-Timing Mode
- Re-Timing Clock Frequency Supports up to 220 MHz
- Built-In Output Protection Diodes and Clamp Diodes
- +2.5/+3.3V Input Logic
- Built-In CW Switches to Pair with External CW Transmitters (CW Mode-1)
- 9 mm x 9 mm 64-Lead VQFN Package

Applications

- Medical Ultrasound Imaging Systems
- NDT Ultrasound
- Piezoelectric or Capacitive Transducer Drivers

General Description

The HV7321 is a 4-channel, 5-level, ultrasound transmitter with built-in T/R switches, output protection diodes and clamp diodes. The HV7321 can provide up to ±2.5A and the output voltage swing can be up to ±80V. The HV7321 supports both Transparent and Re-Timing mode. The re-timing clock frequency can support up to 220 MHz. The re-timing feature helps reduce the output jitter introduced by the driving the field-programmable gate array (FPGA).

The HV7321 has two different modes for CW transmission, CW-Mode 0 and CW-Mode 1.

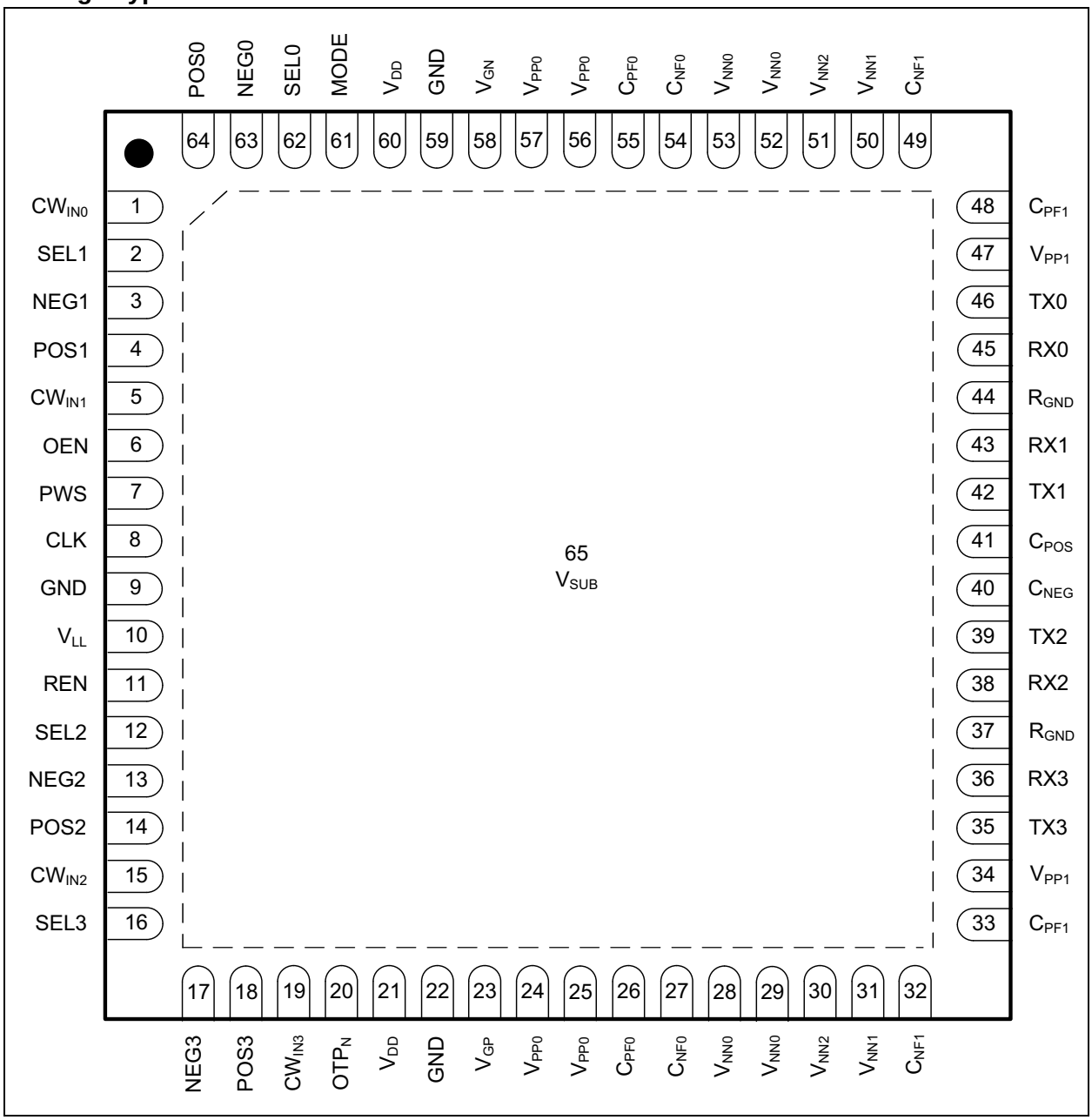
In CW-Mode 0 (Mode = 0, PWS = 0), the V_{PP1} and V_{NN1} rails are used for CW transmission. The output current is reduced in CW Mode-0.

In CW-Mode 1, the HV7321 accepts the output of an external CW beamformer as CW source.

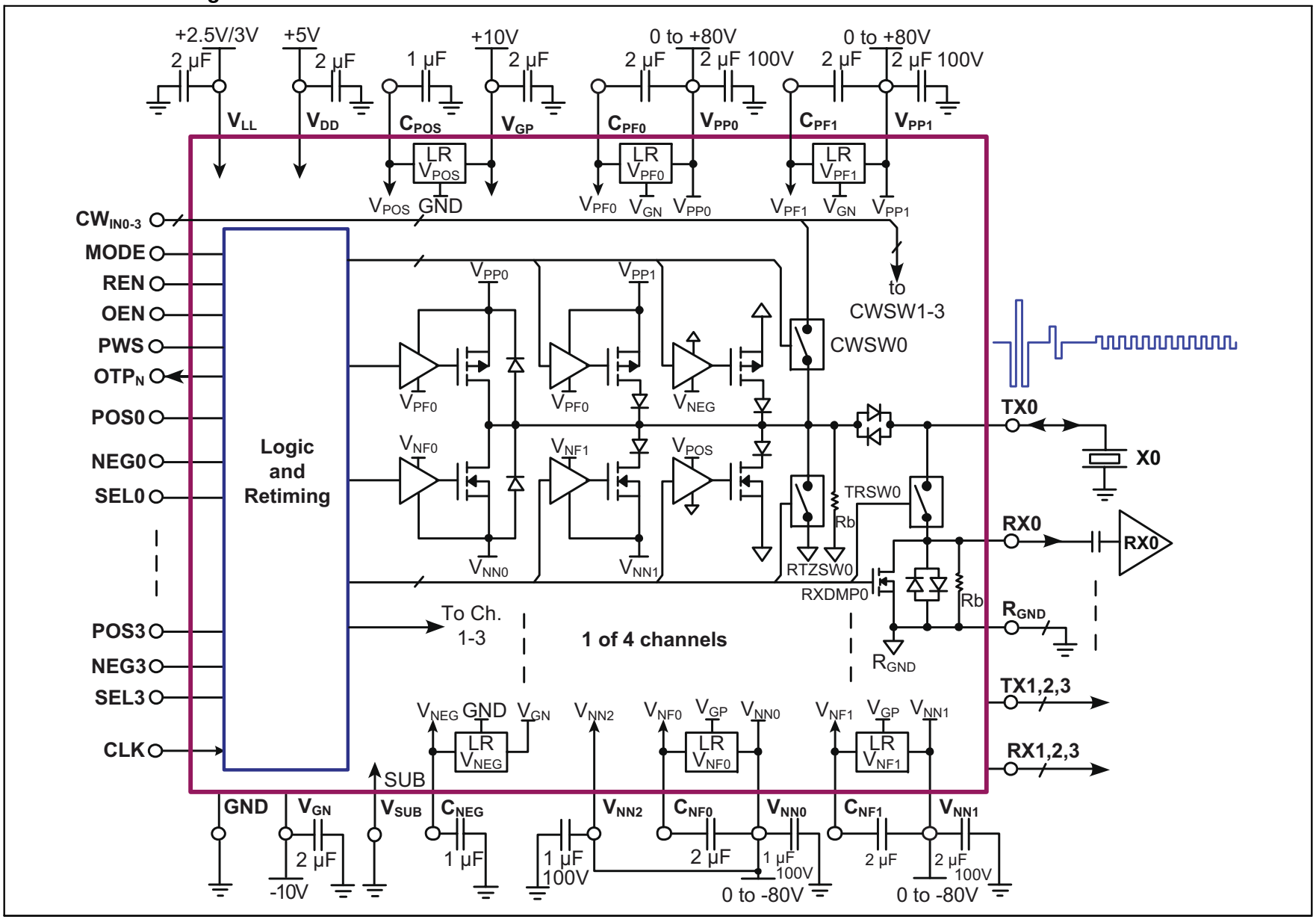
The HV7321 is LVCMOS 2.5V/3.3V input compatible, which can be interfaced with the FPGA directly.

The HV7321 is available in a 9 mm x 9 mm 64-Lead VQFN package.

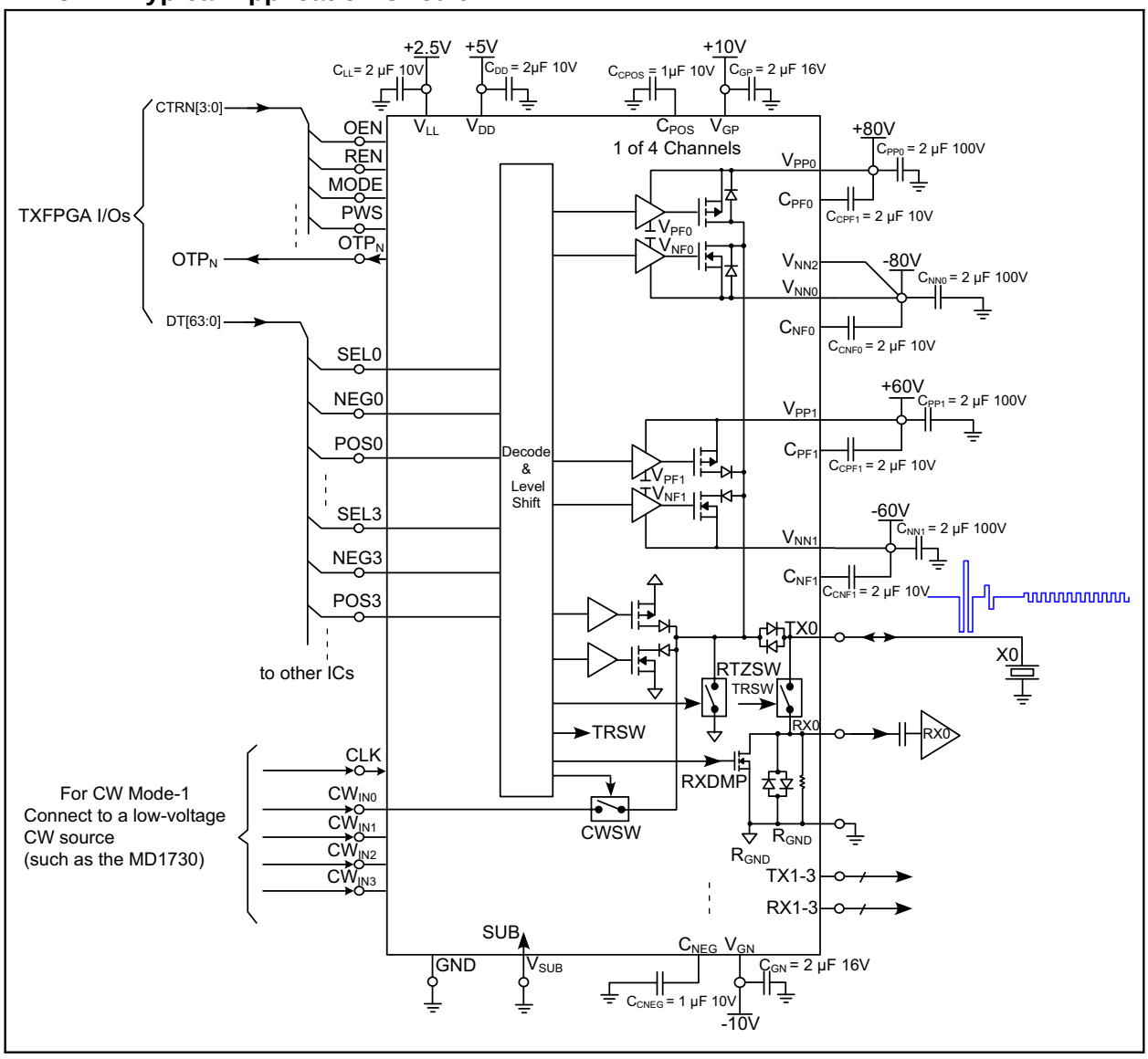
Package Types



HV7321 – Block Diagram



HV7321 – Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Positive logic supply (V_{LL}) ..... -0.5V to +5.5V
All I/O & CLK pin voltage (V_{IO}) ..... -0.5V to +5.5V
Positive voltage supply (V_{DD}) ..... -0.5V to +5.5V
Positive gate driver supply (V_{GP}) ..... -0.5V to +13.5V
Negative gate driver supply (V_{GN}) ..... -13.5V to +0.5V
High voltage positive supply ($V_{PP0,1}$) ..... -1.0V to +85V
High voltage negative supply ($V_{NN0,1,2}$) ..... -85V to +1.0V
CW input voltage (V_{CWIN}) ..... -7.5V to +7.5V
TX pin voltage (V_{TX}) ..... -85V to +85V
RX pin to GND voltage (V_{RX}) ..... ±0.7 to ±1.4V
Operating temperature ..... 0°C to +85°C
Storage temperature ..... -55°C to +150°C
Maximum junction temperature ..... +130°C
Maximum not-latch-up current ..... +100 mA
ESD Rating CW_{IN},TX, V_{PP}, V_{NN} pins ..... ±500V
ESD Rating – all other pins ..... ±2kV

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical specifications: V_{LL} = +2.5V, V_{DD} = +5.0V, $V_{PP0,1}$ = +80V, $V_{NN0,1,2}$ = -80V, V_{GP} = +10V, V_{GN} = -10V, V_{SUB} = 0V, PWS = OEN = REN = 1, T_A = 25°C, unless otherwise specified. Parameters in **Bold** apply over the operating temperature range of **T_A = T_J = 0 to +85°C.**

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Operating Supply Voltages						
Positive Logic Supply	V_{LL}	**2.25**	2.50	**3.60**	V	**Note 1**
Positive Voltage Supply	V_{DD}	**4.75**	5.0	**5.25**	V	**Note 1**
Positive Gate Driver Supply	V_{GP}	**8.0**	10	**12**	V	**Note 1** See Table 3-1.
Negative Gate Driver Supply	V_{GN}	**-12**	-10	**-8.0**		
High Voltage Positive Supply	V_{PP0}	**0**	—	**80**	V	**Note 1** Must be $V_{PP0} \geq V_{PP1}$
	V_{PP1}	**0**	—	**80**		
High Voltage Negative Supply	V_{NN0}	**-80**	—	**0**	V	**Note 1** Must be $V_{NN0} \leq V_{NN1}$
	V_{NN1}	**-80**	—	**0**		
Operating Supply Current						
V_{LL} Quiescent Current	I_{LLQ}	—	0.06	0.7	µA	OEN = REN = 0
V_{DD} Quiescent Current	I_{DDQ}	—	30	80	µA	
V_{PP0} Quiescent Current	I_{PP0Q}	—	0.37	6	µA	
V_{NN0} Quiescent Current	I_{NN0Q}	-9	-0.78	—	µA	
V_{PP1} Quiescent Current	I_{PP1Q}	—	0.44	10	µA	
V_{NN1} Quiescent Current	I_{NN1Q}	-10	-1.46	—	µA	
V_{NN2} Quiescent Current	I_{NN2Q}	-7	-3.84	—	µA	

Note 1: Characterized only; not 100% tested in production.
2: Design guidance only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical specifications: V_{LL} = +2.5V, V_{DD} = +5.0V, $V_{PP0,1}$ = +80V, $V_{NN0,1,2}$ = -80V, V_{GP} = +10V, V_{GN} = -10V, V_{SUB} = 0V, PWS = OEN = REN = 1, T_A = 25°C, unless otherwise specified. Parameters in **Bold** apply over the operating temperature range of **T_A = T_J = 0 to +85°C.**

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Current	I_{DDEN}	—	0.9	1.0	mA	f = 0 MHz f_{CLK} = 0 MHz MODE = 0 or 1
V_{PP0} Current	I_{PP0EN}	—	0.1	0.13	mA	
V_{NN0} Current	I_{NN0EN}	-0.12	-0.1	—	mA	
V_{PP1} Current	I_{PP1EN}	—	0.1	0.13	mA	
V_{NN1} Current	I_{NN1EN}	-0.12	-0.1	—	mA	
V_{NN2} Current	I_{NN2EN}	-0.05	-0.03	—	mA	
V_{LL} Current with Re-Timing	I_{LLRT}	—	0.11	0.3	mA	f_{CLK} = 80 MHz TX one-channel output, no load, continuous, **Note 1**
V_{DD} Current with Re-Timing	I_{DDRT}	—	7.08	8	mA	
V_{LL} Max. Current of SEL = 0/1	I_{LL5}	—	23	40	µA	CLK = 0 PWS = 1 MODE = 0 I_{PP05}/I_{NN05} and I_{PP15}/I_{NN15} are calculated using TX one channel output continuous, no load, at 5 MHz.
V_{DD} Max. Current of SEL = 0/1	I_{DD5}	—	1.5	1.7	mA	
V_{GP} Max. Current of SEL = 0/1	I_{GP5}	—	2.6	4	mA	
V_{GN} Max. Current of SEL = 0/1	I_{GN5}	-14	-9	—	mA	
V_{PP0} Current of SEL = 0 (1)	I_{PP05}	—	136	146	mA	
V_{NN0} Current of SEL = 0 (1)	I_{NN05}	-132	-125	—	mA	
V_{PP1} Current of SEL = 1 (1)	I_{PP15}	—	148	158	mA	
V_{NN1} Current of SEL = 1 (1)	I_{NN15}	-150	-143	—	mA	
V_{GP} Current of SEL = 1	I_{GPCW}	—	1.0	2.0	mA	TX one-channel output 5 MHz, continuous, no load V_{PP1}/V_{NN1} = ±5V PWS = MODE = 0 CW Mode-0, **Note 1**
V_{GN} Current of SEL = 1	I_{GNCW}	-8.0	-5.0	—	mA	
V_{PP1} Current of SEL = 1	I_{PP1CW}	—	17	26	mA	
V_{NN1} Current of SEL = 1	I_{NN1CW}	-20	-15	—	mA	
CWSW High-Voltage Analog Switch						
CW Switch Input Voltage	$V_{CWIN0–3}$	-7.0	—	+7.0	V	
CWSW Analog Switch On-Resistance (1)	R_{CWSW}	—	26.5	35	Ω	I_{CWSW} = ±100 mA
TRSW Off Withstand Voltage	V_{CWSW}	-80	—	+80	V	I_{SW} = ±1.0 µA
CWSW Off Capacitance to GND	C_{CWSW}	—	5.0	—	pF	MODE = 1, 1 MHz, 0 dBm, DC 0V, **Note 1**
CWSW On Capacitance to GND		—	60	—		
CWSW Switching On Time	t_{CWSW}	—	800	1100	ns	50% MODE rise to CWSW on/off **Note 1**
CWSW Switching Off Time		—	66	90		
TX Output P-Channel MOSFET on V_{PP0}						
On-Resistance	R_{ON_P0}	—	8.5	19	Ω	I_{SD} = 100 mA
Peak Output Current	I_{OUT_P0}	1	1.5	—	A	V_{PP0} = +25V, R_L = 1.0Ω to GND **Note 1**
		2.0	2.8	—	A	V_{PP0} = +80V, R_L = 1.0Ω to GND **Note 1**

Note 1: Characterized only; not 100% tested in production.

2: Design guidance only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical specifications: V_{LL} = +2.5V, V_{DD} = +5.0V, $V_{PP0,1}$ = +80V, $V_{NN0,1,2}$ = -80V, V_{GP} = +10V, V_{GN} = -10V, V_{SUB} = 0V, PWS = OEN = REN = 1, T_A = 25°C, unless otherwise specified. Parameters in **Bold** apply over the operating temperature range of **$T_A = T_J$ = 0 to +85°C.**

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TX Output P-Channel MOSFET on V_{PP1}						
On-Resistance at PWS = 1	R_{ON_P1}	—	16	21	Ω	I_{SD} = 100 mA
On-Resistance at PWS = 0		—	33	43		
Peak Output Current at PWS = 1 (1)	I_{OUT_P1}	0.8	1.0	—	A	$V_{PP0,1}$ = +25V, R_L = 1.0Ω to GND
		1.5	1.75	—		$V_{PP0,1}$= +80V, R_L = 1.0Ω to GND
Peak Output Current at PWS = 0 (1)		0.4	0.5	—		$V_{PP0,1}$ = +25V, R_L = 1.0Ω to GND
		0.8	0.95	—		$V_{PP0,1}$ = +80V, R_L = 1.0Ω to GND
TX Output N-Channel MOSFET on V_{NN0}						
On-Resistance	R_{ON_N0}	—	8	10	Ω	I_{SD} = 100 mA
Peak Output Current (1)	I_{OUT_N0}	-1.4	-1.7	—	A	V_{NN0} = -25V, R_L = 1.0Ω to GND
		-2.0	-2.3	—	A	V_{NN0} = -80V, R_L = 1.0Ω to GND
TX Output N-Channel MOSFET on V_{NN1}						
On-Resistance at PWS = 1	R_{ON_N1}	—	11	13	Ω	I_{SD} = 100 mA
On-Resistance at PWS = 0		—	36	45		
Peak Output Current at PWS = 1 (1)	I_{OUT_N1}	—	-1.2	-1.0	A	$V_{NN0,1}$ = -25V, R_L = 1.0Ω to GND
		—	-1.6	-1.3		$V_{NN0,1}$ = -80V, R_L = 1.0Ω to GND
Peak Output Current at PWS = 0 (1)		—	-0.4	-0.3		$V_{NN0,1}$ = -25V, R_L = 1.0Ω to GND
		—	-0.55	-0.4		$V_{NN0,1}$= -80V, R_L = 1.0Ω to GND
TX Damping P-Channel MOSFET on GND						
On-Resistance	R_{ON_PDMP}	—	7.0	16	Ω	I_{SD} = 100 mA
Peak Output Current (1)	I_{OUT_PDMP}	2.3	2.7	—	A	R_L = 1.0Ω from -25V to TX
		2.3	2.8	—	A	R_L = 1.0Ω from -80V to TX
TX Damping N-Channel MOSFET on GND						
On-Resistance	R_{ON_NDMP}	—	7.0	16	Ω	I_{SD} = 100 mA
Peak Output Current (1)	I_{OUT_NDMP}	—	-2.0	-1.8	A	R_L = 1.0Ω from +25V to TX
		—	-2.3	-2.0	A	R_L = 1.0Ω from +80V to TX
RTZSW Auto Bleed High-Voltage Analog Switch						
RTZSW On-Resistance (1)	R_{RTZSW}	—	238	270	Ω	I_{SD} = ±1.0 mA
RTZSW Off Withstand Voltage (1)	V_{RTZSW}	-80	—	+80	V	I_{SW} = ±100 µA
TX OUTPUT Isolation Diodes and Bleed Resistor						
Diode Forward Voltage	V_F	—	0.96	1.9	V	I_{FM} = 300 mA, **Note 1**
Forward Continuous Current	I_{FM}	—	300	—	mA	**Note 2**
Peak Forward Pulse Current	I_{FSM}	—	3.0	—	A	PW = 50 ns, **Note 2**
Total Capacitance of 2-diode	C_T	—	3.5	—	pF	at 1 MHz, 1 dBm, 0V DC, **Note 2**
TX/RX Bleed Resistor to GND	R_b	11	15	20	kΩ	**Note 1**

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2: Design guidance only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical specifications: V_{LL} = +2.5V, V_{DD} = +5.0V, $V_{PP0,1}$ = +80V, $V_{NN0,1,2}$ = -80V, V_{GP} = +10V, V_{GN} = -10V, V_{SUB} = 0V, PWS = OEN = REN = 1, T_A = 25°C, unless otherwise specified. Parameters in **Bold** apply over the operating temperature range of **T_A = T_J = 0 to +85°C.**

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TRSW and RXDMP Switches						
TRSW Analog Switch On-Resistor	R_{TRSW}	—	18	22	Ω	I_{TRSW} = ±1.0 mA **Note 1**
TRSW Off Withstand Voltage	V_{TRSW}	-80	—	+80	V	I_{SW} = ±100 µA, **Note 1**
RX to GND Protection Diode	V_F	—	1.5	2.2	V	I_F = ±100 mA, **Note 1**
RXDMP Switch On-Resistance	R_{RXDMP}	—	17	21	Ω	I_{SD} = ±1.0 mA, **Note 1**
RX Pin to GND Capacitance	C_{RXG}	—	—	7.0	pF	1 MHz, 1 dBm, 0V DC, **Note 2**
Built-In Gate Drive Voltage Linear Regulators						
Output P-Channel Gate Drive Voltage Referenced to V_{PP0}	V_{PF0}	-5.2	-4.6	-3.8	V	V_{GN} - V_{PP0} < -10V
Output P-Channel Gate Drive Voltage Referenced to V_{PP1}	V_{PF1}	-5.2	-4.6	-3.8	V	V_{GN} - V_{PP1} < -10V
Output N-Channel Gate Drive Voltage Referenced to V_{NN0}	V_{NF0}	3.3	4.2	5.2	V	V_{GP} - V_{NN0} > 10V
Output N-Channel Gate Drive Voltage Referenced to V_{NN1}	V_{NF1}	3.3	4.2	5.2	V	V_{GP} - V_{NN1} > 10V
Output N-Channel Gate Drive Voltage Referenced to GND	V_{POS}	3.2	4.2	5.2	V	
Output P-Channel Gate Drive Voltage Referenced to GND	V_{NEG}	-5.2	-4.5	-3.8	V	
Dropout Voltage of (V_{PP0} - V_{GN})	V_{DOPF0}	-2.9	-2.6	-2.4	V	
Dropout Voltage of (V_{PP1} - V_{GN})	V_{DOPF1}	-2.9	-2.6	-2.4	V	
Dropout Voltage of (V_{GP} - V_{NN0})	V_{DONF0}	3.0	3.3	3.6	V	
Dropout Voltage of (V_{GP} - V_{NN1})	V_{DONF1}	3.0	3.3	3.6	V	
Dropout Voltage of (V_{NEG} - V_{GN})	V_{DONEG}	2.9	3.3	3.5	V	
Dropout Voltage of (V_{GP} - V_{POS})	V_{DOPOS}	-2.8	-2.6	-2.4	V	
Logic & Clock Input Characteristics						
Input Logic Low Voltage	V_{IL}	0	—	0.2 V_{LL}	V	
Input Logic High Voltage	V_{IH}	0.8 V_{LL}	—	V_{LL}	V	
Input Logic Low Current	I_{IL}	-1.0	—	—	µA	**Note 1**
Input Logic High Current	I_{IH}	—	—	1.0	µA	**Note 1**
Input Capacitance	C_{IN}	—	2.0	3.0	pF	**Note 2**
OEN Switching On Time	t_{OEN}	—	200	—	µs	50% OEN rise to TX ready, **Note 2**
OEN Switching Off Time		—	20	—	ns	50% OEN fall to TX all output FETs on HV rails are off, **Note 1**
Thermal protection OTP_N & UVLO						
OTP_N Output Max. Pull-Up	V_{OH}	—	—	5.25	V	
OTP_N Output Low Max. Voltage	V_{OL}	—	—	0.1	V	at 100 µA
		—	—	0.4	V	at 4.0 mA
OTP_N Output High Current	I_{OFF}	—	—	15	µA	25°C, at 5.25V pull-up, **Note 1**

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2: Design guidance only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical specifications: V_{LL} = +2.5V, V_{DD} = +5.0V, $V_{PP0,1}$ = +80V, $V_{NN0,1,2}$ = -80V, V_{GP} = +10V, V_{GN} = -10V, V_{SUB} = 0V, PWS = OEN = REN = 1, T_A = 25°C, unless otherwise specified. Parameters in **Bold** apply over the operating temperature range of **$T_A = T_J$ = 0 to +85°C.**

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Thermal Shutdown Trip Point	T_{TRIP}	125	138	160	°C	OTP_N = LO when thermal shut-down occurs, **Note 1**
Thermal Shutdown Hysteresis	T_{HYS}	—	38	—	°C	
V_{DD} OK On Voltage	V_{DDUVON}	3.45	3.7	4.05	V	**Note 1**
V_{DD} UVLO Trip Voltage	$V_{DDUVOFF}$	3.05	3.4	3.85		
V_{LL} OK On Voltage	V_{LLUVON}	1.59	1.7	1.81		
V_{LL} UVLO Trip Voltage	$V_{LLUVOFF}$	1.39	1.6	1.71		
TX Output HD2 & Timing Characteristics						
Second Harmonic Distortion	HD2	—	-44	-40	dB	V_{PP0}/V_{NN0} = ±70V launched in 100 µs apart, with load of 220 pF//1k (Second Harmonic Distortion). HD2, single-cycle inverting 5.0 MHz **Note 1**
Output Rise Time from 0V to V_{PP0}	t_{r1}	—	10	12	ns	
Output Fall Time from 0V to V_{NN0}	t_{f1}	—	10	12		
Output Rise Time from V_{NN0} to V_{PP0}	t_{r2}	—	17	19		
Output Fall Time from V_{PP0} to V_{NN0}	t_{f2}	—	17	19		
Output Rise Time from V_{NN0} to 0V	t_{r3}	—	10	13.5		
Output Fall Time from V_{PP0} to 0V	t_{f3}	—	10	13.5		
Propagation Delay Rise Time 1	t_{dr1}	—	16	18	ns	All these tr,tf,td values, at $V_{PP0,1}/V_{NN0,1}$ = ±70V, 220 pF//1k **Note 1**
Propagation Delay Fall Time 1	t_{df1}	—	16	18		
Propagation Delay Rise Time 2	t_{dr2}	—	17.5	19		
Propagation Delay Fall Time 2	t_{df2}	—	17.5	19		
Propagation Delay Rise Time 3	t_{dr3}	—	14	16		
Propagation Delay Fall Time 3	t_{df3}	—	14	16		
Output Rise Time from 0V to V_{PP1}	t_{r4}	—	15	17	ns	All these tr,tf,td values at $V_{PP0,1}/V_{NN0,1}$ = ±70V, 220 pF//1k **Note 1**
Output Fall Time from 0V to V_{NN1}	t_{f4}	—	15	17		
Output Rise Time from V_{NN1} to V_{PP1}	t_{r5}	—	24	27		
Output Fall Time from V_{PP1} to V_{NN1}	t_{f5}	—	24	27		
Output Rise Time from V_{NN1} to 0V	t_{r6}	—	10	13		
Output Fall Time from V_{PP1} to 0V	t_{f6}	—	10	13		
Propagation Delay Rise Time 4	t_{dr4}	—	15	17	ns	
Propagation Delay Fall Time 4	t_{df4}	—	15	17		
Propagation Delay Rise Time 5	t_{dr5}	—	16	18		
Propagation Delay Fall Time 5	t_{df5}	—	16	18		
Propagation Delay Rise Time 6	t_{dr6}	—	15	17		
Propagation Delay Fall Time 6	t_{df6}	—	15	17		
Delay Time Matching with SEL = L	Δt_{d1}	—	1.5	2.0	ns	P to N, ch.-to-ch. matching in IC, typ. at $V_{PP0,1}/V_{NN0,1,2}$ = ±70V, 220 pF//1k, **Note 1**
Delay Time Matching with SEL = H	Δt_{d2}	—	1.5	2.0	ns	

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical specifications: V_{LL} = +2.5V, V_{DD} = +5.0V, $V_{PP0,1}$ = +80V, $V_{NN0,1,2}$ = -80V, V_{GP} = +10V, V_{GN} = -10V, V_{SUB} = 0V, PWS = OEN = REN = 1, T_A = 25°C, unless otherwise specified. Parameters in **Bold** apply over the operating temperature range of **$T_A = T_J$ = 0 to +85°C.**

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TRSW Switch On Delay Time	t_{TRSW}	130	180	230	ns	From POS = 0 & NEG = 0, **Note 1**
TRSW Switch Off Delay Time		8	12	16	ns	From POS = 1 or NEG = 1, **Note 1**
RTZSW Switch On Delay Time	t_{RTZSW}	130	180	240	ns	From POS = 0 & NEG = 0, **Note 1**
RTZSW Switch Off Delay Time		11	21	31	ns	From POS = 1 or NEG = 1, **Note 1**
RXDMP Damp Switch On Delay Time	t_{RXDMP}	3	10	15	ns	From POS = 1 or NEG = 1, **Note 1**
RXDMP Damp Switch Off Delay Time		0.55	1.4	2.35	us	From POS = 0 & NEG = 0, **Note 1**
PWS = 0 to 1 Mode Change Time	t_{MC}	—	220	—	ns	**Note 2**
Output Max. Frequency Range	f_{OUT}	—	20	—	MHz	100Ω resistor load, **Note 2**
Re-Timing Clock Frequency	f_{CLK}	10	—	220	MHz	**Note 2**
Re-Timing Clock Rise & Fall Times	t_{RC},t_{FC}	—	0.5	5.0	ns	**Note 2**
Set-Up Time, POS/NEG to CLK	t_{su}	2.0	—	—	ns	**Note 2**
Hold Time, CLK to POS/NEG	t_H	1.0	—	—	ns	**Note 2**
Clock Time Low (2)	t_{CLK_LO}	2.0	—	100	ns	CLK input must be activated before POS and NEG inputs are high. CLK input must be deactivated after POS and NEG inputs are low.
Clock Time High (2)	t_{CLK_HI}	2.0	—	100		
Clock Recognition Time (1)	t_{CLK_REC}	—	2.0	—		
Clock Release Time (1)	t_{CLK_RLS}	150	330	500		

Note 1: Characterized only; not 100% tested in production.

2: Design guidance only.

TEMPERATURE CHARACTERISTICS

Unless otherwise indicated, all parameters apply with V_{LL} = +2.5V, V_{DD} = +5.0V, $V_{PP0,1}$ = +80V, $V_{NN0,1,2}$ = -80V, V_{GP} = +10V, V_{GN} = -10V, V_{SUB} = 0V, OEN = REN = 1

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_{OA}	0	—	+85	°C	
Storage Temperature Range	T_{ST}	-55	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+130	°C	
Total Power Dissipation	PD	—	3.0	—	W	
Thermal Package Resistances (64LD 9 mm x 9 mm VQFN)						
Junction-to-Ambient Thermal Resistance	θ_{JA}	—	16.3	—	°C/W	JEDEC (2S2P) 4L PCB 114.3 mm x 76.2 mm x1.6 mm T_A = 85°C
Junction-to-Board Thermal Resistance	θ_{JB}	—	2.55	—	°C/W	JEDEC (2S2P) 4L PCB 114.3 mm x 76.2 mm x1.6 mm T_A = 85°C
Junction-to-Case Top Thermal Resistance	θ_{JC}	—	0.2	—	°C/W	JEDEC (2S2P) 4L PCB 114.3 mm x 76.2 mm x1.6 mm T_A = 85°C

TABLE 1-1: INPUT OUTPUT LOGIC TRUTH TABLE (TRANSPARENT, CLK = 0)

Function	OTP_N	Logic Inputs							TX Output	RTZSW & TRSW	CWSW	RXDMP
		OEN	MODE	PWS	CLK	SEL	NEG	POS				
Pulsed-Echo Mode (1)	1	1	0	1	0	0	0	0	RTZ	OFF	OFF	ON
	1	1	0	1	0	0	0	1	V_{PP0}	OFF	OFF	ON
	1	1	0	1	0	0	1	0	V_{NN0}	OFF	OFF	ON
	1	1	0	1	0	0	1	1	RTZ+(4)	ON	OFF	OFF
	1	1	0	1	0	1	0	0	RTZ	OFF	OFF	ON
	1	1	0	1	0	1	0	1	V_{PP1}	OFF	OFF	ON
	1	1	0	1	0	1	1	0	V_{NN1}	OFF	OFF	ON
	1	1	0	1	0	1	1	1	high Z	OFF	OFF	ON
CW Mode-0 (2)	1	1	0	0	0	0	0	0	RTZ	OFF	OFF	ON
	1	1	0	0	0	0	0	1	V_{PP0}	OFF	OFF	ON
	1	1	0	0	0	0	1	0	V_{NN0}	OFF	OFF	ON
	1	1	0	0	0	0	1	1	RTZ+(4)	ON	OFF	OFF
	1	1	0	0	0	1	0	0	RTZ	OFF	OFF	ON
	1	1	0	0	0	1	0	1	V_{PP1}	OFF	OFF	ON
	1	1	0	0	0	1	1	0	V_{NN1}	OFF	OFF	ON
	1	1	0	0	0	1	1	1	high Z	OFF	OFF	ON
CW Mode-1 (3)	1	1	1	x	x	other than 011			high Z	OFF	ON	ON
						0	1	1	RTZ+(4)	ON	OFF	OFF
Device Disabled	x	0	x	x	x	x	x	x	high Z	OFF	OFF	ON
Thermal Protection Activated	0	x	x	x	x	x	x	x	high Z	OFF	OFF	ON

Note 1: In Pulsed-Echo mode, low duty cycle must be used due to the IC power dissipation limit.

2: When PWS = 0, V_{PP1}/V_{NN1} output current is reduced for low-voltage CW mode-0. V_{PP0}/V_{NN0} output current is unaffected when PWS = 1, as in Pulsed-Echo mode.

3: In CW MODE = 1, the CWSW is turned on to use external CW waveform at CW_{IN}, if the channel SEL = NEG = POS = 0.

4: When SEL = 0, NEG = 1, POS = 1, the channel is in Receiving mode (RTZ+).

TABLE 1-2: INPUT OUTPUT LOGIC TRUTH TABLE (WITH CLK RE-TIMING, CLK ≥ 10MHZ)

Function	OTP_N	Logic Inputs							TX Output	RTZSW & TRSW	CWSW	RXDMP
		OEN	MODE	PWS	CLK	SEL	NEG	POS				
Pulsed-Echo Mode (1)	1	1	0	1	↑	0	0	0	RTZ	OFF	OFF	ON
	1	1	0	1	↑	0	0	1	V_{PP0}	OFF	OFF	ON
	1	1	0	1	↑	0	1	0	V_{NN0}	OFF	OFF	ON
	1	1	0	1	↑	0	1	1	RTZ+(4)	ON	OFF	OFF
	1	1	0	1	↑	1	0	0	RTZ	OFF	OFF	ON
	1	1	0	1	↑	1	0	1	V_{PP1}	OFF	OFF	ON
	1	1	0	1	↑	1	1	0	V_{NN1}	OFF	OFF	ON
	1	1	0	1	↑	1	1	1	high Z	OFF	OFF	ON
CW Mode-0 (2)	1	1	0	0	↑	0	0	0	RTZ	OFF	OFF	ON
	1	1	0	0	↑	0	0	1	V_{PP0}	OFF	OFF	ON
	1	1	0	0	↑	0	1	0	V_{NN0}	OFF	OFF	ON
	1	1	0	0	↑	0	1	1	RTZ+(4)	ON	OFF	OFF
	1	1	0	0	↑	1	0	0	RTZ	OFF	OFF	ON
	1	1	0	0	↑	1	0	1	V_{PP1}	OFF	OFF	ON
	1	1	0	0	↑	1	1	0	V_{NN1}	OFF	OFF	ON
	1	1	0	0	↑	1	1	1	high Z	OFF	OFF	ON
CW Mode-1 (3)	1	1	1	x	x	other than 011			high Z	OFF	ON	ON
						0	1	1	RTZ+(4)	ON	OFF	OFF
Device Disabled	x	0	x	x	x	x	x	x	high Z	OFF	OFF	ON
Thermal Protection Activated	0	x	x	x	x	x	x	x	high Z	OFF	OFF	ON

Note 1: In Pulsed-Echo mode, low duty cycle must be used due to the IC power dissipation limit.

2: When PWS = 0, V_{PP1}/V_{NN1} output current is reduced for low-voltage CW mode-0. V_{PP0}/V_{NN0} output current is unaffected when PWS = 1, as in Pulsed-Echo mode.

3: In CW MODE = 1, the CWSW is turned on to use external CW waveform at CWIN, if the channel SEL = NEG = POS = 0.

4: When SEL = 0, NEG = 1, POS = 1, the channel is in Receiving mode (RTZ+).

1.1 TYPICAL TIMING DIAGRAMS

Figure 1-1 shows the timing of control inputs and RTZ, T/R and RXDMP switches per each channel of the HV7321.

Upon the completion of a receiving period, an RTZ period (SEL, NEG, POS = 000) should be asserted before transmitting again.

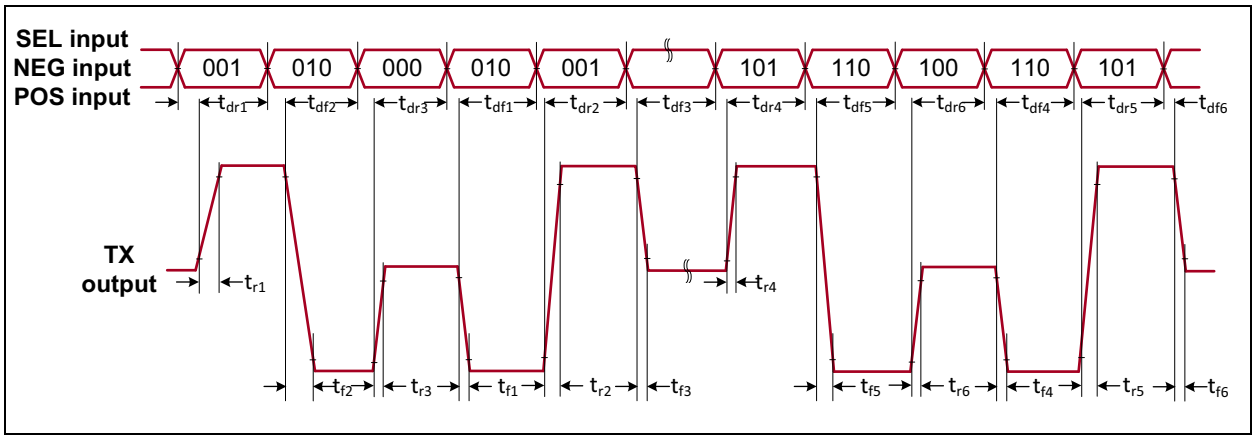


FIGURE 1-1: *Logic Input Timing Diagram.*

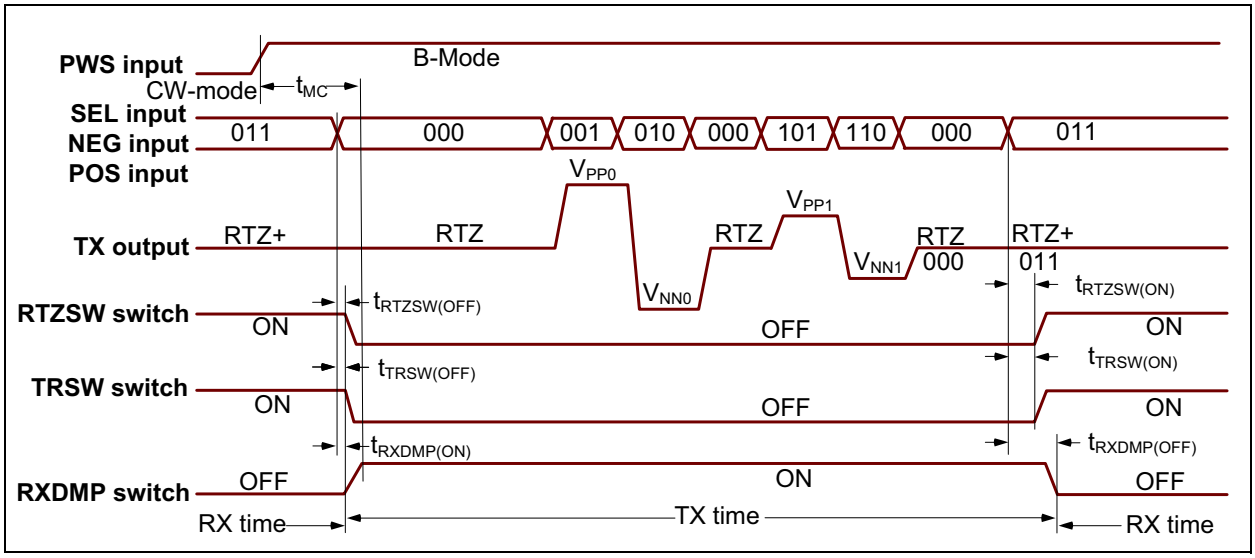


FIGURE 1-2: *TX Output Timing Diagram.*

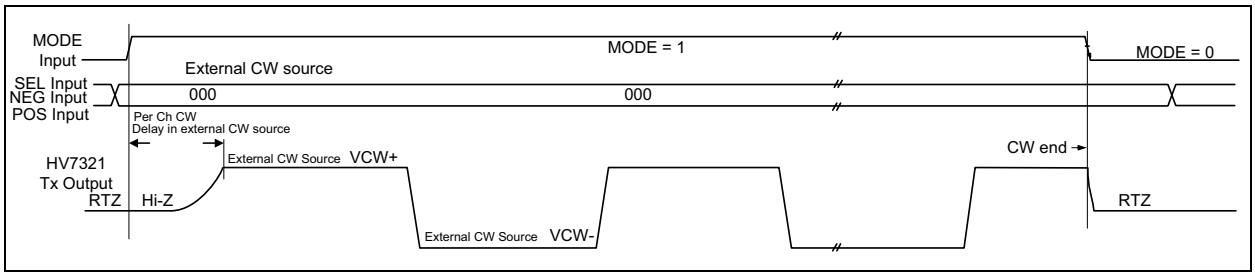


FIGURE 1-3: *Timing Diagram of HV7321 TX Output and Switches in CW Mode-1 Driven by External CW Source.*

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

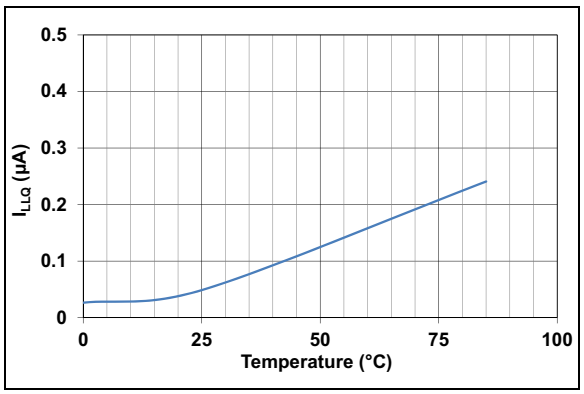


FIGURE 2-1: *I_{LLQ} vs. Temperature.*

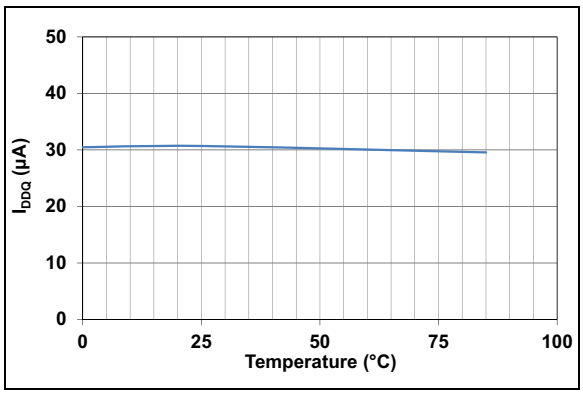


FIGURE 2-4: *I_{DDQ} vs. Temperature.*

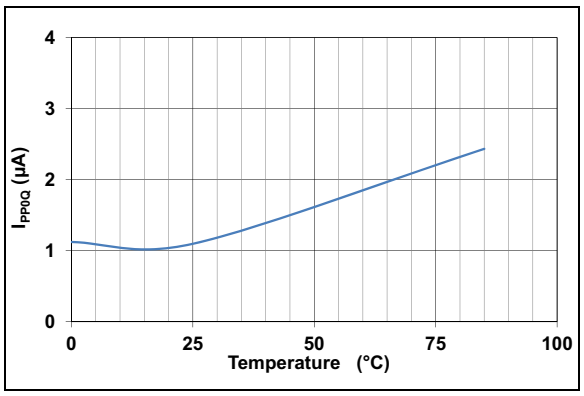


FIGURE 2-2: *I_{PP0Q} vs. Temperature.*

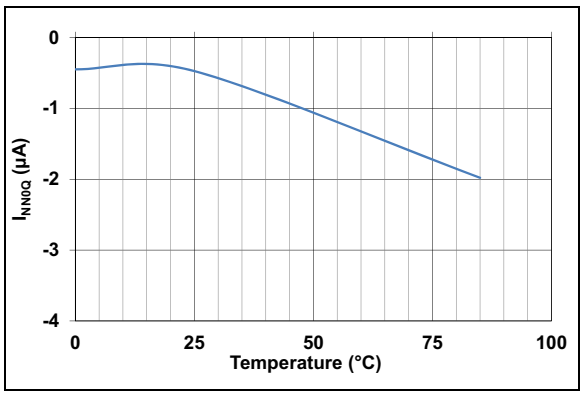


FIGURE 2-5: *I_{NN0Q} vs. Temperature.*

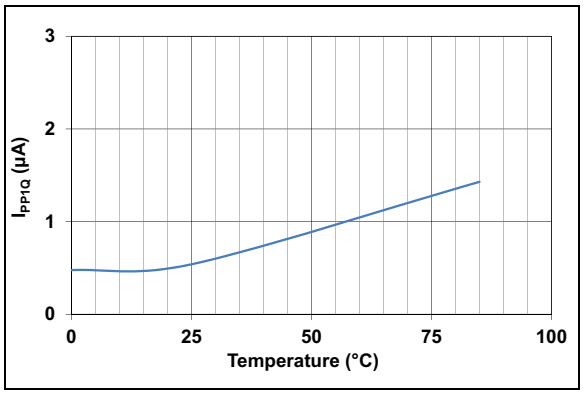


FIGURE 2-3: *I_{PP1Q} vs. Temperature.*

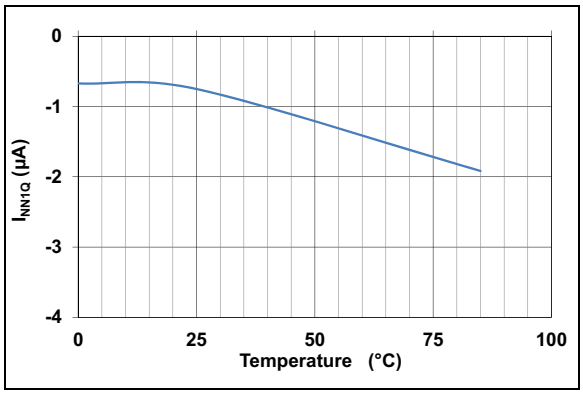


FIGURE 2-6: *I_{NN1Q} vs. Temperature.*

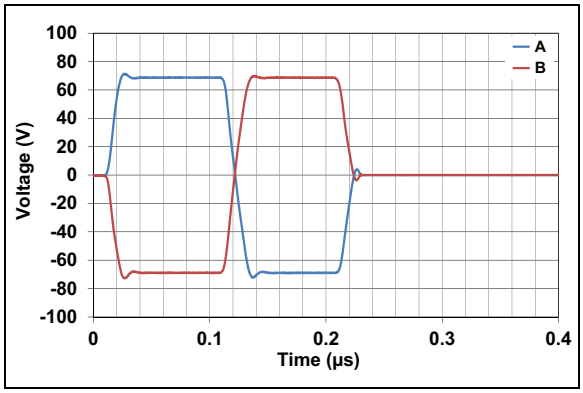


FIGURE 2-7: *TX Output Waveform, 1-Cycle 5 MHz with 220 pF//1K Load.*

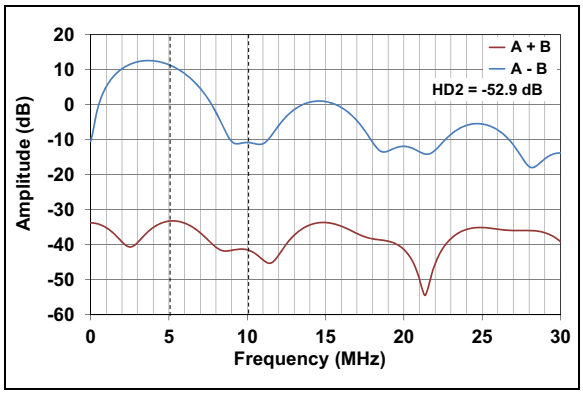


FIGURE 2-8: *TX Output HD2, 1-Cycle Inverting, 5 MHz with 220pF//1K Load.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin	Symbol	Description
1	CW_{IN0}	External CW input for channel 0
2	SEL1	SEL input logic pin selects transmission high-voltage rails for channel 1. If SEL = 0, select V_{PP0}/V_{NN0}. If SEL = 1, select V_{PP1}/V_{NN1}. See Table 1-1.
3	NEG1	NEG input logic pin turns on/off corresponding output N-channel MOSFET for channel 1. See Table 1-1.
4	POS1	POS input logic pin turns on/off corresponding output P-channel MOSFET for channel 1. See Table 1-1.
5	CW_{IN1}	External CW input for channel 1
6	OEN	Output enable logic input pin. When OEN = V_{LL}, the transmitter outputs are enabled. When OEN = 0, the transmitter outputs are disabled.
7	PWS	Logic input pin. When PWS = 0, the output FETs for V_{PP1} and V_{NN1} are scaled down to reduce the output current for CW Mode-0.
8	CLK	Re-timing clock input pin. Connect CLK to ground for transparent mode.
9, 22, 59	GND	Ground
10	V_{LL}	Input logic power supply pin
11	REN	Enable pin for the built-in voltage regulators.See section **Section 4.3 "Operation Modes"** for details.
12	SEL2	SEL input logic pin selects transmission high-voltage rails for channel 2. If SEL = 0, select V_{PP0}/V_{NN0}. If SEL = 1, select V_{PP1}/V_{NN1}. See Table 1-1.
13	NEG2	NEG input logic pin turns on/off corresponding output N-channel MOSFET for channel 2. See Table 1-1.
14	POS2	POS input logic pin turns on/off corresponding output P-channel MOSFET for channel 2. See Table 1-1.
15	CW_{IN2}	External CW input for channel 2
16	SEL3	SEL input logic pin selects transmission high-voltage rails for channel 3. If SEL = 0, select V_{PP0}/V_{NN0}. If SEL = 1, select V_{PP1}/V_{NN1}. See Table 1-1.
17	NEG3	NEG input logic pin turns on/off corresponding output N-channel MOSFET for channel 3. See Table 1-1.
18	POS3	POS input logic pin turns on/off corresponding output P-channel MOSFET for channel 3. See Table 1-1.
19	CW_{IN3}	External CW input for channel 3
20	OTP_N	Temperature sensor open drain output
21, 60	V_{DD}	+5V supply
23	V_{GP}	+10V supply pin for the linear regulator
24, 25, 56, 57	V_{PP0}	Positive high-voltage supply pin. V_{PP0} must be equal to or greater than V_{PP1}.
26, 55	C_{PF0}	Internal linear regulator output pin. Connect 2 µF 10V capacitor to V_{PP0}.
27, 54	C_{NF0}	Internal linear regulator output pin. Connect 2 µF 10V capacitor to V_{NN0}.
28, 29, 52, 53	V_{NN0}	Negative high-voltage supply pin. V_{NN0} must be equal to or more negative than $V_{NN1,2}$
30, 51	V_{NN2}	Negative high-voltage supply pin. V_{NN2} connects to the most negative supply rail.
31, 50	V_{NN1}	Negative high-voltage supply pin. V_{NN1} must be equal to or less negative than V_{NN0}.
32, 49	C_{NF1}	Internal linear regulator output pin. Connect 2 µF 10V capacitor to V_{NN1}.
33, 48	C_{PF1}	Internal linear regulator output pin. Connect 2 µF 10V capacitor to V_{PP1}.
34, 47	V_{PP1}	Positive high voltage supply V_{PP1}. Must be equal to or lower than V_{PP0}.
35	TX3	Channel 3 transmitter output pin

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin	Symbol	Description
36	RX3	Channel 3 T/R switch output
37, 44	R_{GND}	Power ground
38	RX2	Channel 2 T/R switch output
39	TX2	Channel 2 transmitter output pin
40	C_{NEG}	Internal linear regulator output pin. Connect 1 µF 10V capacitor to GND.
41	C_{POS}	Internal linear regulator output pin. Connect 1 µF 10V capacitor to GND.
42	TX1	Channel 1 transmitter output pin
43	RX1	Channel 1 T/R switch output
45	RX0	Channel 0 T/R switch output
46	TX0	Channel 0 transmitter output pin
58	V_{GN}	-10V supply pin for the linear regulator
61	MODE	CW Mode selection pin. See section **Section 4.3 "Operation Modes"**.
62	SEL0	SEL input logic pin selects transmission high-voltage rails for channel 0. If SEL = 0, select V_{PP0}/V_{NN0}. If SEL = 1, select V_{PP1}/V_{NN1}. See Table 1-1.
63	NEG0	NEG input logic pin turns on/off corresponding output N-channel MOSFET for channel 0. See Table 1-1.
64	POS0	POS input logic pin turns on/off corresponding output P-channel MOSFET for channel 0. See Table 1-1.
Thermal Pad	V_{SUB}	Connect to ground.

4.0 DEVICE DESCRIPTION

4.1 Overview

The HV7321 is a 4-channel, 5-level ultrasound transmitter with built-in T/R switches, output protection diodes and clamp diodes.

The HV7321 can provide up to ±2.6A and the output voltage swing can be up to ±80V.

The HV7321 supports both Transparent and Re-Timing mode. The re-timing clock frequency can support up to 220 MHz. The re-timing feature helps reduce the output jitter introduced by the driving FPGA.

4.2 Recommended Power-up Sequence

Powering up/down in any arbitrary sequence will not cause any damage to the device. The powering-up sequences in Table 4-1 are only recommended in order to minimize possible in-rush current. Figure 4-1 shows the timing diagram of related signals.

TABLE 4-1: POWER-UP SEQUENCE

Step	Power-Up Description
1	V_{LL} ON with logic signal low
2	V_{DD}, V_{GP} and V_{GN} ON
3	REN = 1
4	$V_{PP0,1}$ and $V_{NN0,1}$ ON
5	OEN = 1 & Logic control signal active

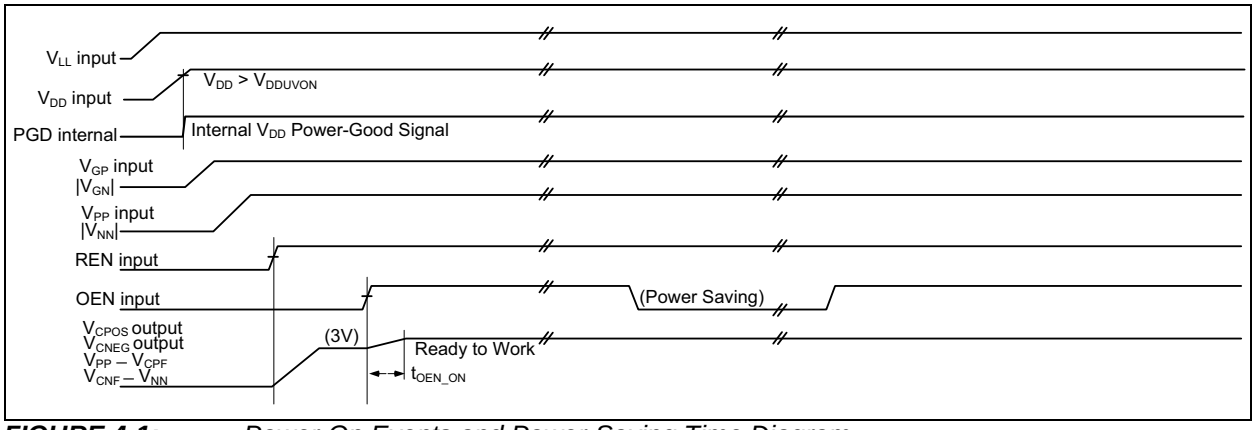


FIGURE 4-1: *Power-On Events and Power-Saving Time Diagram.*

4.3 Operation Modes

There are five modes of operation: Device Disabled, Output Disabled, Pulsed-Echo Mode, CW Mode-0 and CW Mode-1.

4.3.1 DEVICE ENABLE MODE

In Device Disabled mode, the regulators are turned off when REN is low. The regulators are ON when REN = V_{LL}. All regulators are ON except V_{NEG} and V_{POS} for power saving when REN = 1. When REN is low, OEN = X (OEN = 1 or 0) since device is disabled. Refer to Table 4-2.

TABLE 4-2: REN & OEN LOGIC INPUTS

REN	OEN	Device	TX Output
0	X	Disabled	high Z
1	0	Enabled	high Z
1	1	Enabled	ON

4.3.2 OUTPUT HIGH Z MODE

In Output Disabled mode, regulators are enabled REN = 1 and OEN = 0 (Output Enable logic input) and output pins (TX0-3) are in high Z state. OEN = 1 enables the outputs.

4.3.3 PULSED-ECHO MODE

Pulsed-Echo mode (B-mode) enables the 5-level waveform generation. OEN = 1, MODE = 0, and PWS = 1 enable Pulsed-Echo mode after HV7321 powers on. SEL/NEG/POS inputs of desired channel determine the corresponding TX Output pulse.

4.3.4 CW MODE-0

CW Mode-0 enables continuous wave mode provided solely by the HV7321. OEN = 1, MODE = 0 and PWS = 0 activate CW Mode-0. FPGA selects V_{PP1} and V_{NN1} amplitudes via SEL/NEG/POS inputs.

In theory, V_{PP0} and V_{NN0} can be selected but this is strongly discouraged since V_{PP0} and V_{NN0} usage increases power consumption and causes excessive heating in CW Mode-0.

4.3.5 CW MODE-1

CW Mode-1 is enabled using an external CW signal source for continuous wave mode. OEN = 1 and MODE = 1 activate CW Mode-1. External CW signals can connect to any of CW_{IN0-3}. In this mode, the CW signal source also feeds the CLK input. See Table 4-3 for details.

TABLE 4-3: MODE & PWS LOGIC INPUTS

Mode	PWS	State
0	0	CW Mode-0
0	1	Pulsed-Echo
1	X	CW Mode-1

4.3.5.1 External CW Beamformer Option (CW Mode-1)

The HV7321 has built-in CW switches that allow the use of an external CW beamformer to further minimize jitter and phase noise on CW waveforms. This mode is called CW Mode-1.

One suggested external CW beamformer is the MD1730, which has very low phase noise and 8-channel CW output. A pair of HV7321s can operate with the MD1730 as an 8-channel CW waveform generator. See Figure 4-2.

The MD1730 supports both differential and single-ended signals using CLKP and CLKN inputs. The MD1730 enables setting the CW output phase delay and frequency for channels via SPI. Please refer to the MD1730 data sheet for more information.

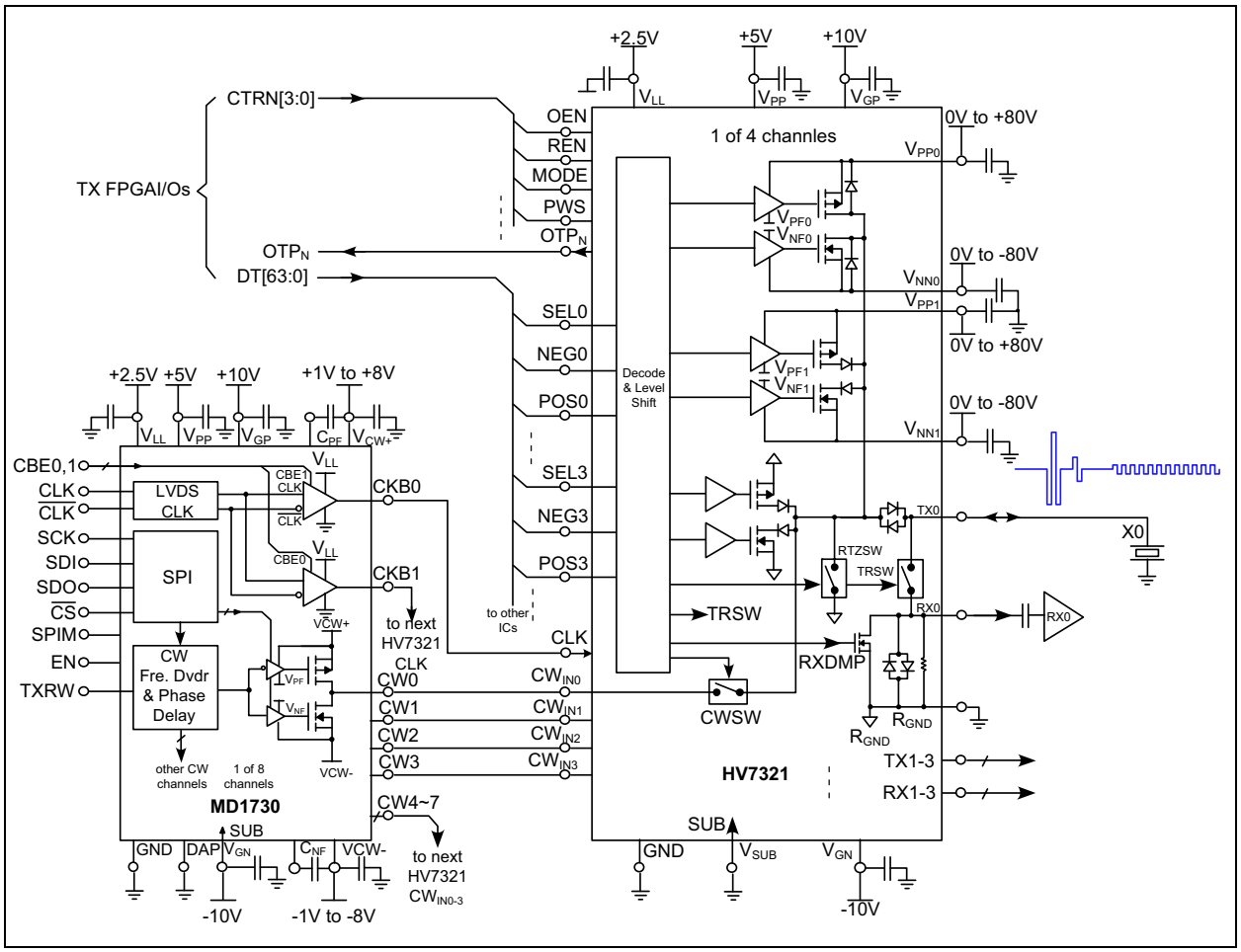


FIGURE 4-2: *HV7321 + MD1730 Integration.*

4.4 High Temperature Protection

When overtemperature is detected, OTPN = 0 and all outputs are high Z regardless of OEN and the other logic control inputs. Table 4-4 shows the relationship between REN, OEN inputs, OTPN output, and the corresponding device status.

TABLE 4-4: REN, OEN, OTP_N VS. DEVICE STATUS

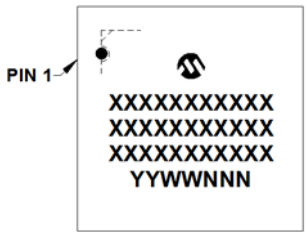
OTP_N	REN	OEN	Device	TX Output
0	0	X	Disabled	high Z
0	1	X	Enabled	high Z
1	0	X	Disabled	high Z
1	1	0	Enabled	high Z
1	1	1	Enabled	ON

NOTES:

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

64-Lead VQFN (9 x 9 x 1.0 mm)

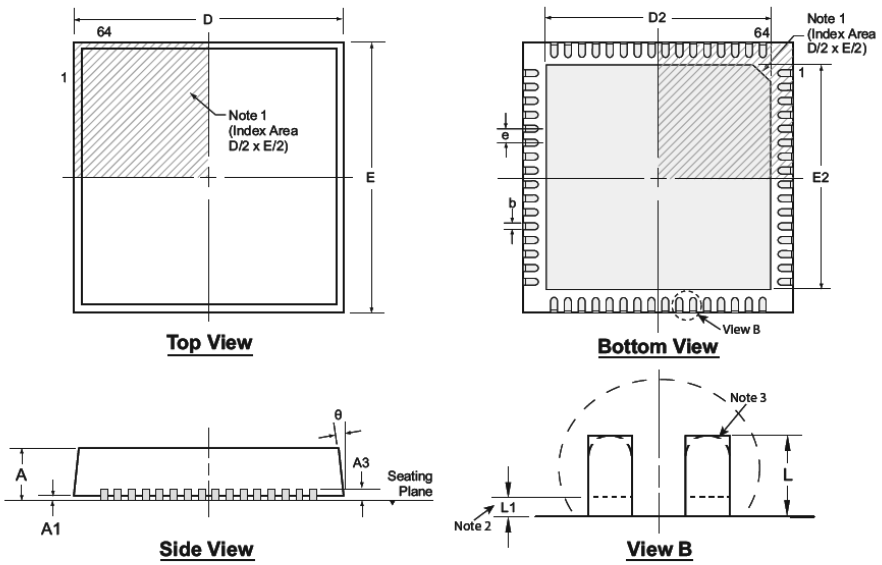


Example

Legend:	XX...X Product Code or Customer-specific information Y Year code (last digit of calendar year) YY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01') NNN Alphanumeric traceability code (e3) Pb-free JEDEC designator for Matte Tin (Sn) ***** This package is Pb-free. The Pb-free JEDEC designator ( ) (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

64-Lead QFN Package Outline (K6)

9.00x9.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	8.85*	6.00	8.85*	6.00	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	9.00	7.70*	9.00	7.70*		0.40	-	-
	MAX	1.00	0.05		0.30	9.15*	7.80†	9.15*	7.80†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VMMD-4, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-X
Device	Package	Environmental

Device:	HV7321:	4-Ch. 5-Level ±80V High-Voltage Ultrasound Pulser with T/R Switches
Package:	K6 =	Very Thin Plastic Quad Flat Pack, No Lead Package, 9.00 x9.00 x1.0 mm Body, 0.50 mm Pitch, 64-Lead (VQFN)
Environmental:	G =	Lead (Pb)-free/ROHS-compliant package

Examples:

a) HV7321K6-G: 4-Ch. 5-Level ±80V High-Voltage Ultrasound Pulser with T/R Switches 64LD 9x9 mm VQFN package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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