T-67-21-55

National Semiconductor

74FCT138A
1-of-8 Decoder/Demultiplexer

General Description

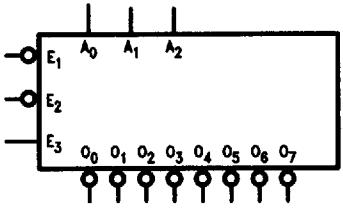
The 'FCT138A is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'FCT138A devices or a 1-of-32 decoder using four 'FCT138A devices and one inverter.

Features

- I_{CC} reduced to 40.0 μA
- NSC 74FCT138A is pin and functionally equivalent to IDT 74FCT138A
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA
- CMOS power levels
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols



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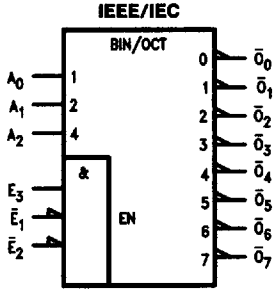
IEEE/IEC



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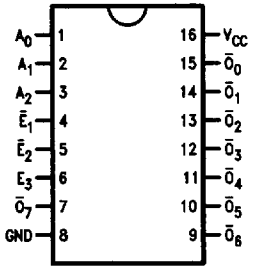
Connection Diagram

Pin Assignment for DIP and SOIC



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Pin Names	Description
A_0–A_2	Address Inputs
$\bar{E}_1$–$\bar{E}_2$	Enable Inputs
E_3	Enable Input
$\bar{O}_0$–$\bar{O}_7$	Outputs

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Functional Description

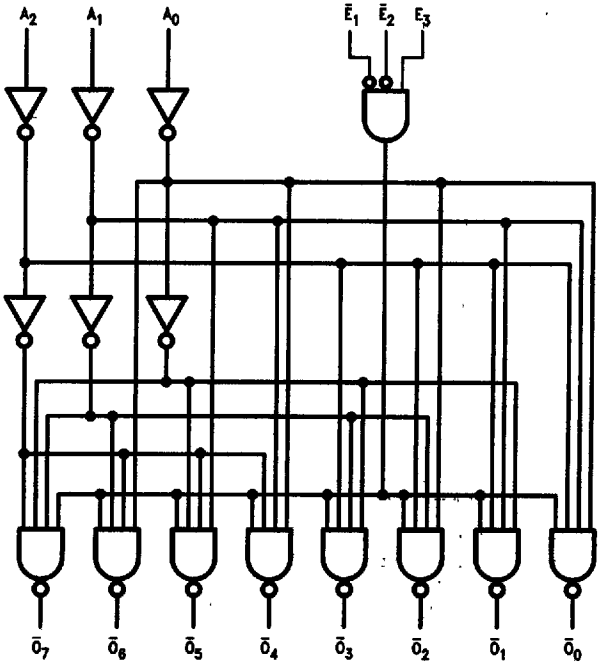
The 'FCT138A high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The 'FCT138A features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'FCT138A devices and one inverter (see *Figure 1*). The 'FCT138A can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
74FCTA −0.5V to 7.0V

Temperature Under Bias (T_{BIAS})
74FCTA −55°C to +125°C

Storage Temperature (T_{STG})
74FCTA −55°C to +125°C

Power Dissipation (P_T) 0.5W

DC Output Current (I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum ratings for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
74FCTA 4.75V to 5.25V

Input Voltage 0V to V_{CC}

Output Voltage 0V to V_{CC}

Operating Temperature (T_A)
74FCTA 0°C to +70°C

Junction Temperature (T_J)
PDIP 140°C

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCTA Min	74FCTA Typ	74FCTA Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4	V_{CC} 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −15 mA
V_{OL}	Maximum Low Level Output Voltage		GND GND 0.3	0.2 0.2 0.5	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
						V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA
I_{CC}	Maximum Quiescent Supply Current		1.0	40.0	μA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)			0.45	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCTA Min	74FCTA Typ	74FCTA Max	Units	Conditions	
I_C	Total Power Supply Current (Note 6)			5.0	mA	V_{CC} = Max Outputs Open f_i = 10 MHz Enable Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				5.5			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	Conditions	74FCTA T_A, V_{CC} = Com, R_L = 500Ω, C_L = 50 pF (Note 1) Min	74FCTA Max	Units	Fig. No.
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	C_L = 50 pF R_L = 500Ω	1.5	5.8	ns	2-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	C_L = 50 pF R_L = 500Ω	1.5	5.9	ns	2-9
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	C_L = 50 pF R_L = 500Ω	1.5	5.9	ns	2-9

Note 1: Minimum limits guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f = 1.0 MHz

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.