

For Immediate Assistance, Contact Your Local Salesperson



ADS7833

DEMO BOARD
AVAILABLE
See Appendix A

www.burr-brown.com/databook/ADS7833.html

10-Channel, 12-Bit DATA ACQUISITION SYSTEM

FEATURES

- 3 SIMULTANEOUS SAMPLED CHANNELS
- 3 SYNCHRONIZED 12-BIT ADCs
- 6.6 μ s THROUGHPUT RATE
- FULLY DIFFERENTIAL MUX INPUTS
- DIGITALLY SELECTABLE INPUT RANGES
- ± 5 V POWER SUPPLIES
- SERIAL DIGITAL INPUT/OUTPUTS
- 2 SIMULTANEOUS SAMPLED AUXILIARY CHANNELS
- DIRECT INTERFACE TO MOTOROLA'S DSP56004/7

DESCRIPTION

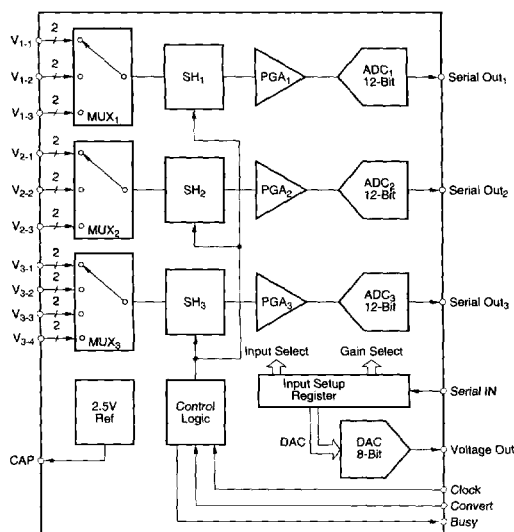
The ADS7833 consists of three 12-bit analog-to-digital converters preceded by three simultaneously operating sample-and-hold amplifiers, and multiplexers for 10 differential inputs. The ADCs have simultaneous serial outputs for high speed data transfer and data processing.

The ADS7833 also offers a programmable gain amplifier with programmable gains of 1.0V/V, 1.25V/V, 2.5V/V, and 5.0V/V. Channel selection and gain selection are selectable through the serial input control word. The high throughput rate is maintained by simultaneously clocking in the 13-bit input control word for the next conversion while the present conversions are clocked out.

The part also contains an 8-bit digital-to-analog converter whose digital input is supplied as part of the input control word.

APPLICATIONS

- AC MOTOR SPEED CONTROLS
- THREE PHASE POWER CONTROL
- UNINTERRUPTABLE POWER SUPPLIES
- VIBRATION ANALYSIS
- PC DATA ACQUISITION
- MEDICAL INSTRUMENTATION



Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

At $V_{ANA+} = +5V$, $V_{ANA-} = -5V$, $V_{DIG+} = +5V$, $V_{DIG-} = -5V$, and $T_A = -40^{\circ}C$ to $+85^{\circ}C$, using internal reference, $f_{CLOCK} = 2.1MHz$.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

PARAMETER	CONDITIONS	ADS7833N			UNITS
		MIN	TYP	MAX	
RESOLUTION		12			Bit
ANALOG INPUT Full Scale Voltage, Differential	$G = 1.0V/V$ $G = 1.25V/V$ $G = 2.5V/V$ $G = 5.0V/V$		± 2.5 ± 2.0 ± 1.0 ± 0.5		V V V V
Common-Mode Voltage		± 0.5	See Table VII		V
Impedance			10^{12}		Ω
Capacitance			20		pF
THROUGHPUT SPEED Conversion Time Complete Cycle Throughput Rate	CLK = 2.1MHz Acquire and Convert			6.1 6.6	μs μs kHz
SAMPLING DYNAMICS S/H Droop Rate S/H Acquisition Time S/H Aperture Delay S/H Aperture Jitter Sampling Skew, Channel-to-Channel			0.1 0.5 50 50 3		$\mu V/\mu s$ μs ns ps ns
DC ACCURACY Integral Linearity - ADC Differential Linearity - ADC No Missing Codes Integral Linearity - Asynchronous, Synchronous Differential Linearity - Asynchronous, Synchronous Full Scale Error Full Scale Error Other Gains Full Scale Error Drift Zero Error - ADC Zero Error - Asynchronous, Synchronous Zero Error Drift	$G = 1.0V/V$ $G = 1.0V/V$ $G = 2.5V/V$ $G = 1.0V/V$ $G = 1.0V/V$ $G = 1.0V/V$	12	± 0.5 ± 0.5 0.5 0.5 ± 10 ± 10 ± 0.5 ± 0.5 ± 0.5	± 2 ± 3 ± 3 2 4 ± 100 ± 100 ± 15 ± 20	LSB LSB Bits LSB LSB % of FSR % of FSR ppm/ $^{\circ}C$ ppm/ $^{\circ}C$ LSB LSB ppm/ $^{\circ}C$
AC ACCURACY Total Harmonic Distortion $f_{IN} = 1kHz$ $f_{IN} = 1MHz$ CMR	$V_{CM} = 1V$, $f_{CM} = 1MHz$		92 72 40		dB dB dB
REFERENCE Internal Reference Voltage Internal Reference Accuracy Internal Reference Drift Internal Reference Source Current External Reference Voltage Range for Specified Linearity External Reference Current Drain		2.25	2.5 ± 0.25 ± 10 10 2.5 10	2.75	V % ppm/ $^{\circ}C$ μA V μA
DIGITAL INPUTS Logic Levels V_{IL} V_{IH} I_{IL} I_{IH} Input Capacitance	At All Digital Input Pins	0 +3.5		1.5 +5 ± 10 ± 10 15	V V μA μA pF
DIGITAL OUTPUTS Data Format Data Coding V_{OL} V_{OH} Leakage Current Output Capacitance	$I_{SINK} = 1.6mA$ $I_{SOURCE} = 500\mu A$ At All Digital Output Pins	0 4.2	12-Bit Serial BTC	0.4 5 ± 5 15	V V μA pF

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SPECIFICATIONS (CONT)

At $V_{ANA+} = +5V$, $V_{ANA-} = -5V$, $V_{DIG+} = +5V$, $V_{DIG-} = -5V$, and $T_A = -40^{\circ}C$ to $+85^{\circ}C$, using internal reference, $f_{CLOCK} = 2.1MHz$.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

PARAMETER	CONDITIONS	ADS7833N			UNITS
		MIN	TYP	MAX	
POWER SUPPLIES	Specified Performance				
V_{ANA+}		+4.75	+5.0	+5.25	V
V_{ANA-}		-4.75	-5.0	-5.25	V
V_{DIG+}		+4.75	+5.0	+5.25	V
V_{DIG-}		-4.75	-5.0	-5.25	V
I_{ANA+}			15	25	mA
I_{ANA-}			8	10	mA
I_{DIG+}			3	5	mA
I_{DIG-}			1	2	mA
Power Dissipation			125		mW
TEMPERATURE RANGE					
Specified Performance		-40		+85	$^{\circ}C$
Derated Performance		-55		+125	$^{\circ}C$
Storage		-65		+150	$^{\circ}C$

DIGITAL-TO-ANALOG CONVERTER

PARAMETER	CONDITIONS	ADS7833N			UNITS
		MIN	TYP	MAX	
RESOLUTION		8-Bits			
Output Range	T_D 0.5LSB	0		+2.5	V
Output Settling Time				1	μs
Linearity Error				± 1	LSB
Differential Linearity				± 1	LSB
Output Current		200			μA
Offset Error			± 1	10	mV
Full Scale Error				2	%

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltage	$\pm 25V$
Ground Voltage Difference: AGND and DGND	$\pm 0.3V$
Power Supply Voltages:	
V_{ANA+}	+7V
V_{ANA-}	-7V
V_{DIG+}	+7V
V_{DIG-}	-7V
Digital Inputs	-0.3V to $V_{DIG} + 0.3V$
Maximum Junction Temperature	+165 $^{\circ}C$
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300 $^{\circ}C$

CONVERSION AND DATA TIMING

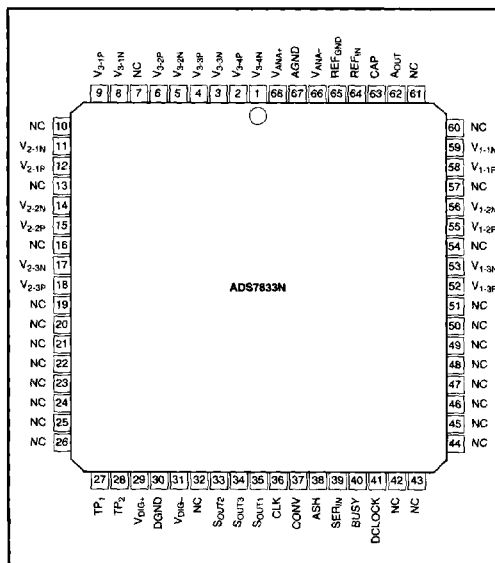
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	A/D Conversion Time	6.6	4.0		μs
CLK	A/D Conversion Clock	2.1	2.8		MHz
t_1	Setup Time for Conversion Before Rising Edge of Clock	50			ns
t_2	Hold Time for Conversion After Rising Edge of Clock	50			ns
t_3	Setup Time for Serial Out		25		ns
t_4	Setup Time for Serial Input	30			ns
t_5	Hold Time for Serial Input	30			ns

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
ADS7833N	68-Lead PLCC	312

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION



Or, Call Customer Service at 1-800-548-6132 (USA Only)

PIN DEFINITIONS

PIN NO	NAME	TYPE ⁽¹⁾	DESCRIPTION	PIN NO	NAME	TYPE ⁽¹⁾	DESCRIPTION
1	V _{3-4N}	AI	Voltage Input, Channel 3, Mux I/P 4, Negative Side	35	S _{OUT1}	DO	Serial Digital Output, Channel 1
2	V _{3-4P}	AI	Voltage Input, Channel 3, Mux I/P 4, Positive Side	36	CLK	DI	Clock for A/D Converters
3	V _{3-3N}	AI	Voltage Input, Channel 3, Mux I/P 3, Negative Side	37	CONV	DI	Start A/D Converters. When CONV goes to "0" (low) the next rising edge of CLK starts the conversion.
4	V _{3-3P}	AI	Voltage Input, Channel 3, Mux I/P 3, Positive Side	38	ASH	DI	Digital Control for Asynchronous Sample Hold. If signal is "1" (high), signals are sampled.
5	V _{3-2N}	AI	Voltage Input, Channel 3, Mux I/P 2, Negative Side	39	SER _{IN}	DI	Serial Digital Input for Input Control Word
6	V _{3-2P}	AI	Voltage Input, Channel 3, Mux I/P 2, Positive Side	40	BUSY	DO	A/D Converters Busy. Busy if signal is "0" (low).
7	NC	—	No Connection	41	DCLOCK	DO	A Delayed and Truncated Version of the CLK Signals. It is Delayed 50ns from the CLK Signal and Stays Low after 13 DCLOCK Cycles.
8	V _{3-1N}	AI	Voltage Input, Channel 3, Mux I/P 1, Negative Side	42	NC	—	No Connection
9	V _{3-1P}	AI	Voltage Input, Channel 3, Mux I/P 1, Positive Side	43	NC	—	No Connection
10	NC	—	No Connection	44	NC	—	No Connection
11	V _{2-1N}	AI	Voltage Input, Channel 2, Mux I/P 1, Negative Side	45	NC	—	No Connection
12	V _{2-1P}	AI	Voltage Input, Channel 2, Mux I/P 1, Positive Side	46	NC	—	No Connection
13	NC	—	No Connection	47	NC	—	No Connection
14	V _{2-2N}	AI	Voltage Input, Channel 2, Mux I/P 2, Negative Side	48	NC	—	No Connection
15	V _{2-2P}	AI	Voltage Input, Channel 2, Mux I/P 2, Positive Side	49	NC	—	No Connection
16	NC	—	No Connection	50	NC	—	No Connection
17	V _{2-3N}	AI	Voltage Input, Channel 2, Mux I/P 3, Negative Side	51	NC	—	No Connection
18	V _{2-3P}	AI	Voltage Input, Channel 2, Mux I/P 3, Positive Side	52	V _{1-3P}	AI	Voltage Input, Channel 1, Mux I/P 3, Positive Side
19	NC	—	No Connection	53	V _{1-3N}	AI	Voltage Input, Channel 1, Mux I/P 3, Negative Side
20	NC	—	No Connection	54	NC	—	No Connection
21	NC	—	No Connection	55	V _{1-2P}	AI	Voltage Input, Channel 1, Mux I/P 2, Positive Side
22	NC	—	No Connection	56	V _{1-2N}	AI	Voltage Input, Channel 1, Mux I/P 2, Negative Side
23	NC	—	No Connection	57	NC	—	No Connection
24	NC	—	No Connection	58	V _{1-1P}	AI	Voltage Input, Channel 1, Mux I/P 1, Positive Side
25	NC	—	No Connection	59	V _{1-1N}	AI	Voltage Input, Channel 1, Mux I/P 1, Negative Side
26	NC	—	No Connection	60	NC	—	No Connection
27	TP1	—	Test Point 1, Make No Connection	61	NC	—	No Connection
28	TP2	—	Test Point 2, Make No Connection	62	A _{OUT}	AO	Output of DAC
29	V _{DIG+}	P	Digital Supply Voltage, +5V	63	CAP	AO	Decoupling Point for Internal Reference
30	DGND	P	Digital Supply Voltage, Ground	64	REF _{IN}	AI	Input Pin for External Reference
31	V _{DIG-}	P	Digital Supply Voltage, -5V	65	REF _{GND}	P	Ground Pin for External Reference
32	NC	—	No Connection	66	V _{ANA-}	P	Analog Supply Voltage, -5V
33	S _{OUT2}	DO	Serial Digital Output, Channel 2	67	AGND	P	Analog Supply Voltage, Ground
34	S _{OUT3}	DO	Serial Digital Output, Channel 3	68	V _{ANA+}	P	Analog Supply Voltage, +5V

NOTE: (1) AI is Analog Input, AO is Analog Output, DI is Digital Input, DO is Digital Output, P is Power Supply Connection.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.