High Current PROFET™

BTS50040-2SFA

Smart High-Side Power Switch
Dual Channel, 2x 4mΩ

Datasheet

High Current PROFET™
V2.0, 2016-02-02

Automotive

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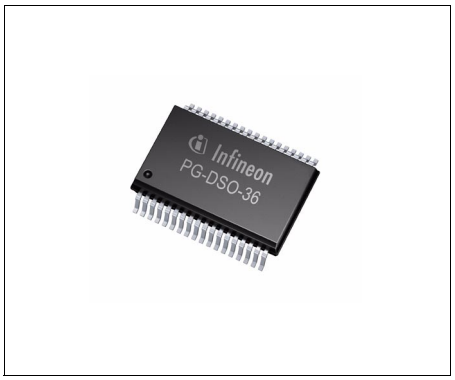
1 Overview



PG-DSO-36-44

Features

- 3.3 and 5V compatible, ground referenced CMOS compatible inputs for each channel
- Optimized electromagnetic compatibility (EMC)
- Very low standby current
- Slew rate configurable via external circuitry or signal
- Secure load turn-off while device ground disconnected
- ReverSave™ - Reverse battery protection without external components
- Inverse load current capability
- Infineon® INTELLIGENT LATCH
- Green Product (RoHS compliant) and halogen free package
- AEC qualified

Extended Supply Voltage Range for Operation	$V_{S(ext)}$	6 .. 28V
Logic Supply Voltage	V_{DD}	4.5 .. 5.5 V
Minimum power stage over-voltage protection	$V_{DS(CL))}$	40 V
Typical on-state resistance at T_j = 25°C (channel 0, 1)	$R_{DS(ON)}$	4.0 mΩ
Maximum on-state resistance at T_j = 150°C (channel 0, 1)	$R_{DS(ON)}$	8.2 mΩ
Typical nominal load current per channel, both channel active	$I_{L(nom)}$	11 A
Minimum short circuit shutdown threshold at T_j = -40°C	$I_{L(SC)}$	130 A
Maximum stand-by current for whole device with load for $T_j \leq 85$°C	$I_{S(OFF)}$	12 µA

Description

The BTS50040-2SFA is a dual channel high-side power switch in PG-DSO-36-44 package providing embedded protective functions including ReverSave™ and Infineon® INTELLIGENT LATCH. It is most suitable for loads with high inrush current, such as glow plugs, PTC heaters, or lamps.

The power transistors are built by a dual N-channel vertical power MOSFET with charge pump. The design is based on Smart power chip by chip technology.

The BTS50040-2SFA has ground referenced CMOS compatible inputs.

ReverSave™ is a protection feature that causes the power transistor to switch on in case of reverse polarity. As a result, the power dissipation is reduced.

Infineon® INTELLIGENT LATCH ensures a latched switch-off and reporting in case of fault condition.

Type	Package	Marking
BTS50040-2SFA	PG-DSO-36-44	S50040-2A

Power Stage

- Four different slew rates selectable via pin SRS0 and SRS1

Protective Functions

- Short circuit protection with latch
- Thermal shutdown with latch
- Infineon® INTELLIGENT LATCH - reset able latch resulting from protective switch-off
- ReverSave™ - Reverse battery protection by self turn on of power MOSFET
- Inverse load current capability - Inverse operation function
- Stable behavior at under voltage on V_S or V_{dd}
- Over voltage protection (including load dump)
- Loss of ground protection
- Loss of Vs protection (with external diode for charged inductive loads)
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Seperate enable function for current sense signal of each channel via pin SEN0 and SEN1
- Provides analog sense signal of load current in normal operation mode
- Provides low signal in case of over temperature and short circuit to ground
- Open load detection in ON-state by load current sense

Applications

- µC compatible high-side power switch with diagnostic feedback for 12 V system grounded loads in automotive applications
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, such as glow plugs, PTC heaters, or lamps
- Replaces electromechanical relays, fuses and discrete circuits

2 Block Diagram and Terms

2.1 Block Diagram

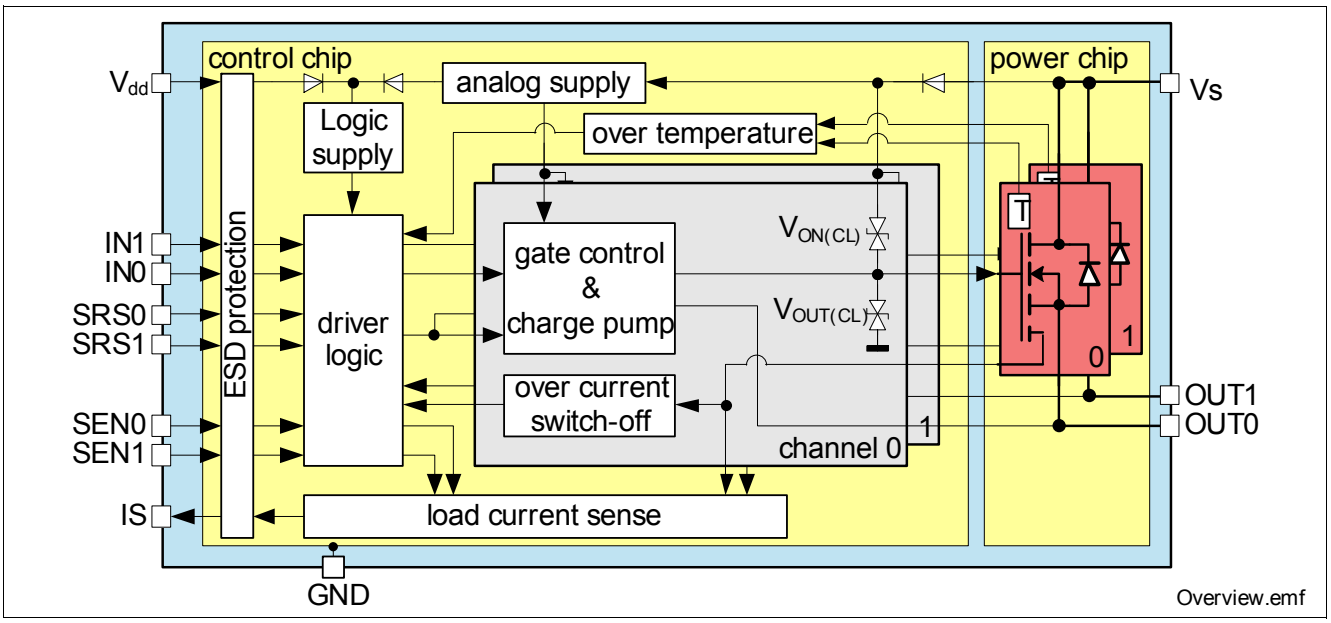


Figure 1 Block Diagram

2.2 Terms

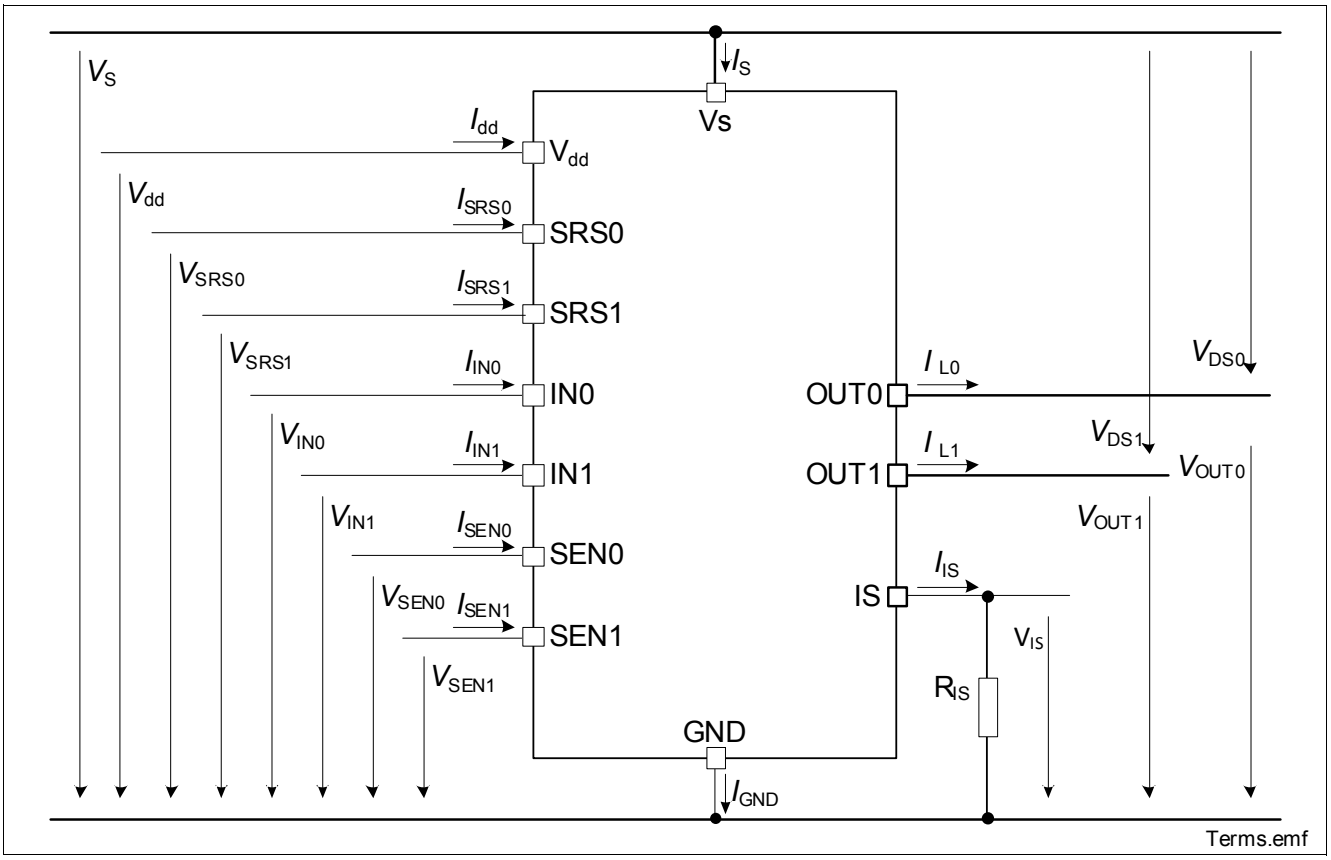


Figure 2 Terms

3 Pin Configuration

3.1 Pin Assignment BTS50040-2SFA

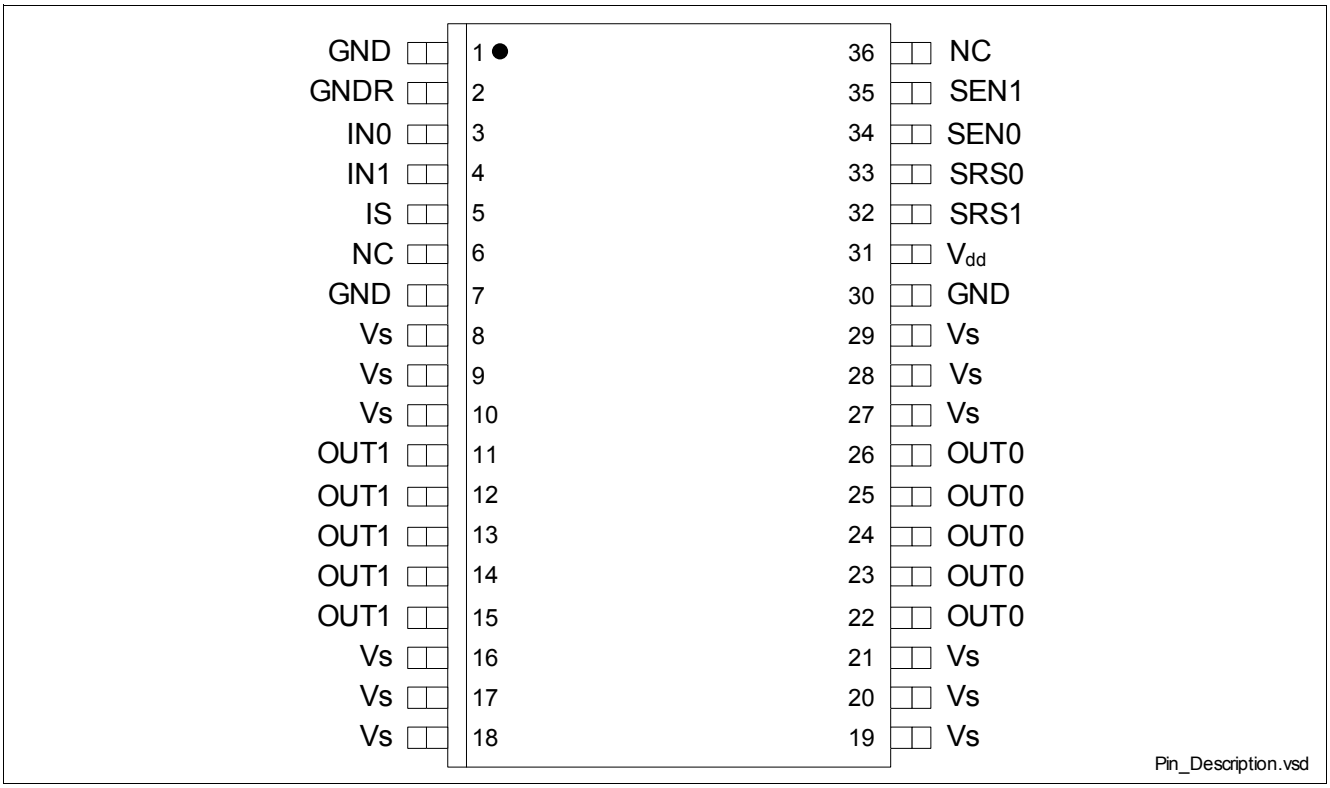


Figure 3 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1, 7, 30	GND	–	**Ground;** Ground connection for control chip[1)]
2	GNDR	–	**Ground reference**; Needs to be connected to GND.
3	IN0	I	**Input 0;** activates channel 0. Has an internal pull down resistor.
4	IN1	I	**Input 1;** activates channel 1. Has an internal pull down resistor.
5	IS	O	**Sense Output;** analog sense current signal proportional to I_{L0} or I_{L1}.
6, 36	NC	–	**Not connected;** For handling of NC pins, please see **Chapter 7.1**.
8..10, 16..21, 27..29	Vs	–	**Supply voltage;** Positive power supply for power outputs[1)]
11, 12, 13, 14, 15	OUT1	O	**Output of channel 1;** power output 1[1)]
22, 23, 24, 25, 26	OUT0	O	**Output of channel 0;** power output 0[1)]
31	Vdd	–	**Logic supply** (5V)
32	SRS1	I	**Slew rate selector pin 1.** See section **“Timings” on Page 23** for seetings.
33	SRS0	I	**Slew rate selector pin 0.** See section **“Timings” on Page 23** for seetings.
34	SEN0	I	**Sense Enable for channel 0.** See **Table 1 Truth Table for Power Stages**.
35	SEN1	I	**Sense Enable for channel 1.** See **Table 1 Truth Table for Power Stages**.

1) All GND pins have to be connected externally. All Vs pins have to be connected externally. All OUT pins of a channel have to be connected externally.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Operation outside the parameters listed here may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability

Absolute Maximum Ratings [1)]

Tj = -40 °C to +150 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Supply Voltage						
4.1.1	Supply voltage	V_S	0	28	V	–
4.1.2	Logic supply voltage	V_{dd}	-0.3	5.5	V	–
4.1.3	Reverse polarity voltage	$-V_{S(rev)}$	0	16	V	[2)] $T_{j(0)}$ = 25 °C $t \leq$ 2 min
4.1.4	Supply voltage for short circuit protection (single pulse)	$V_{bat(SC)}$	0	24	V	[3)] R_{SUPPLY} = 10 mΩ L_{SUPPLY} = 5 µH [R_{CABLE}; L_{CABLE}]= [20 mΩ; 0 µH] or [50 mΩ; 5 µH]
4.1.5	Supply Voltage for Load Dump protection	$V_{S(LD)}$	–	40	V	R_I = 2 Ω [4)], t_d =400 ms
4.1.6	Current through ground pin	I_{GND}	-34	25	mA	$t \leq$ 2 min
4.1.7	Current through Vdd pin	I_{dd}	-34	5	mA	$t \leq$ 2 min
Input Pins						
4.1.8	Voltage at digital input pins IN0, IN1, SRS0, SRS1, SEN0, SEN1	V_{DIO}	-0.3	5.5	V	–
4.1.9	Current through digital input pins IN0, IN1, SRS0, SRS1, SEN0, SEN1	I_{DIO}	-0.75 -2	0.75 2	mA	– $t \leq$ 2 min
Output Pins						
4.1.10	Voltage at sense pin	V_{IS}	-0.3	5.5	V	–
4.1.11	Current through sense pin IS	I_{IS}	–	20	mA	–
Power Stages						
4.1.12	Load current [5)]	$\|I_L\|$	–	$I_{L(SC)}$	A	–
4.1.13	Inductive load switch-off energy (single pulse)	E_{AS}	–	411	mJ	V_S = 13.5 V[6)] $I_{L(0)}$ = 20 A, $T_{j(0)} \leq$ 150 °C
4.1.14	Inductive load switch-off energy (repetitive pulses)	E_{AR}	–	64	mJ	V_S = 13.5V[7)] $I_{L(0)}$ = 20A $T_{j(0)} \leq$ 105 °C
Temperatures						
4.1.15	Junction temperature	T_j	-40	150	°C	–
4.1.16	Dynamic temperature increase while switching	ΔT_j	–	60	K	–
4.1.17	Storage temperature	T_{stg}	-55	150	°C	–

Absolute Maximum Ratings (cont'd)[1)]

Tj = -40 °C to +150 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
ESD Susceptibility						
4.1.18	ESD susceptibility HBM all pins Vs pins versus OUT	V_{ESD1}	 -2 -4	 2 4	kV	[7)]HBM
4.1.19	ESD susceptibility CDM all pins Pin 1, 18, 19, 36 (corner pins)	V_{ESD2}	 -500 -750	 500 750	V	[8)]CDM

1) Not subject to production test, specified by design.
2) At negative battery voltages (V_S < 0V) logic pins can reach negative potentials ($V_S \le V_{pin} \le$ GND). In this case, too high currents through affected pins have to be avoided by means of series resistors.
3) Setup in accordance with AEC Q100-012 and AEC Q101-006
4) $V_{S(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839. R_i is the internal resistance of the Load Dump pulse generator
5) Short circuit shutdown is a protection feature. Protection features are not designed for continuous repetitive operation.
6) See also **Chapter 5.1.3**. Resuls for E_{AR} from simulation of temperature swing.
7) ESD resistivity, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).
8) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

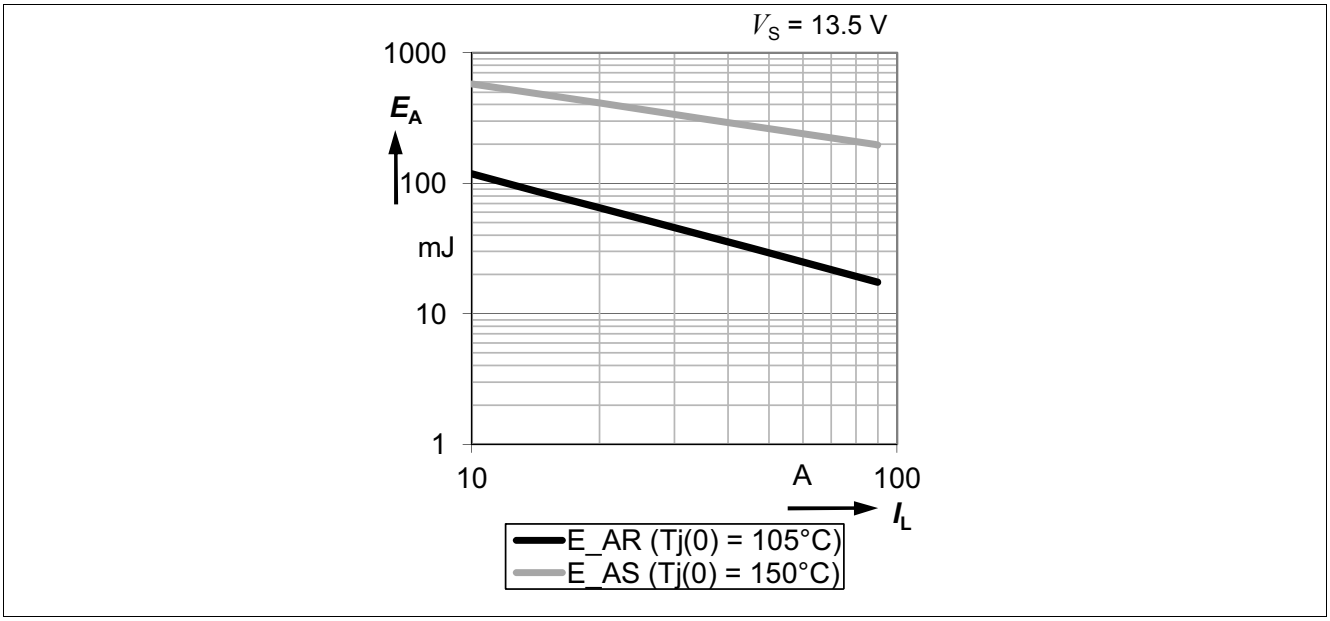


Figure 4 Maximum energy dissipation[1)]

Note: Clamping overrides all protection functionalities. In order to avoid device destruction resulting from inductive switch-off or over voltage the device has to be operated within the maximum ratings.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1) Not subject to production test, specified by design. Resuls for E_{AR} from simulation of temperature swing.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Supply Voltage						
4.2.1	Nominal Supply Voltage Range for Operation	$V_{S(NOM)}$	9	16	V	–
4.2.2	Extended Supply Voltage Range for Operation	$V_{S(EXT)}$ [1]	6	28	V	[2] $V_{dd} = V_{dd(NOM)}$
4.2.3	Logic Supply Voltage Range for Operation	$V_{dd(NOM)}$	4.5	5.5	V	–
4.2.4	Load current range for sense functionality [1]	$I_{L(IS)}$	2	40	A	$I_{IS} - I_{IS(LH)} > 30$ µA $I_{IS} < I_{IS(lim)}$ $V_{IS} < V_{IS(lim)}$ $V_S = V_{S(NOM)}$ $V_{INx} = V_{SENx} = 5$ V
4.2.5	Junction temperature	T_j	-40	150	°C	–

1) Not subject to production test, specified by design

2) In extended supply voltage range, the device is functional but electrical parameters are not specified.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Soldering point one channel active all channels active	R_{thjsp} [1]	 – –	 – –	 16 15	K/W	junction to Vs pins (8, 9, 10, 16, 17, 18, 19,20,21,27,28, 29)
4.3.2	Junction to Ambient one channel active all channels active	R_{thJA} [1]	 – –	 27 26	 – –	K/W	[2] T_a = 105 °C P_{loss} = 1W per channel cooling area I

1) Not subject to production test, specified by design

2) Specified R_{thJA} values is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

Figure 5 is showing the typical thermal impedance of BTS50040-2SFA mounted according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s and 2s2p board. The product (chip + package) was simulated on a 76,4 x 114,3 x 1,5 mm board with 2 inner copper layers (2x 70µm Cu, 2 x 35µm Cu). Where applicable, a thermal via

array under the exposed pad contacted the first inner copper layer. The PCB layer structure is shown in **Figure 6**. The PCB top view is shown in **Figure 7**.

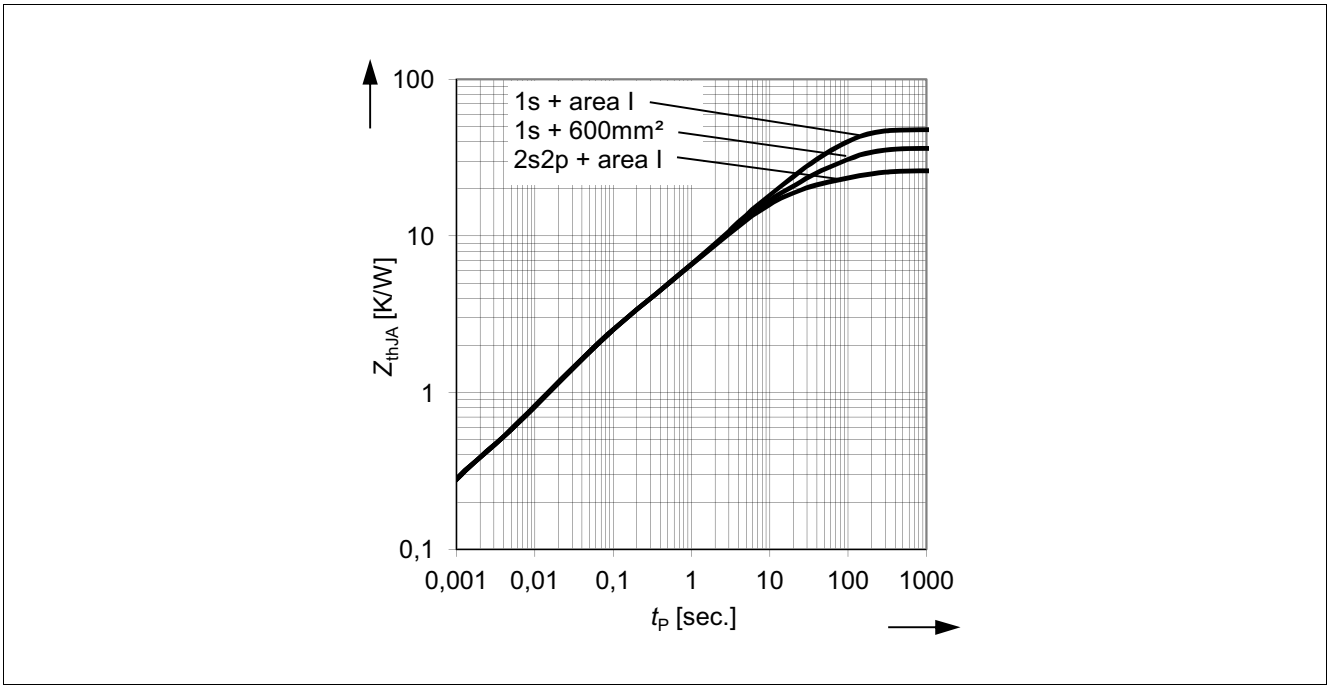


Figure 5 Typical transient thermal impedance Zth(JA) = f(tP) for different cooling areas

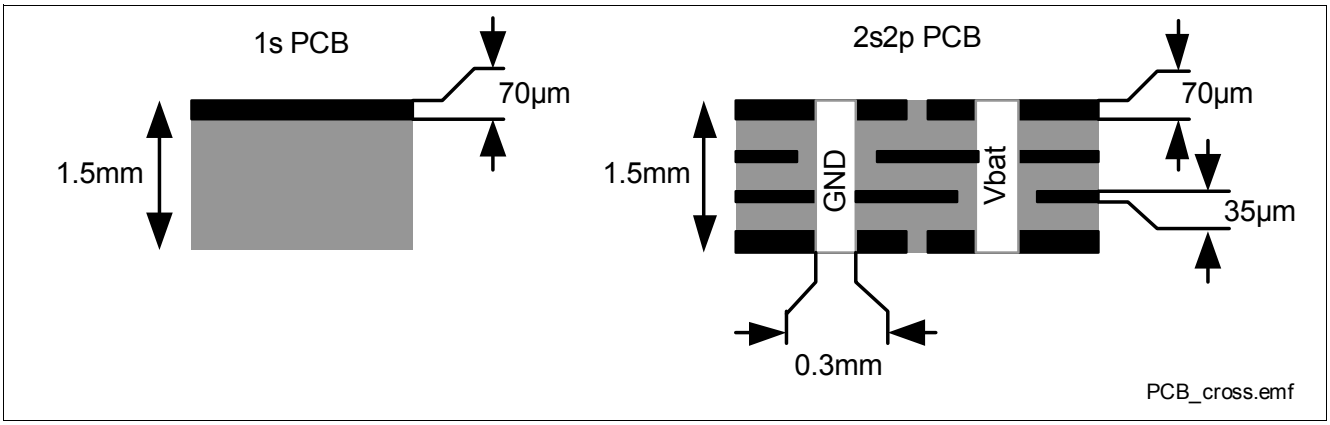


Figure 6 Cross section and front view of 1s and 2s2p PCB used for ZthJA simulation

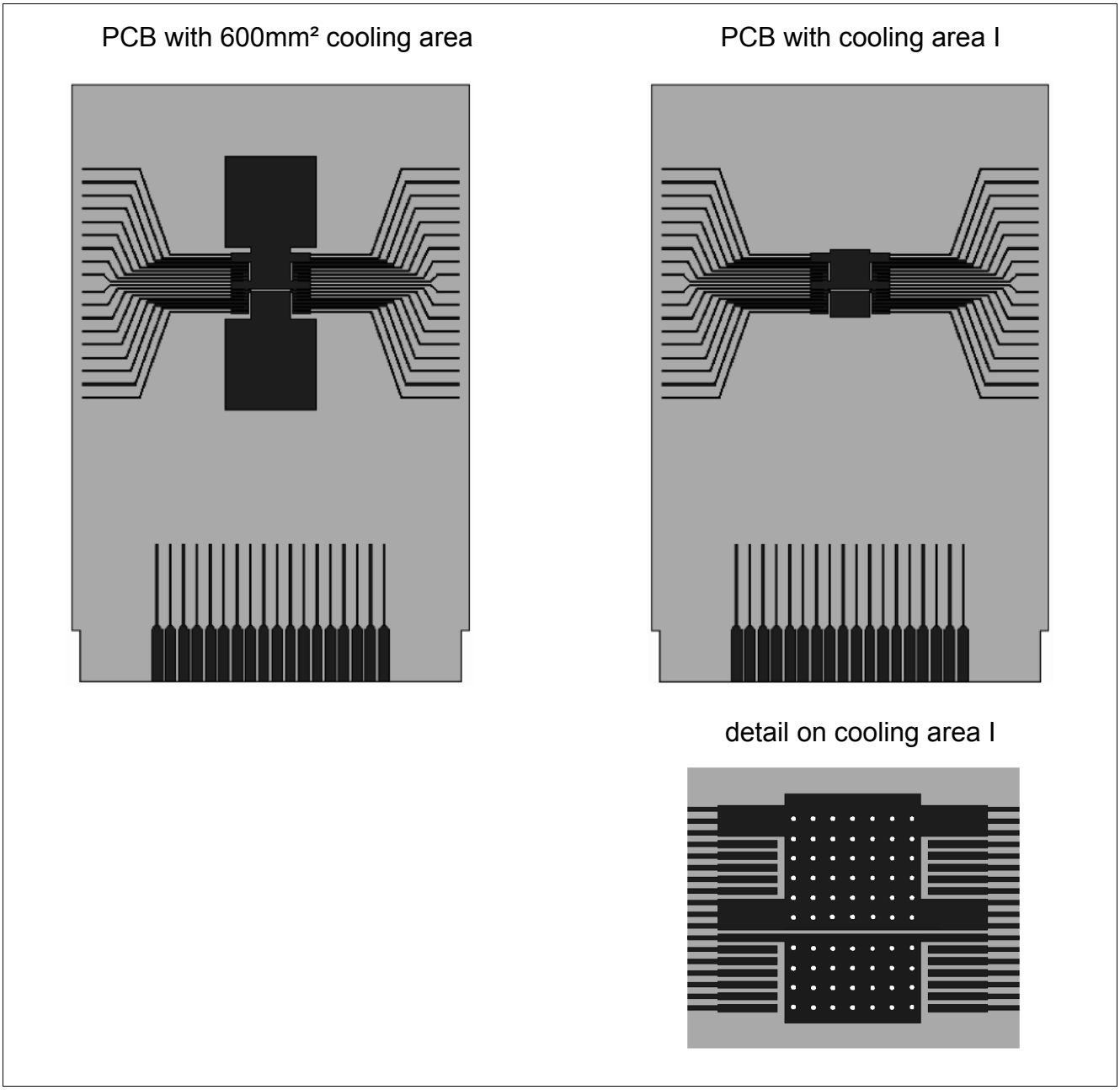


Figure 7 Top view of PCB with different cooling areas used for ZthJA simulation

4.4 Package

Pos.	Parameter	Value	Test Conditions
4.4.1	Jedec humidity category acc. J-STD-020-D	MSL3	–
4.4.2	Jedec classification temperature acc. J-STD-020-D	260°C	–

5 Functional Description

5.1 Power Stages

The BTS50040-2SFA is a high side switch with two independent outputs OUT0 and OUT1, made out of a dual N-channel power MOSFET with charge pump. For each channel, the BTS50040-2SFA provides sophisticated protection and diagnostic features.

Table 1 Truth Table for Power Stages

Operation Mode	Input (INx) Level	Output Level (OUTx)	Diagnostic Output (IS)	
			SENx = H	SENx = L
Normal Operation (ON)	H	~V_S	$I_{IS} = I_L / k_{ILIS}$	Z
Inverse Operation (-I_L)		>V_S	Z	
Short Circuit to V_S		V_S	< I_L / k_{ILIS}	
Open Load		~V_S	Z	
Protective switch-off resulting from Short Circuit to GND or Over Temperature [1]	X	Z	Z	Z
Undervoltage switch-off [2]				
Normal Operation (OFF)	L	Z	Z	Z
Inverse Operation (-I_L)		>V_S	Z	
Short Circuit to V_S		Z	Z	
Open Load				

L = Low Level, H = High Level, X = don't care, Z = high impedance, only leakage provided, potential depends on external circuit

1) Output state and fault reporting remains latched until reset signal (SEN0=SEN1=High).

2) After undervoltage shutdown, undervoltage restart is delayed ($t_{delay(UV)}$) if V_{dd} = $V_{dd(NOM)}$, V_{IN} = HIGH.

5.1.1 Output On-State Resistance

The on-state resistance $R_{DS(ON)}$ of each channel depends on the supply voltage V_S and the junction temperature T_j. **Figure 8** shows these dependencies for the typical on-state resistance. The on-state resistance in reverse polarity mode is described in **Chapter 5.3.3**.

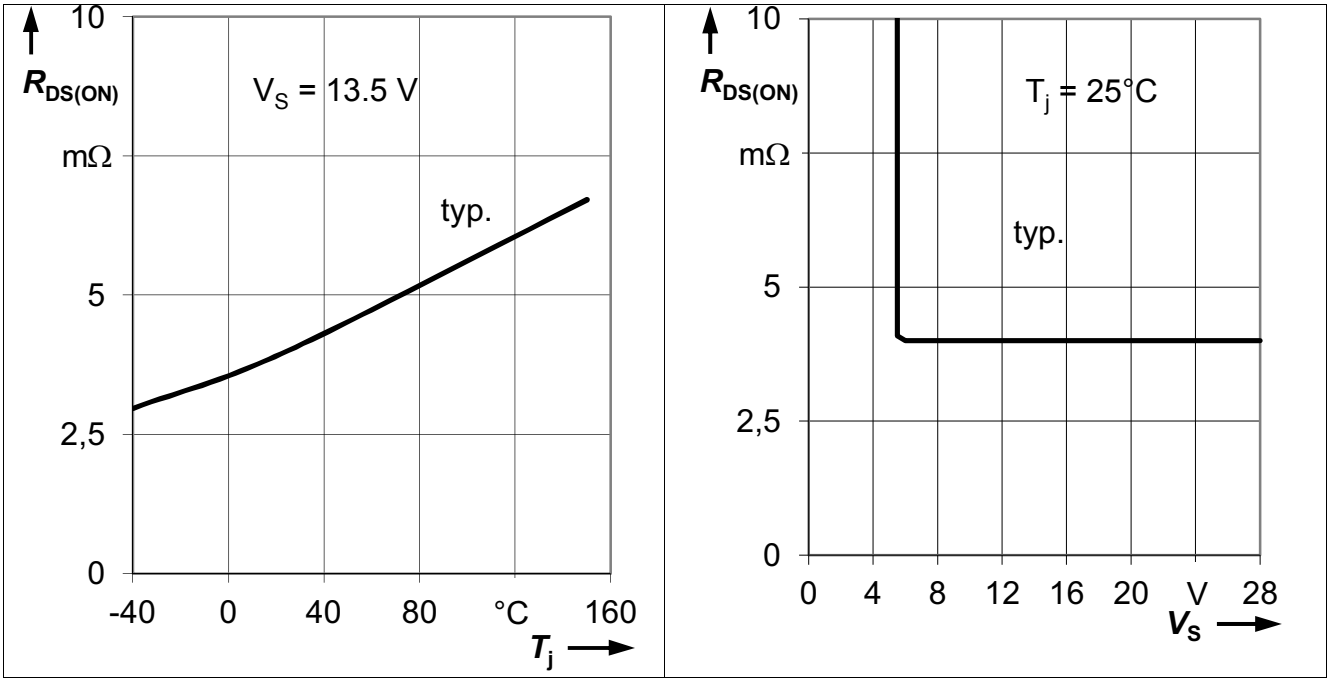


Figure 8 Typical On-State Resistance

5.1.2 Output Timing

The power stage is designed for high side configuration (**Figure 10**).

The BTS50040-2SFA offers 4 pre-defined switching behavior for the power stage. Defined slew rates as well as edge shaping support PWM'ing of the load while achieving lowest EMC emission at minimum switching losses. The different switching speeds can be selected by using slew rate selector pins SRS0 and SRS1. Please look at chapter **Chapter 6.1 Electrical Characteristics Table** parameter **$(dV/dt)_{ON}$** and **$-(dV/dt)_{OFF}$** on page **24** on setting up SRS0 and SRS1.

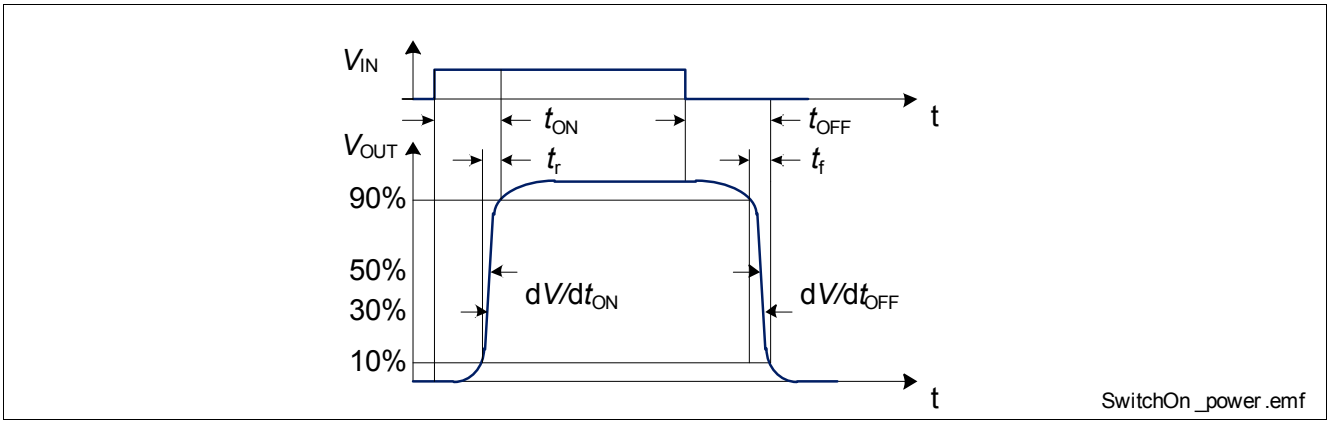


Figure 9 Switching a Load (resistive)

5.1.3 Output Inductive Clamp

When switching off inductive loads, the output voltage V_{OUT} drops below ground potential due to the inductive properties of the load ($-di_L/dt = -v_L/L$; $-V_{OUT} \cong -V_L$).

To prevent destruction of the device, there is a voltage clamp mechanism implemented that keeps the voltage drop across the device at a certain level. At nominal battery voltage the output is clamped to $V_{OUT(CL)}$. At over voltages

the output is clamped to $V_{DS(CL)}$. See **Figure 10** and **Figure 11** for details. The maximum allowed load inductance is limited.

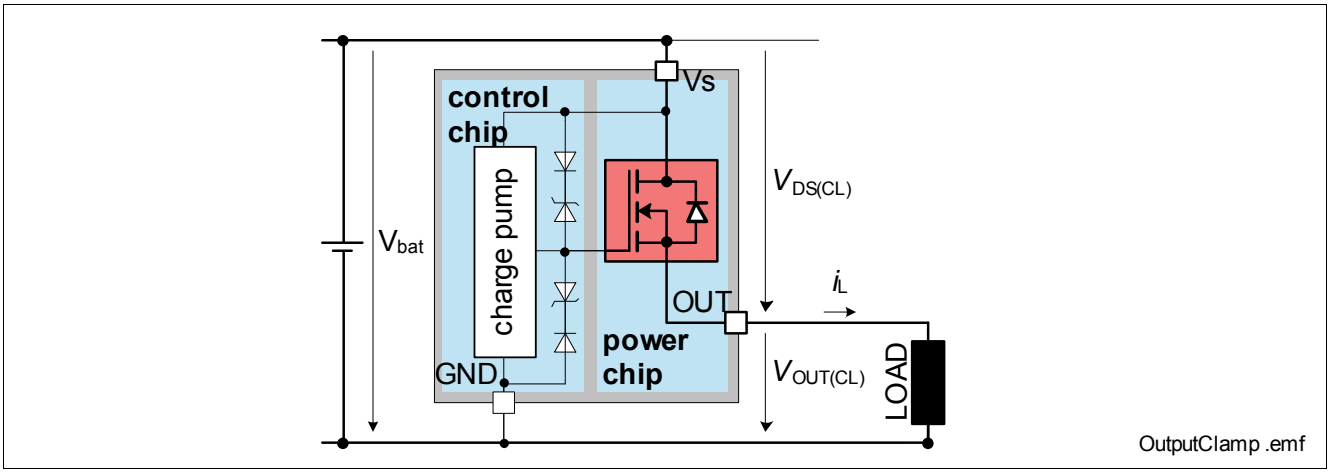


Figure 10 Output Clamp

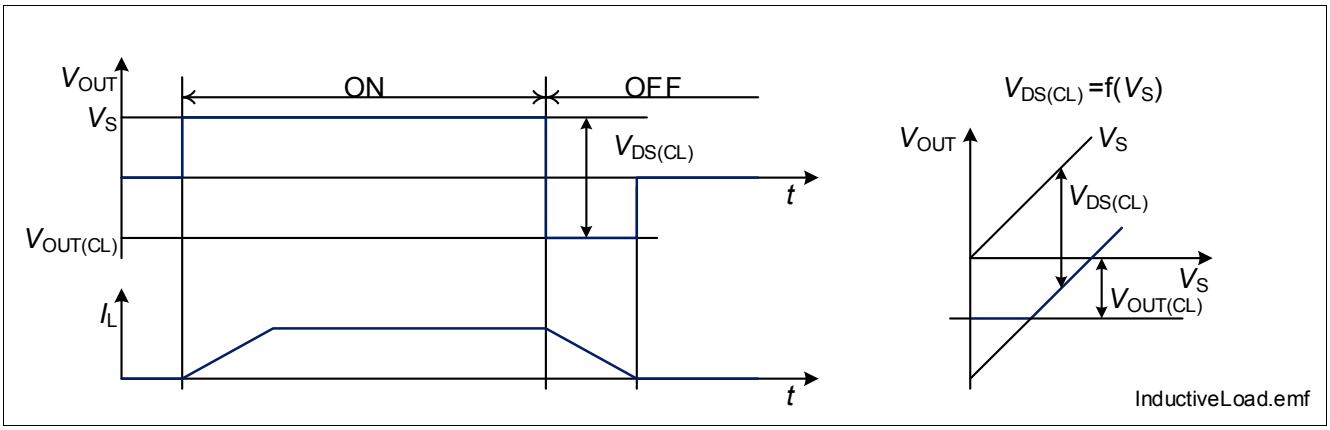


Figure 11 Switching an Inductance

Maximum Load Inductance

While de-energizing inductive loads, energy has to be dissipated in the BTS50040-2SFA. This energy can be calculated by the following equation:

$$E_A = (V_S + |V_{OUT(CL)}|) \cdot \left[\frac{-|V_{OUT(CL)}|}{R_L} \cdot \ln\left(1 + \frac{R_L \cdot I_L}{|V_{OUT(CL)}|}\right) + I_L \right] \cdot \frac{L}{R_L}$$

In the event of de-energizing very low ohmic inductances ($R_L \approx 0$) the following, simplified equation can be used:

$$E_A = \frac{1}{2} L I_L^2 \cdot \frac{|V_{DS(CL)}|}{|V_{DS(CL)}| - V_S}$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 4** for the maximum allowed energy dissipation.

5.1.4 Inverse Operation Capability

The BTS50040-2SFA can be operated in inverse load current condition (V_{OUT} > V_S). Inverse load current is a negative load current, e.g. caused by a load operating as a generator. The device does not block the current flow during inverse mode.

In ON condition, a voltage drop across the activated channel of $-V_{ON(INV)} = -I_L \times R_{DS(ON)}$ can be observed. As long as the inverse current does not exceed |-IL|<|-IL(inv)|, the logic will operate normally.

In OFF condition, a voltage drop across the inactive channel of $-V_{OFF(INV)} = f(-I_L)$ can be observed. Also the accuracy of the sense function of the non-inverted channel may not be within specified range under this condition.

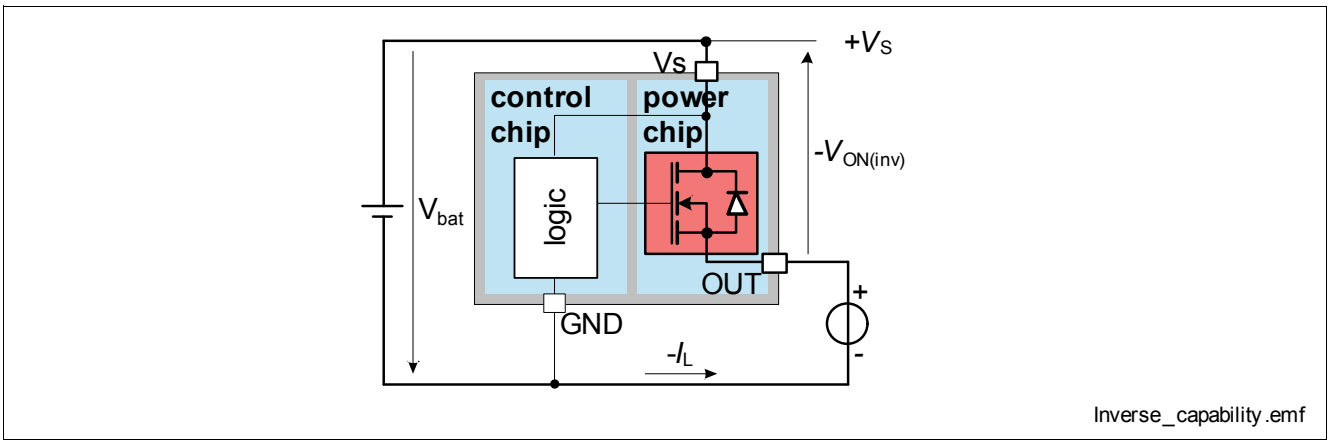


Figure 12 Inverse current capability

Note: Activation of any protection mechanism will not block the current flow. Over temperature detection and current sense is not functional during inverse mode.

5.2 Input Circuit

Figure 13 shows the input circuit of the BTS50040-2SFA. The circuitry is equivalent for all input pins of the device (IN0, IN1, SEN0, SEN1, SRS0, SRS1). The input resistor to ground ensures that the input signal is low in case of open input pin. The z-diode protects the input circuit against ESD pulses. The function which is linked to each pin can be found in **Chapter 3.2** "**Pin Definitions and Functions**".

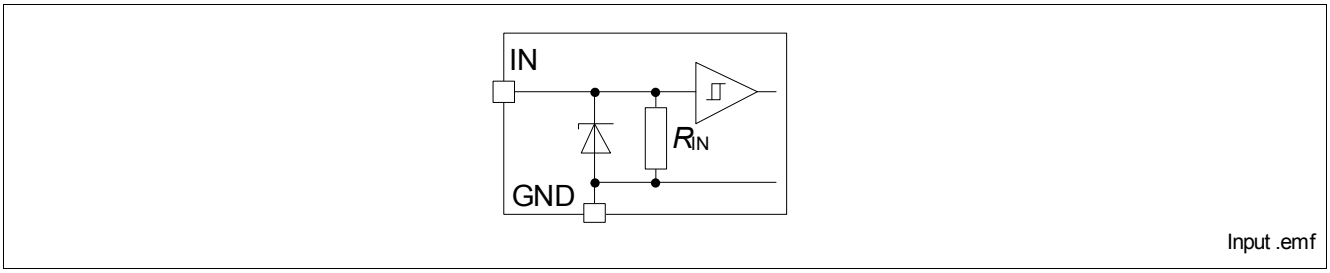


Figure 13 Input Circuit

5.3 Protection Functions

The BTS50040-2SFA provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

5.3.1 Infineon® INTELLIGENT LATCH - fault acknowledge and latch reset

The BTS50040-2SFA provides Infineon® INTELLIGENT LATCH to avoid permanent resetting of a protective, latched switch off in PWM applications, in case of overtemperature or short circuit. To reset a latched protective switch off the fault has to be acknowledged by a HIGH signal at both sense enable pins SEN0 and SEN1 (RESET = (SEN0&SEN1=HIGH)), or by an undervoltage reset of the internal logic supply.

Please refer to **Figure 14** and **Figure 15** for details. To avoid interferrence of reset signal and protective switch-off, either IN0 and IN1 must be low during reset signal, or reset signal must be shorter than 50µs ((SEN0&SEN1=HIGH) only for t< 50µs).

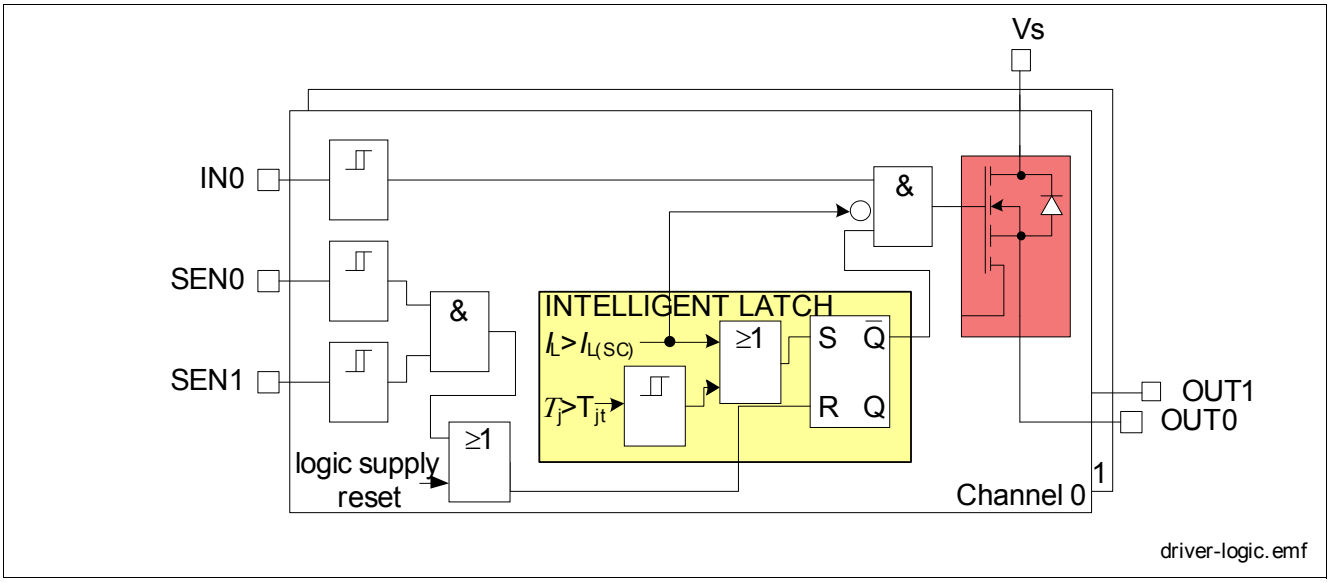


Figure 14 Driver logic

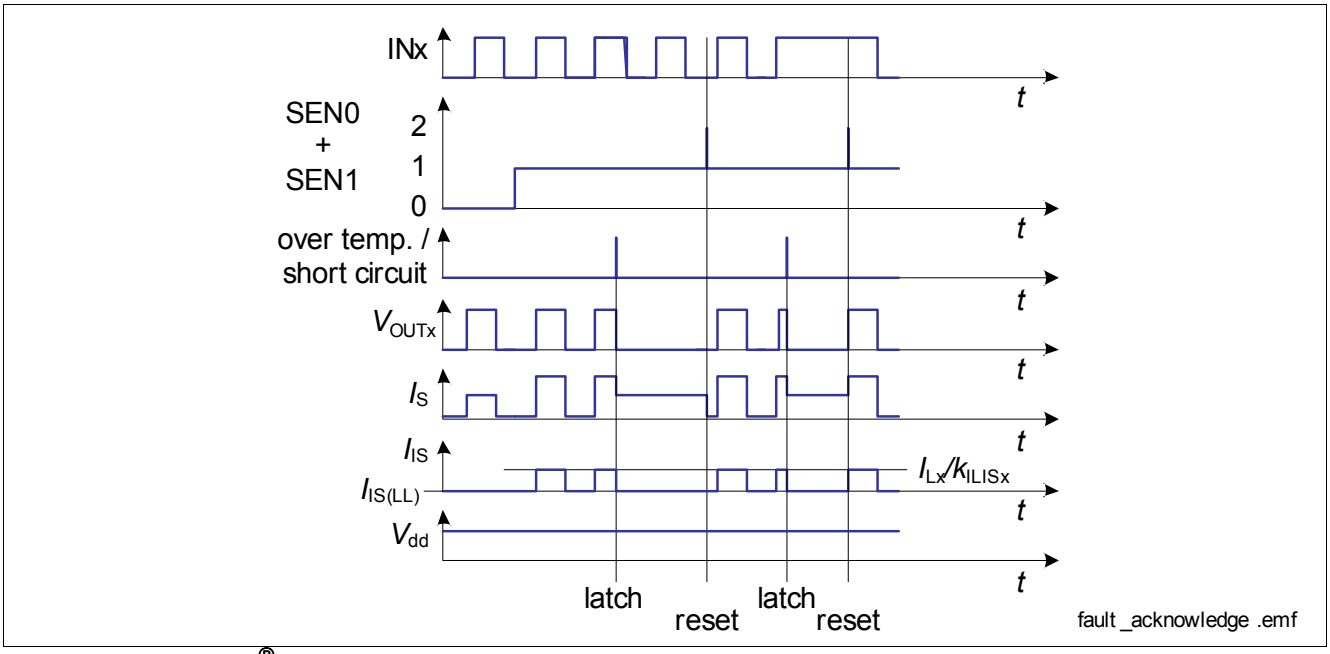


Figure 15 Infineon® INTELLIGENT LATCH - fault acknowledge and latch reset

5.3.2 Short Circuit and Overtemperature Protection

The internal logic permanently monitors the load current I_L and the junction temperature T_j. In the event the short circuit shutdown threshold ($I_{L(SC)}$) or overtemperature shutdown threshold (T_{jt}) is exceeded, the device will switch off the affected channel immediately. Short circuit shutdown and overtemperature shutdown will be latched. Please refer to **Figure 16** for details. A RESET signal will override temperature shutdown hysteresis even if $T_j > T_{jt} - \Delta T_j$. See also **Chapter 5.3.3**.

In case of a short circuit between OUT and ground, an impedance between V_{bat} and V_S pin of the device may cause the device's supply voltage to drop below $V_{S(UV)ON} - \Delta V_{S(UV)}$ before short circuit shutdown threshold is reached. In that case, device turns off in undervoltage. If V_S drops below 4.5V before device has switched off, channels will be deactivated by passive gate discharge, which may take several milliseconds. In this transient condition of passive gate discharge during $V_S < 4.5V$, overtemperature shutdown is not functional. The BTS50040-2SFA restarts automatically from undervoltage when $V_S > V_{S(UV)ON}$ and delay time $t_{delay(UV)}$ has passed and no fault signal was latched.

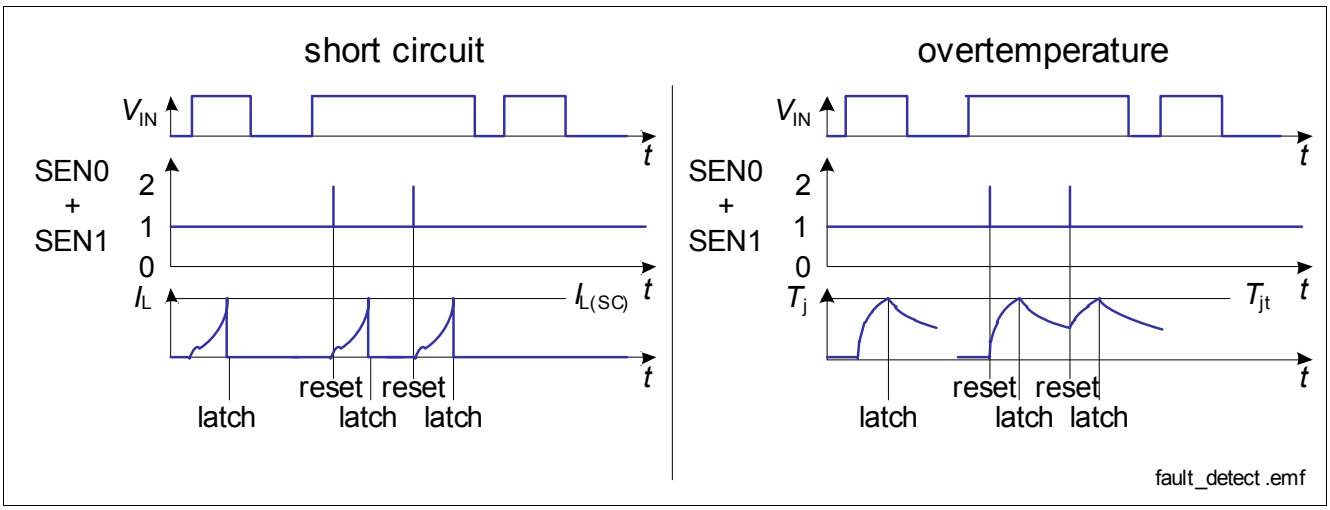


Figure 16 Shutdown by short circuit current and overtemperature detection

5.3.3 Reverse Polarity Protection - ReverSave™

The device can not block a current flow in reverse battery condition. In order to minimize power dissipation, the device offers ReverSave™ functionality. Under reverse polarity condition, the output stage will be switched on, provided a sufficient voltage $-V_S$ is applied between pin Vs and pin GND. Please refer to **Figure 17** for details.

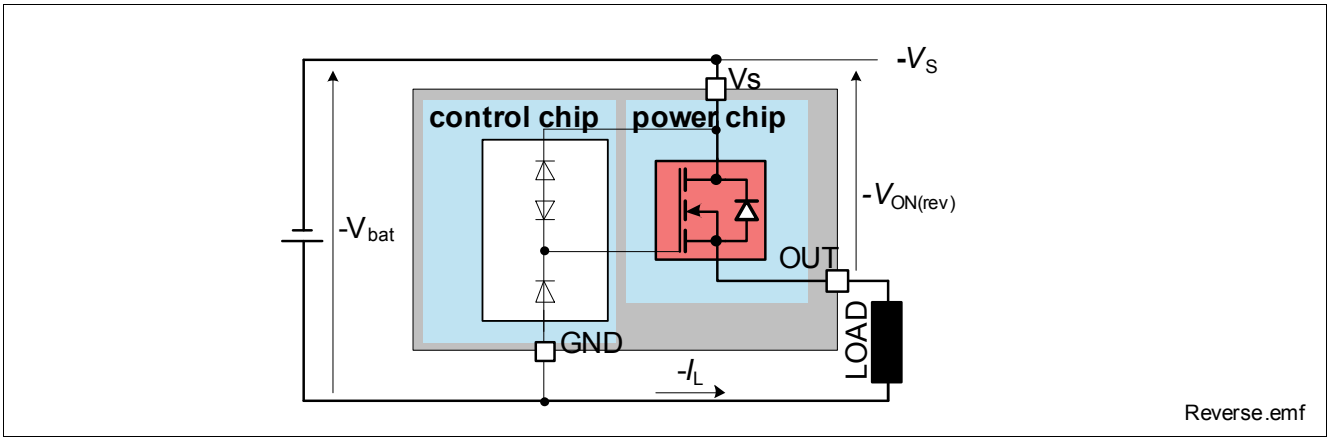


Figure 17 Reverse battery protection

Use the following formula for estimation of overall power dissipation $P_{diss(rev)}$ in reverse polarity mode.

$$P_{diss(rev)} \approx R_{ON(rev)} \cdot I_L^2$$

Note: No protection mechanism is active during reverse polarity. The control chip is not functional. Potentials of logic pins can become negative. Affected pins have to be protected by means of series resistors.

5.3.4 Undervoltage shutdown and restart

The BTS50040-2SFA is supplied by two supply voltages V_S and V_{dd}. With applied V_S and V_{dd} voltages the channels can be activated via the according input pins. The device is in normal operation mode.

The V_S supply line is used by the driver circuitry and the power stage, providing supply for analog and logic circuitry, at normal conditions ($V_{S(NOM)}$).

If V_S is below $V_{S(NOM)}$, the internal logic supply is switched over to V_{dd} line. There is a power-on reset function implemented for the internal logic supply. After start-up of the logic power supply (via V_S or V_{dd}.), all latches are reset.

If V_{dd} is close to $V_{dd(RESET)}$, the switch-over may activate logic supply reset of the INTELLIGENT LATCH function. See **Figure 1** and **Figure 14**. A capacitor between V_{dd} and GND is recommended for filtering purpose as shown in **Figure 23**.

If V_S drops below $V_{S(UV)ON}$ - $\Delta V_{S(UV)}$, power outputs of BTS50040-2SFA will be deactivated. If an input pin INx is HIGH and V_{dd} = $V_{dd(NOM)}$, the power outputs will restart automatically when V_S increases to $V_{S(UV)ON}$ and a delay time of $t_{delay(UV)}$ has passed. Please see **Figure 18** for details. In the time between undervoltage shutdown and undervoltage restart, IS signal is deactivated, with leakage current only.

Stand-by mode is entered as soon as V_S voltage is available, but no V_{dd} supply voltage is applied. If the V_{dd} voltage is applied too, but no channel is switched on, the device is in idle mode.

If V_{dd} is applied before V_S is available, a reset via SEN0=SEN1=HIGH may be necessary for enabling the power stages.

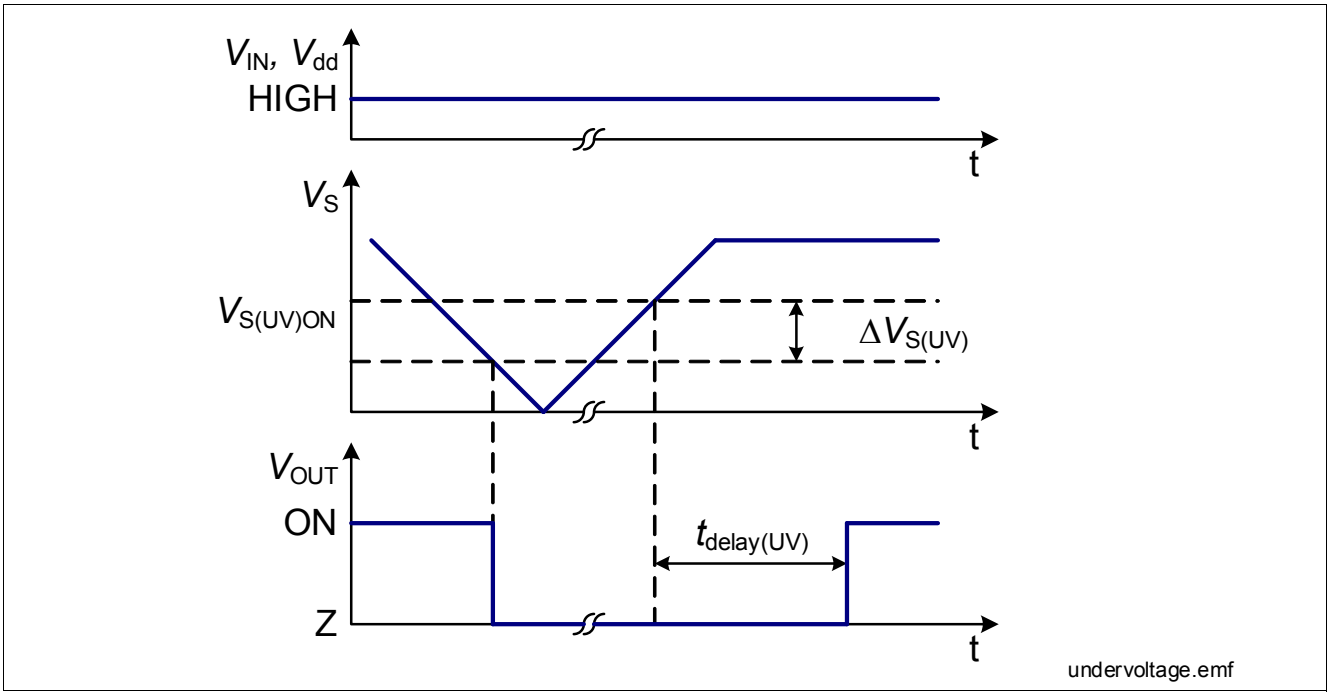


Figure 18 Undervoltage shutdown and restart

5.3.5 Loss of Ground Protection

In case of complete loss of the device ground connections, but load still being connected to ground, the BTS50040-2SFA securely changes to or remains in OFF state.

5.3.6 Loss of Load Protection, Loss of V_S Protection

In case of loss of load with charged primary inductances the maximum supply voltage has to be limited. It is recommended to use a Z-diode, a varistor (V_{Za} < 42 V) or V_S clamping power switches with connected loads in parallel.

In case of loss of V_S connection with charged inductive loads, a current path with load current capability has to be provided, to demagnetize the charged inductances. It is recommended to use a diode, a Z-diode or a varistor (V_{Zb} < 16 V, V_{ZL}+V_D < 16 V,).

For higher clamp voltages currents through all pins have to be limited according to the maximum ratings. Please refer to **Figure 19** for details.

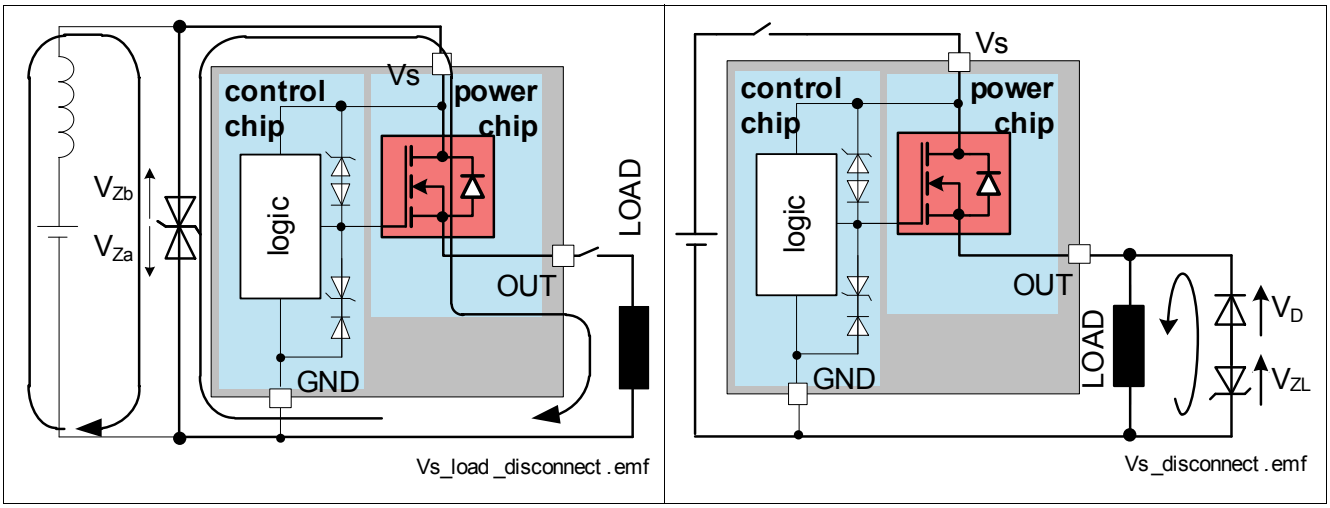


Figure 19 Loss of V_S

In case of complete loss of V_S the BTS50040-2SFA remains in OFF state.

5.4 Diagnostic Functions

For diagnosis purposes, the BTS50040-2SFA provides an analog load current sense signal at the pin IS.

5.4.1 Sense Enable

Providing a low signal at the SENx pin will disable the reporting of channel x. The pin IS will be set to tri-state mode when both SEN pins are low or high. A HIGH signal at SEN0 and SEN1 at the same time resets a preceding latched output condition. Please see **Figure 15**, **Figure 20** and **Table 1 Truth Table for Power Stages** for details.

In order to achieve minimum standby current, SEN0 and SEN1 have to be low level.

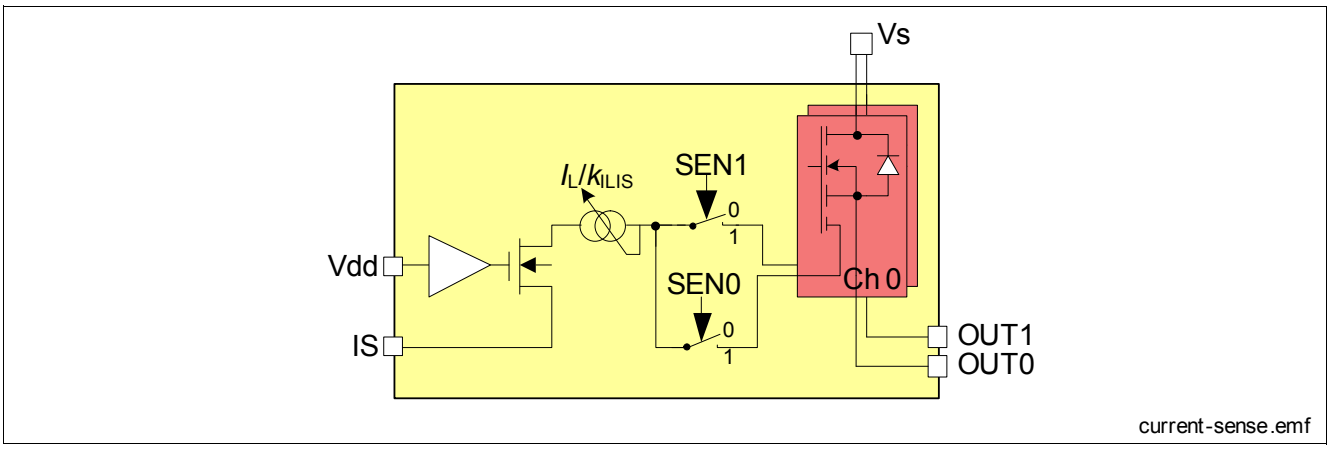


Figure 20 Current sense

Table 2 Truth Table for Sense Enable

SEN0	SEN1	IS	Comment
H	H	$I_{IS(LL)}$	fault latch reset
L	H	$I_{IS}=I_{L1}/k_{ILIS}$	channel 1
H	L	$I_{IS}=I_{L0}/k_{ILIS}$	channel 0
L	L	$I_{IS(LL)}$	–

L = Low Level, H = High Level

5.4.2 Diagnosis during ON

During normal operation, an enabled IS pin provides a sense current, which is proportional to the load current as long as $V_{IS} < V_S$ - 5 V and as long as $I_{IS}*R_{IS}<V_{IS(lim)}$. The ratio of the output current is defined as $k_{ILIS}=I_L/I_{IS}$. During switch-on sense current is provided after a sense settling time $t_{sIS(ON)}$. During inverse operation and switch-off no current is provided.

The output sense current is limited to $I_{IS,lim}$. Please refer to **Figure 21** for details.

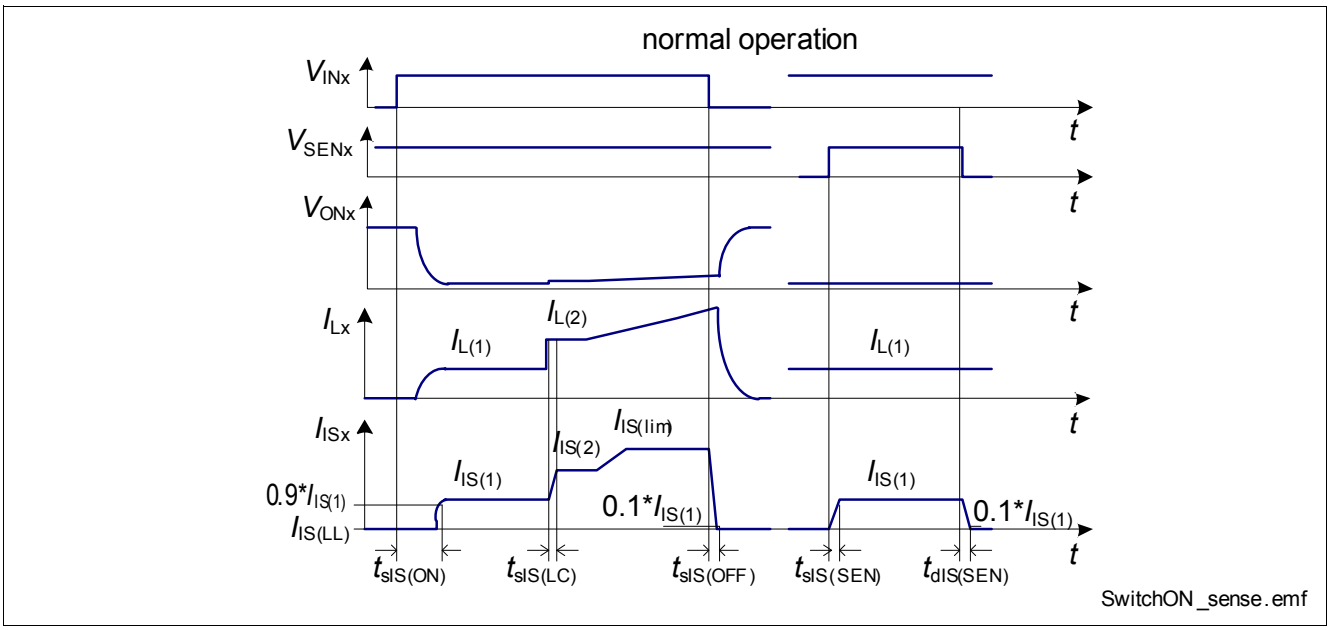


Figure 21 Timing of Diagnosis Signal in ON-state

The accuracy of the provided current sense ratio ($k_{ILIS} = I_L / I_{IS}$) depends on the load current. Please refer to **Figure 22** for details. A typical resistor R_{IS} of 1 kΩ is recommended (see also **Chapter 5.3.5**).

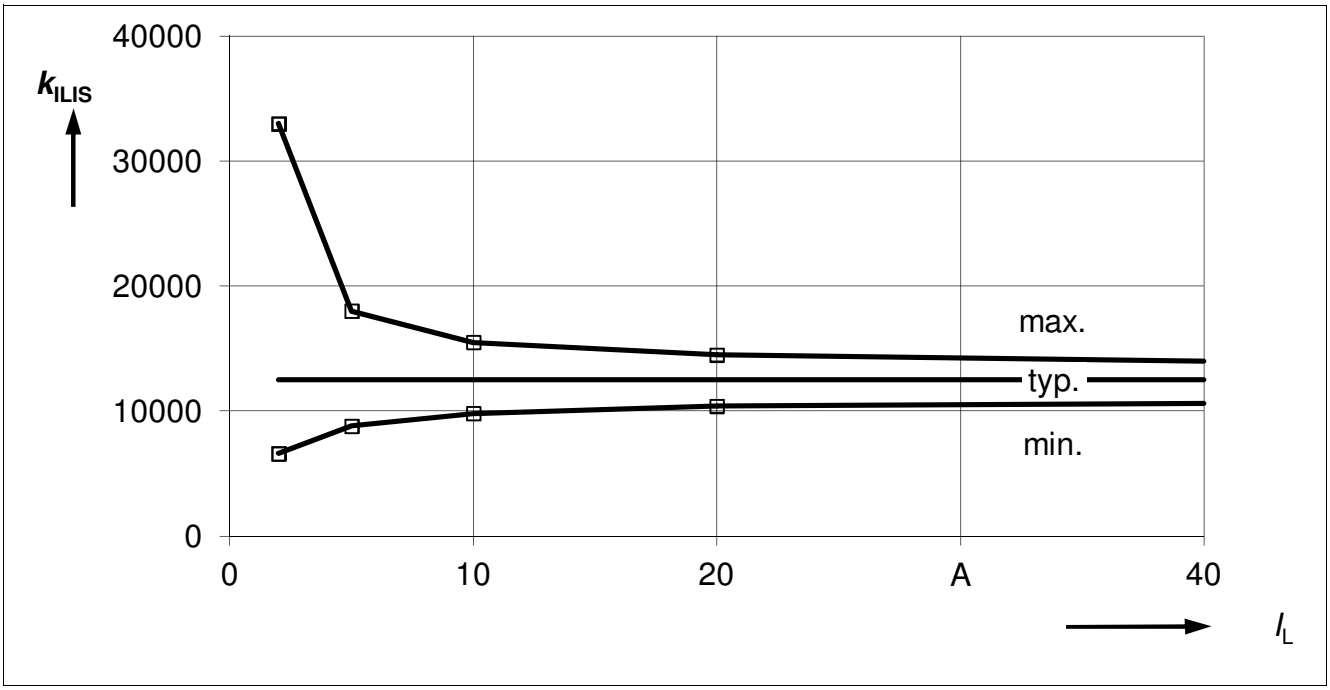


Figure 22 Current sense ratio k_{ILIS}[1)]

1) The curves show the behavior based on characterization data. The marked points are described in this Datasheet in **Chapter 6.1** (Position **6.1.26**).

6 Electrical characteristics

6.1 Electrical Characteristics Table

Note: Characteristics show the deviation of parameters at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

V_S = 9 V to 16 V, V_{dd} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_S = 13.5 V, T_j = 25 °C, V_{dd} = 5 V

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output characteristics							
6.1.1	On-state resistance per channel	$R_{DS(ON)}$				mΩ	V_{IN}=5V, I_L=+/-10A
	T_j=25°C[1)]		–	4.0	–		
	T_j=150°C		–	6.5	8.2		
	V_S=6V, T_j=25°C[1)]		–	7.9	–		
	V_S=6V, T_j=150°C		–	10	16		
6.1.2	Nominal load current per channel[1)2)]	$I_{L(nom)}$	–	11	–	A	T_A = 85 °C $T_j \leq$ 150 °C
6.1.3	Output leakage current per channel	$I_{L(OFF)}$				µA	V_{IN0} = V_{IN1} = 0V V_{OUT}=0V
	T_j = -40 °C, T_j = 25 °C[1)]		–	2	5		
	$T_j \leq$ 85 °C [1)]		–	2	5		
	T_j = 150 °C		–	7	45		
6.1.4	Output clamp during switch-off	$-V_{OUT(CL)}$				V	$V_{OUT} \geq V_S - V_{DS(CL)}$[3)]
	I_L = 40 mA		16	18	20		
	I_L = 10 A [1)]		16	20	25		
6.1.5	Output clamp during over voltage	$V_{DS(CL)}$				V	$V_{DS} \leq V_S - V_{OUT(CL)}$[3)]
	I_L = 40 mA		42	50	–		
	I_L = 20 A [1)]		42	51	–		
6.1.6	Inverse operation output voltage drop	$-V_{OFF(inv)}$				mV	V_{IN}=0V I_L = -10 A
	T_j=25°C[1)]		–	800	1000		
	T_j=150°C		–	650	850		
6.1.7	Inverse current capability[1)]	$-I_{L(inv)}$	25	–	–	A	–
Timings							
6.1.8	Turn-on time to 90% V_S	t_{ON}				µs	V_S = 13.5 V R_L = 2.7 Ω
	SRS1 = 1, SRS0 = 1		–	95	190		
	SRS1 = 1, SRS0 = 0		–	120	240		
	SRS1 = 0, SRS0 = 1		–	170	340		
	SRS1 = 0, SRS0 = 0		–	320	640		
6.1.9	Turn-off time to 10% V_S	t_{OFF}				µs	V_S = 13.5 V R_L = 2.7 Ω
	SRS1 = 1, SRS0 = 1		–	55	110		
	SRS1 = 1, SRS0 = 0		–	70	140		
	SRS1 = 0, SRS0 = 1		–	100	200		
	SRS1 = 0, SRS0 = 0		–	170	340		

V_S = 9 V to 16 V, V_{dd} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_S = 13.5 V, T_j = 25 °C, V_{dd} = 5 V

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.10	Slew rate On 30↗50% V_{OUT}	$(dV/dt)_{ON}$				V/µs	V_S = 13.5 V R_L = 2.7 Ω
	SRS1 = 1, SRS0 = 1		–	0.40	0.80		
	SRS1 = 1, SRS0 = 0		–	0.24	0.48		
	SRS1 = 0, SRS0 = 1		–	0.14	0.28		
	SRS1 = 0, SRS0 = 0		–	0.07	0.16		
6.1.11	Slew rate Off 50↘30% V_{OUT}	$-(dV/dt)_{OFF}$				V/µs	V_S = 13.5 V R_L = 2.7 Ω
	SRS1 = 1, SRS0 = 1		–	0.42	0.84		
	SRS1 = 1, SRS0 = 0		–	0.31	0.62		
	SRS1 = 0, SRS0 = 1		–	0.20	0.42		
	SRS1 = 0, SRS0 = 0		–	0.09	0.21		
Power supply							
6.1.12	Stand-by current	$I_{S(OFF)}$				µA	4) V_{IN0} = V_{IN1} = 0V V_{SEN0} = V_{SEN1} = 0V V_{dd} = 0V no fault condition
	T_j = -40 °C, T_j = 25 °C 1)		–	5	12		
	$T_j \leq$ 85 °C 1)		–	5	12		
	T_j = 150 °C		–	35	115		
6.1.13	Idle current for whole device with loads, both channel OFF	$I_{S(idle)}$	–	800	–	µA	4) V_{IN0} = V_{IN1} = 0V V_{SEN0} = V_{SEN1} = 0V V_{dd} = 5V no fault condition
6.1.14	Logic supply reset threshold 1)	$V_{dd(RESET)}$	–	–	4.5	V	V_S = 0V
6.1.15	Logic supply current	I_{dd}				µA	V_{IN0} = V_{IN1} = 5V V_{SEN0} = V_{SEN1} = 5V V_{dd} = 5V
	V_S = 9 V to 16 V		–	50	150		
	V_S = 6V		–	275	800		
6.1.16	Operating current for whole device active	I_{GND}	–	10	20	mA	V_{IN0} = V_{IN1} =5V V_{SEN0} = V_{SEN1} = 5V V_{dd} = 5V, I_L = 0A
Input characteristics							
6.1.17	L-input level	$V_{IN(L)}$	-0.3	–	1.0	V	–
6.1.18	H-input level	$V_{IN(H)}$	2.0	–	5.5	V	–
6.1.19	input hysteresis	$V_{IN(hys)}$	–	175	–	mV	1)
6.1.20	input pull down resistor	R_{IN}	50	100	200	kΩ	–
Over-Load Protection							
6.1.21	Short circuit shutdown threshold	$I_{L(SC)}$				A	–
	T_j = -40°C		130	180	230		
	T_j = 150°C		90		155		
6.1.22	Thermal shutdown temperature	T_{jt}	150	170 1)	–	°C	–

V_S = 9 V to 16 V, V_{dd} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_S = 13.5 V, T_j = 25 °C, V_{dd} = 5 V

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reverse Battery							
6.1.23	On-State resistance in case of reverse polarity V_S=-8V[1)] V_S=-12V	$R_{ON(rev)}$	 – –	 10 7.9	 – –	mΩ	I_L = -10A T_j = 150°C
Diagnosis signal							
6.1.24	Current sense ratio, static on-condition I_{Lx}=20A I_{Lx}=10A I_{Lx}=5A I_{Lx}=2A V_{INx} = 0 (e.g. during de energizing of inductive loads)	k_{ILIS}	 10400 9800 8800 6600 disabled	12500	 14500 15500 18000 33000	–	$V_{IS} < V_{IS(lim)}$, $V_{IS} < V_S$ - 5 V V_{INx} = High V_{SENx} = High V_{SENy} = Low $I_{Ly} \geq$ 0A
6.1.25	Current sense voltage limitation[1)]	$V_{IS(lim)}$	0.92 x V_{dd}	V_{dd}	1.08 x V_{dd}	V	–
6.1.26	Sense saturation current [1)]	$I_{IS(lim)}$	3.5	6	10	mA	V_{SENx} = 5 V $V_{IS} < V_S$ - 5 V
6.1.27	Current sense leakage current	$I_{IS(LL)}$	–	0.1	1	µA	V_{INx}=V_{SENx}=0V
6.1.28	Current sense offset current	$I_{IS(LH)}$	–	5	100	µA	V_{INx}=V_{SENx}=5V $I_{Lx} \leq$ 0A
6.1.29	Current sense settling time to 90% $I_{IS\_stat.}$ after switch-on[1)]	$t_{sIS(ON)}$	–	350	1000	µs	V_S = 13.5V V_{SENx} = 5 V R_L = 2.7 Ω
6.1.30	Current sense settling time to 10% $I_{IS\_stat.}$ after switch-off [1)]	$t_{sIS(OFF)}$	–	50	100	µs	
6.1.31	Current sense settling time to 90% $I_{IS\_stat.}$ after changing load [1)]	$t_{sIS(LC)}$	–	50	100	µs	V_S = 13.5V V_{SENx} = 5 V I_L = 10↗20A
6.1.32	Current sense settling time to 90% $I_{IS\_stat.}$ after sense enable [1)]	$t_{sIS(SEN)}$	–	7	35	µs	V_S = 13.5V V_{SENx} = 5 V R_L = 2.7 Ω
6.1.33	Current sense deactivation time to 10% $I_{IS\_stat.}$ after sense disable [1)]	$t_{dIS(SEN)}$	–	7	35	µs	
Undervoltage shutdown and restart							
6.1.34	Undervoltage restart threshold	$V_{S(UV)ON}$	–	5.5	6	V	V_{INx} = High
6.1.35	Undervoltage hysteresis[1)]	$\Delta V_{S(UV)}$	–	10	–	mV	V_{INx} = High
6.1.36	Undervoltage restart delay time[1)]	$t_{delay(UV)}$	10	18	30	ms	V_{INx} = High

1) Not subject to production test, specified by design
2) according JESD51_7, FR4 2s2p board, 76.2 x 114.3 x 1.6 mm, 2x70µm Cu, 2x35µm Cu.
3) See **Figure 11**.
4) In case of protective switch-off STANDBY is only reached if the fault was acknowledged by a RESET signal (SEN0&SEN1=High). See also **Chapter 5.3.1** for details.

7 Application schematic

Figure 23 shows an example for an application schematic.

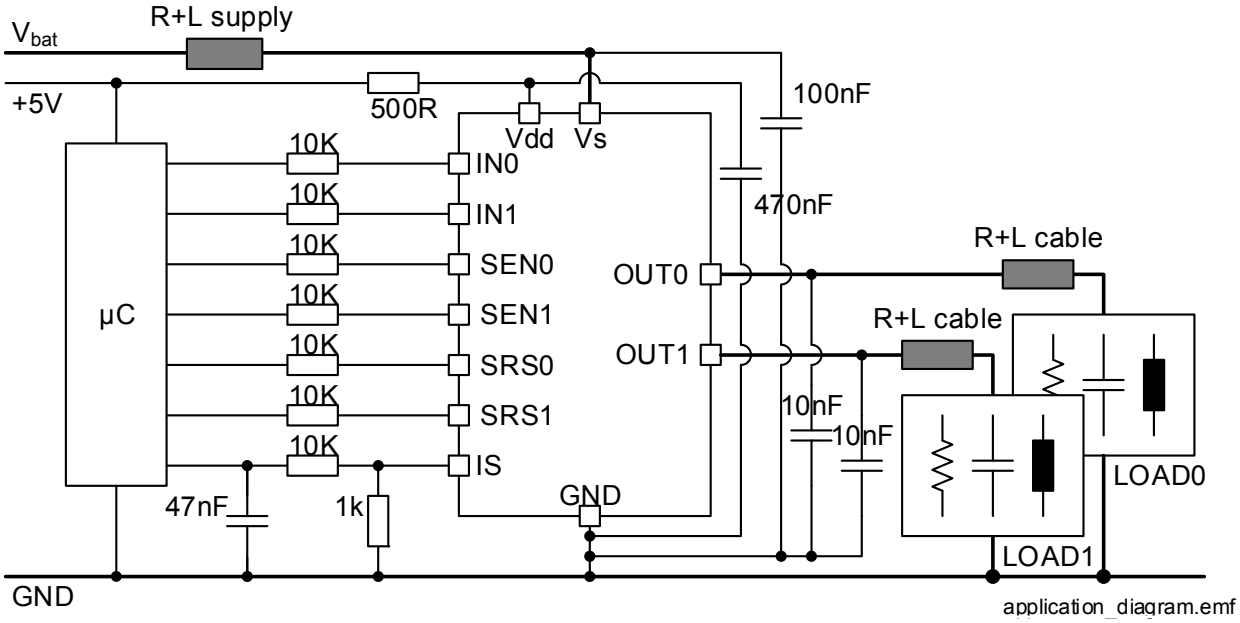


Figure 23 application example

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

7.1 Hints for PCB layout

- Handling of NC pins: It is recommended to connect all NC pins on a defined potential. E.g. pin 6 and pin 36 could be connected to GND potential.
- EMC filter cap between Vs and GND, Vdd and GND: It is recommended to place the filter cap as close as possible to the device to minimize the inductance of the loop.
- GNDR pin: in case of open GNDR pin, transient voltage disturbances may lead to reduction of $t_{delay(UV)}$ to typically 1.9ms.
- The resistors connecting µC and input pins INx, SENx, SRSx, are recommended for protection of pins against fast electrical transients.
- Ground shift: It is recommended to avoid a ground shift between µC ground and device pin GND of more than 0.3V during normal operation.

7.2 Further Application Information

- Please contact us to get the Pin FMEA
- Please contact us to get a test report on short circuit robustness according to AEC Q100-012
- For further information you may contact **http://www.infineon.com/**

8 Package Outlines

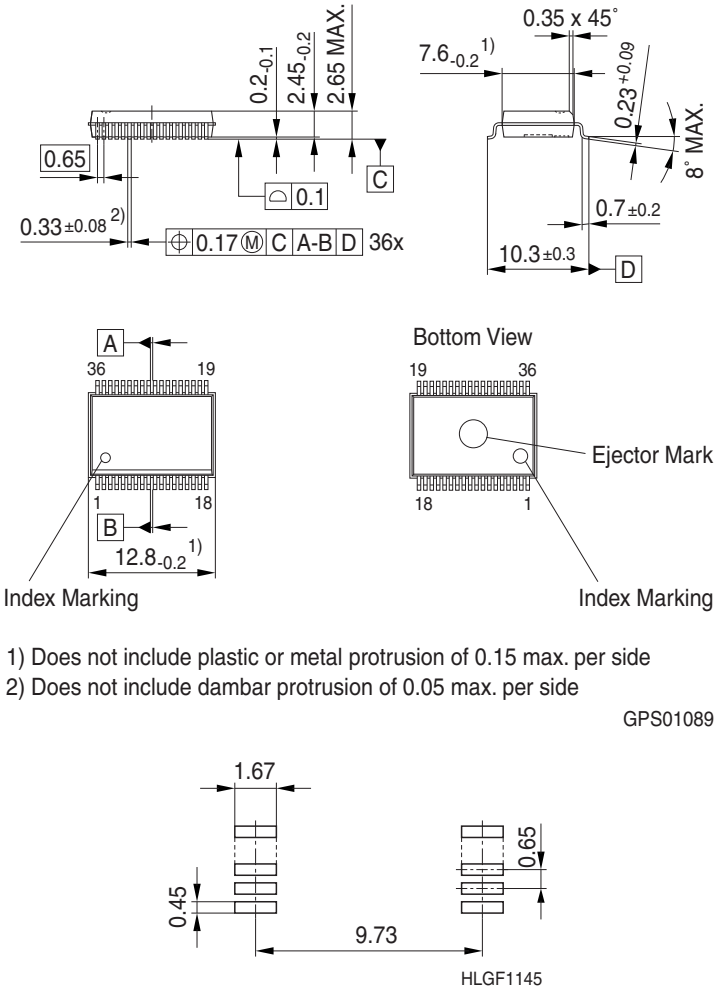


Figure 24 PG-DSO-36-44 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

9 Revision History

BTS50040-2SFA

Revision History: V2.0, 2016-02-02

Version	Date	Changes
DS V2.0	2016-02-02	Introduction of undervoltage shutdown and restart delay function **Chapter 4.1 Absolute Maximum Ratings**: parameter $V_{bat(SC)}$ set to maximum 24V for T_j = -40°C ... 150°C, condition description improved; parameter I_{GND} and I_{dd} minimum rating added; parameter V_{ESD1} and V_{ESD2} "ESD susceptibility" description updated; parameter V_{ESD2} tested according JEDEC JESD22-C101 **Chapter 5.1 Table 1 Truth Table for Power Stages**: undervoltage condition added **Chapter 5.3.2 Short Circuit and Overtemperature Protection** reworked; note on supply voltage breakdown during shortcircuit removed. **Chapter 5.3.4 Undervoltage shutdown and restart** reworked; desciption of undervoltage shutdown on Vs supply line added; **Chapter 3.2**: setting of SRS0 and SRS1 corrected **Chapter 6.1**: parameter t_{ON}, t_{OFF}, $(dV/dt)_{ON}$, $(dV/dt)_{OFF}$: setting of SRS0 and SRS1 corrected parameter I_{dd}: low voltage condition Vs=6V added parameter $I_{S(idle)}$ reduced to typically 800uA parameter $V_{S(UV)ON}$, $\Delta V_{S(UV)}$, $t_{delay(UV)}$ added parameter $t_{sIS(LC)}$ description of condition improved **Chapter 7 Application schematic**: **Figure 23** adding R+L_supply and R+L_cable, fitting to improved description of $V_{bat(SC)}$. **Chapter 7.1 Hints for PCB layout**: Hint on open GNDR pin added. Hint on filter capacitor Vdd to GND added.
DS V1.2	2012-11-30	**Chapter 6**: Specification limits for parameter k_{ILIS} tightened. **Figure 22** updated.
DS V1.1	2012-01-18	**Chapter 1**: Typing error corrected on **Page 1**, parameter $I_{L(SC)}$.
DS V1.0	2011-11-25	Initial version of datasheet

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