

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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J-FET INPUT LOW-POWER OPERATIONAL AMPLIFIER

DESCRIPTION

The μ PC4061 is a J-FET input low-power operational amplifier featuring low supply voltage operation from ± 2 V. Supply current is ten times smaller than μ PC4081 type J-FET input op-amp. With very low input bias current characteristics, the μ PC4061 is an excellent choice for hand-held measurement equipment and other low-power application circuits.

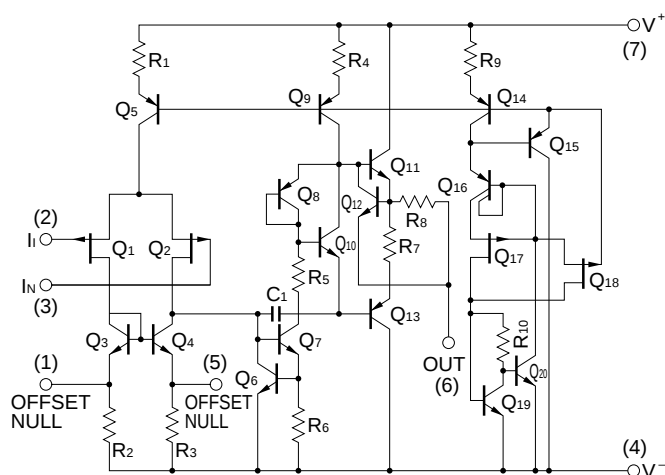
FEATURES

- Low supply current: 220 μA (TYP.)
- Very low input bias and offset currents
- Offset voltage null capability
- High input impedance...J-FET Input Stage
- Low supply voltage operation
- Output short circuit protection
- Internal frequency compensation

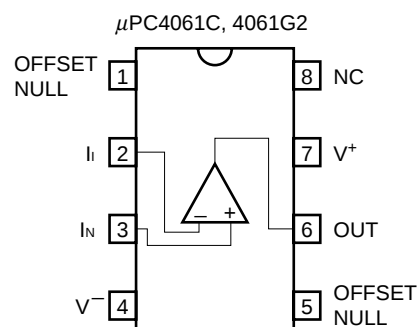
ORDERING INFORMATION

Part Number	Package
μ PC4061C	8-pin plastic DIP (7.62 mm (300))
μ PC4061G2	8-pin plastic SOP (5.72 mm (225))

EQUIVALENT CIRCUIT



PIN CONFIGURATION (Top View)



Remark NC : No Connection

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter		Symbol	Ratings	Unit
Voltage between V ⁺ and V ⁻ ^{Note 1}		V ⁺ - V ⁻	-0.3 to +36	V
Differential Input Voltage		V _{ID}	±30	V
Input Voltage ^{Note 2}		V _I	V ⁻ -0.3 to V ⁺ +0.3	V
Output Voltage ^{Note 3}		V _O	V ⁻ -0.3 to V ⁺ +0.3	V
Power Dissipation	C Package ^{Note 4}	P _T	350	mW
	G2 Package ^{Note 5}		440	mW
Output Short Circuit Duration ^{Note 6}			Indefinite	sec
Operating Ambient Temperature		T _A	-20 to +80	°C
Storage Temperature		T _{stg}	-55 to +125	°C

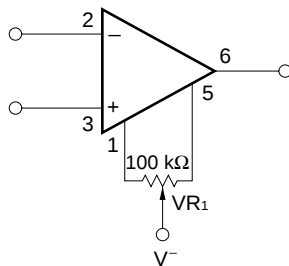
Notes 1. Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.
3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.
4. Thermal derating factor is -5.0 mW/°C when operating ambient temperature is higher than 55 °C.
5. Thermal derating factor is -4.4 mW/°C when operating ambient temperature is higher than 25 °C.
6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V [±]	±2		±16	V
Output Source Current	I _{O SOURCE}			5	mA
Output Sink Current	I _{O SINK}			3.5	mA
Capacitive Load (A _v = +1, R _f = 0 Ω)	C _L			100	pF

OFFSET VOLTAGE NULL CIRCUIT



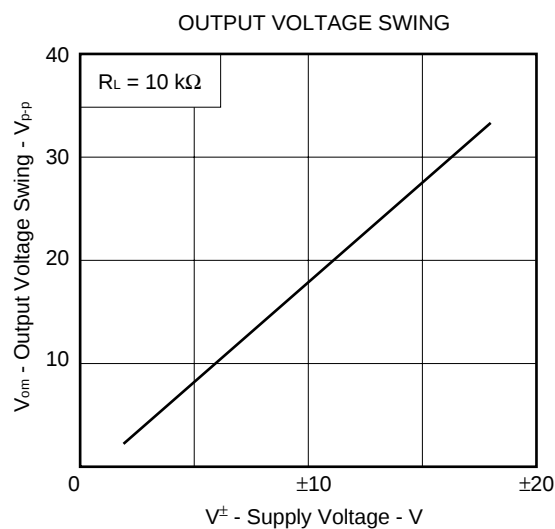
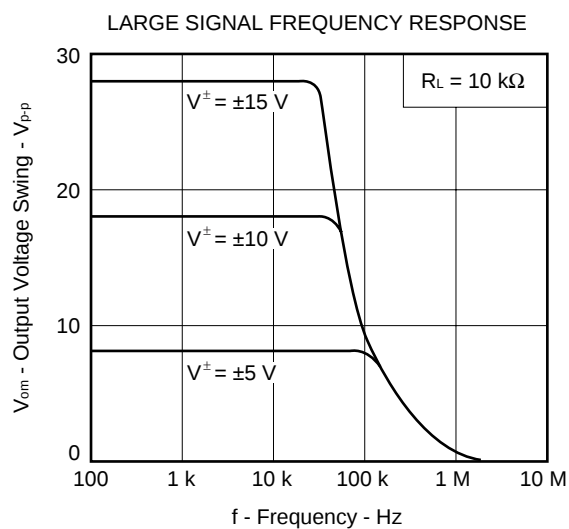
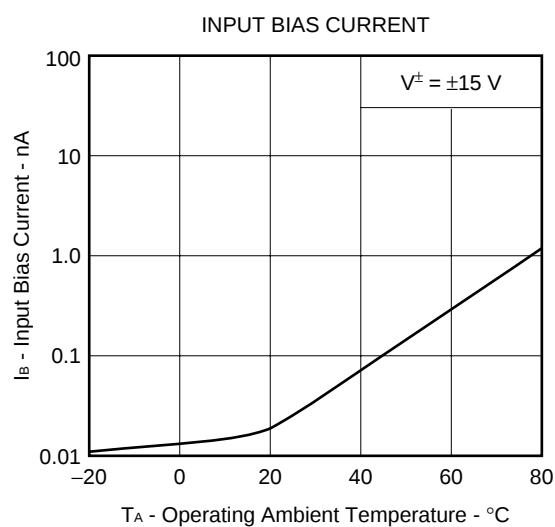
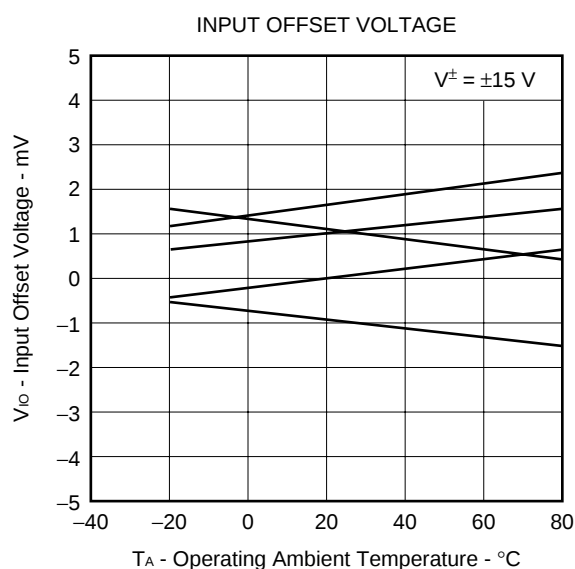
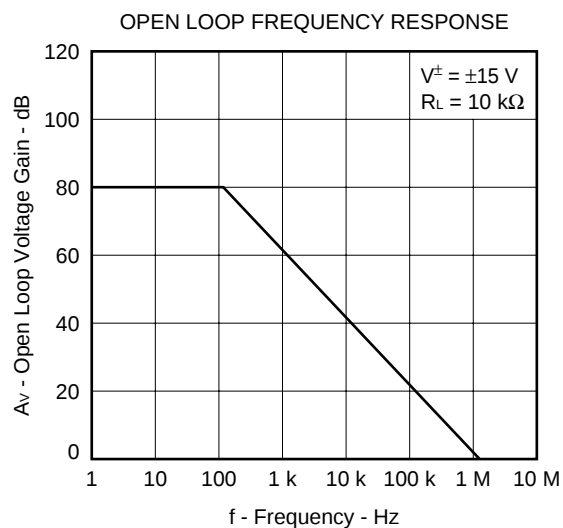
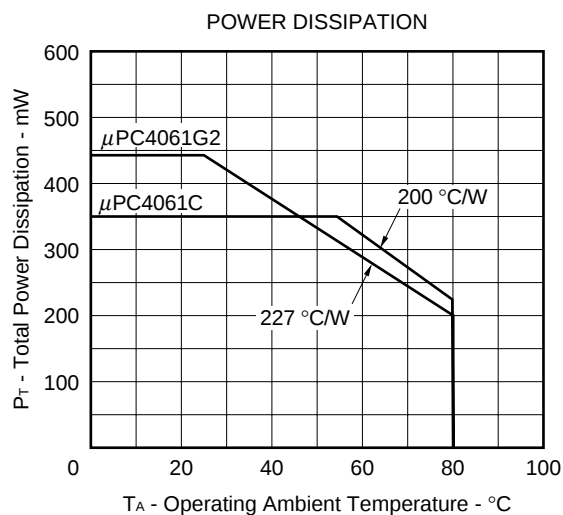
★ **Remark** The OFFSET NULL pins should be left open or connected to V⁻ via a resistor as shown in the left figure. Don't connect to any lines other than V⁻, otherwise malfunction, degradation, or failure may occur.

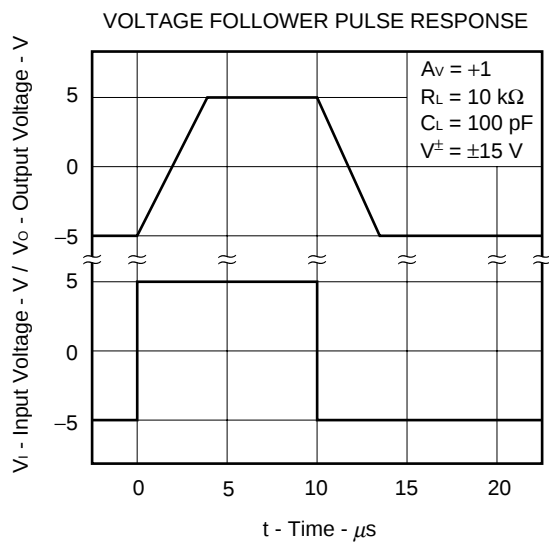
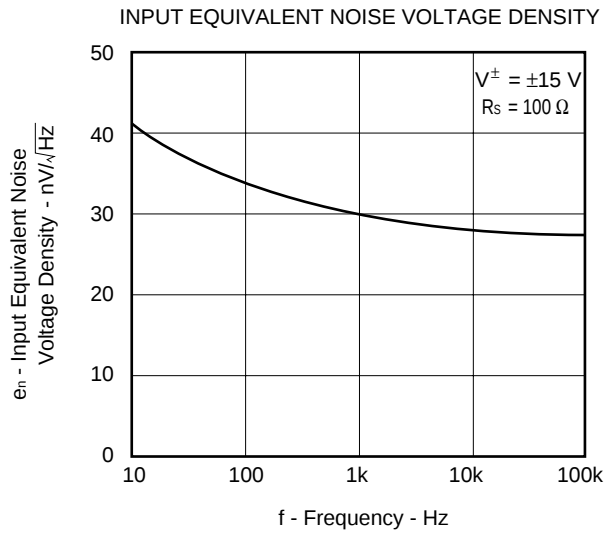
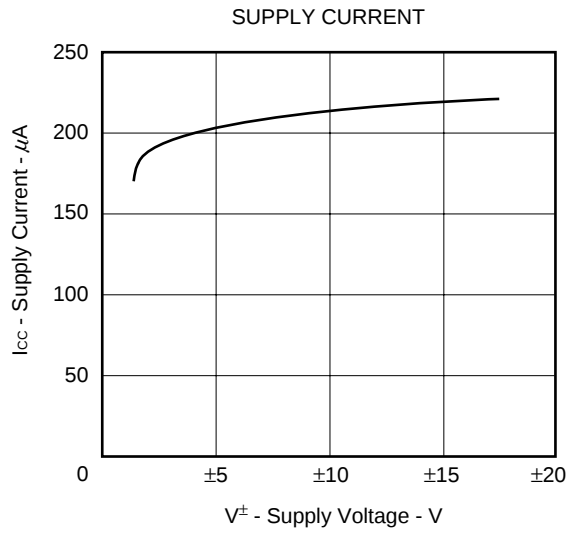
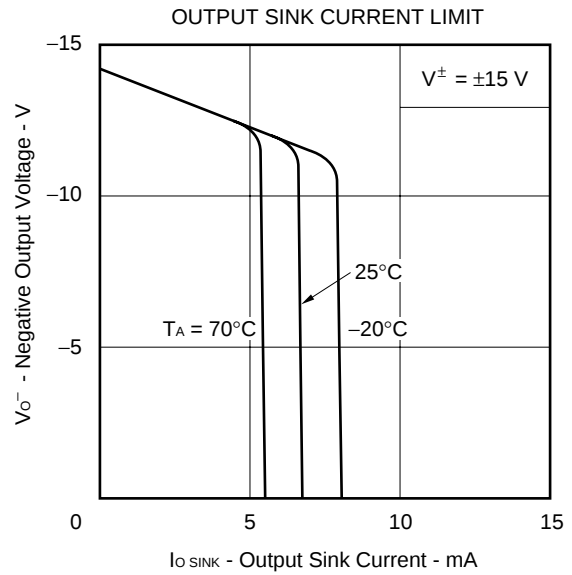
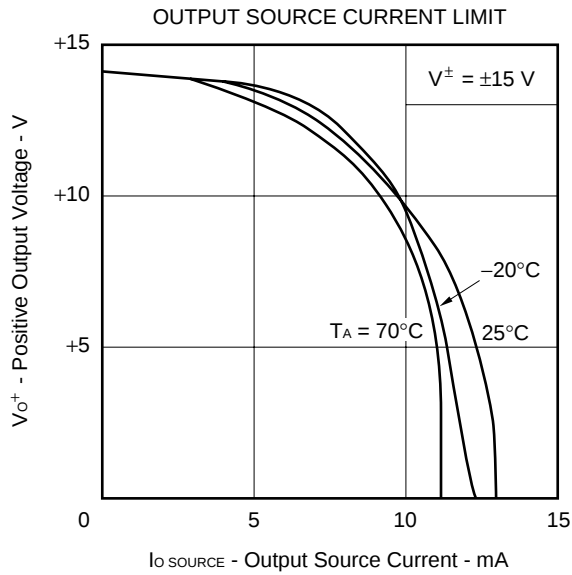
ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, $V^{\pm} = \pm 15\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50\text{ }\Omega$		± 2	± 10	mV
Input Offset Current ^{Note 7}	I_{IO}			± 5	± 50	pA
Input Bias Current ^{Note 7}	I_B			10	100	pA
Large Signal Voltage Gain	A_v	$R_L \geq 10\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	3000	9000		
Supply Current	I_{CC}	$I_O = 0\text{ A}$		220	250	μA
Common Mode Rejection Ratio	CMR		70	90		dB
Supply Voltage Rejection Ratio	SVR		70	90		dB
Output Voltage Swing	V_{om}	$R_L \geq 10\text{ k}\Omega$	± 12	+14.0 -13.6		V
Common Model Input Voltage Range	V_{ICM}		± 12	+15 -13		V
Slew Rate	SR	$A_v = 1$		3		V/μs
Unity Gain Frequency	f_{unity}			1		MHz
Input Equivalent Noise Voltage Density	e_n	$R_S = 100\text{ }\Omega$, $f = 1\text{ kHz}$		30		nV/ $\sqrt{\text{Hz}}$
Input Offset Voltage	V_{IO}	$R_S \leq 50\text{ }\Omega$, $T_A = -20\text{ to }+70\text{ }^{\circ}\text{C}$			± 15	mV
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$	$T_A = -20\text{ to }+70\text{ }^{\circ}\text{C}$		± 10		μV/ $^{\circ}\text{C}$
Input Offset Current ^{Note 7}	I_{IO}	$T_A = -20\text{ to }+70\text{ }^{\circ}\text{C}$			± 2	nA
Input Bias Current ^{Note 7}	I_B	$T_A = -20\text{ to }+70\text{ }^{\circ}\text{C}$			3.5	nA

Notes 7. Input bias currents flow into IC. Because each currents are gate leak current of P-channel J-FET on input stage. And that are temperature sensitive. Short time measuring method is recommendable to maintain the junction temperature close to the operating ambient temperature.

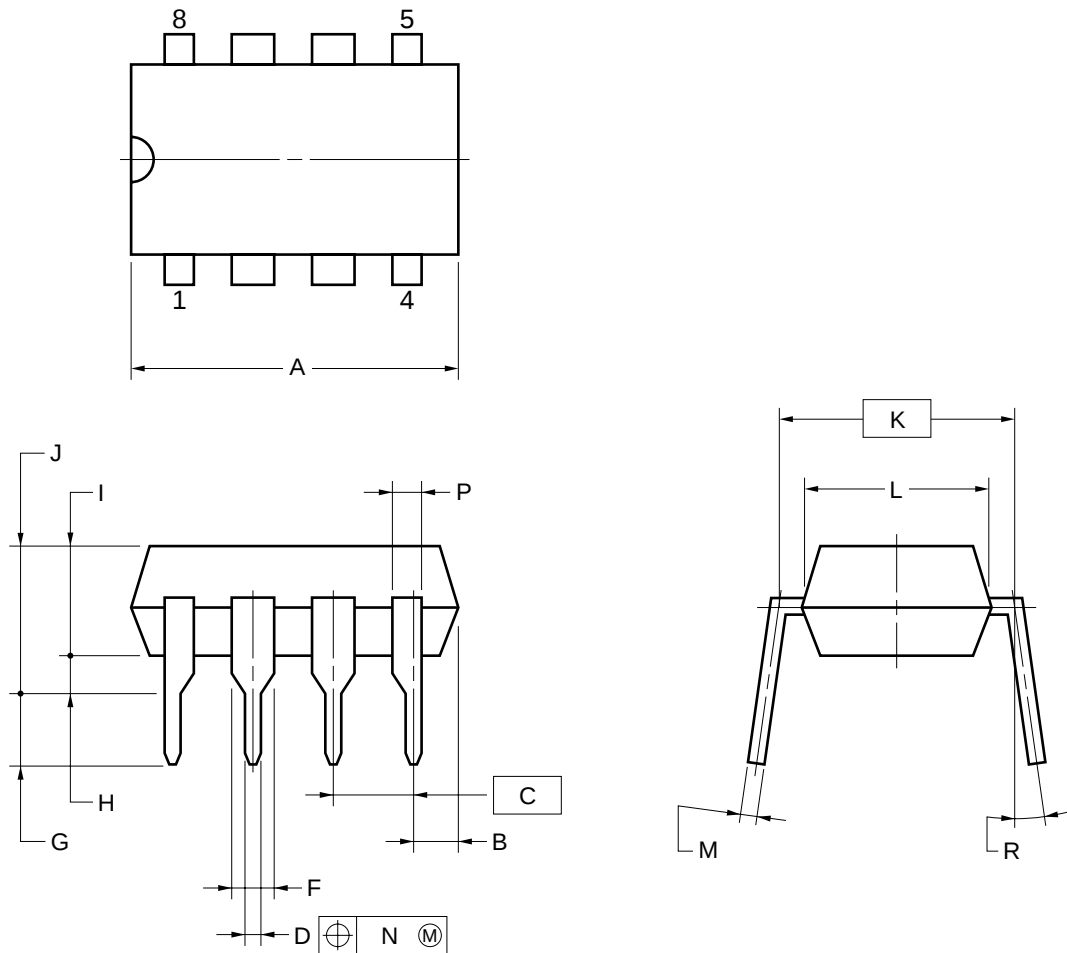
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$, TYP.)





★ PACKAGE DRAWINGS (Unit : mm)

8-PIN PLASTIC DIP (7.62mm(300))



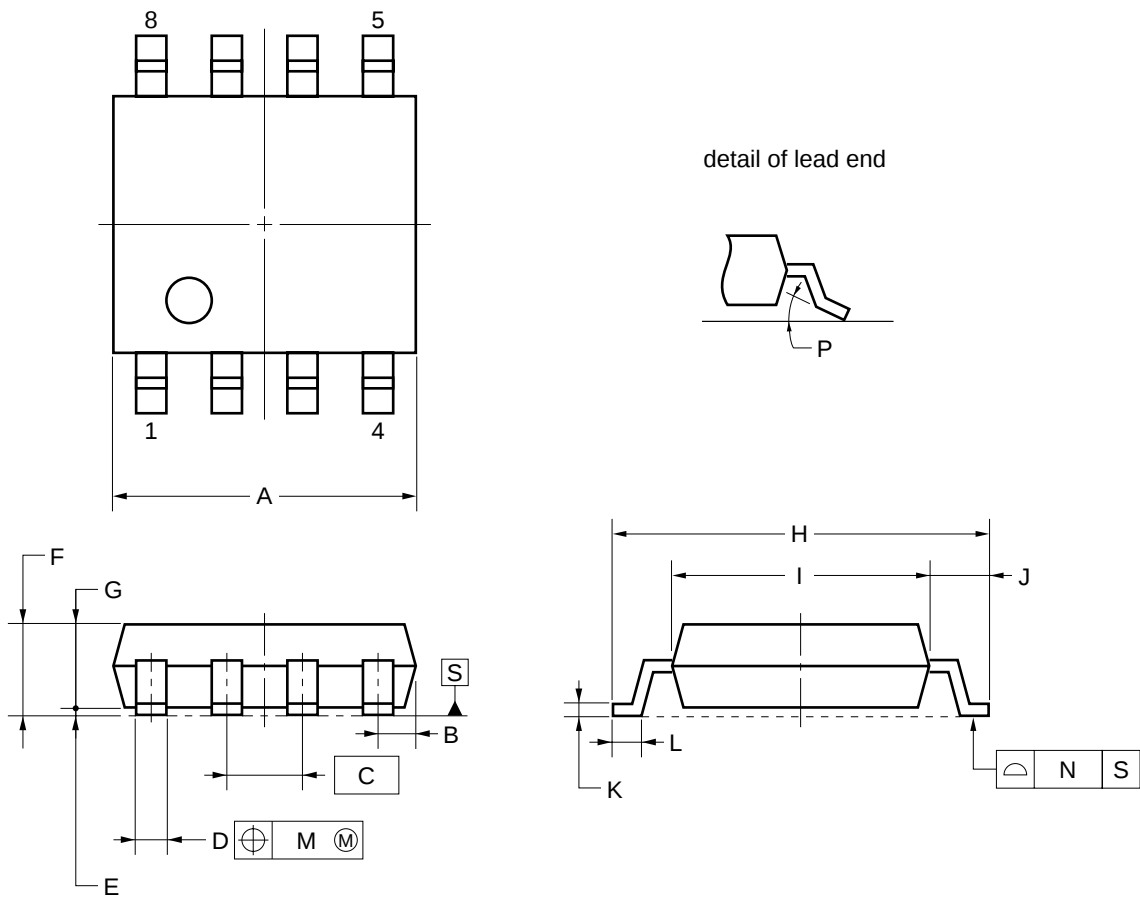
NOTES

1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	10.16 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.4 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.4
M	0.25 ^{+0.10} _{-0.05}
N	0.25
P	0.9 MIN.
R	0~15°

P8C-100-300B,C-2

8-PIN PLASTIC SOP (5.72 mm (225))



NOTE
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 ^{+0.17} _{-0.20}
B	0.78 MAX.
C	1.27 (T.P.)
D	0.42 ^{+0.08} _{-0.07}
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	0.17 ^{+0.08} _{-0.07}
L	0.6±0.2
M	0.12
N	0.10
P	3° ^{+7°} _{-3°}

S8GM-50-225B-6

★ RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL"(C10535E).

Type of Surface Mount Device

μPC4061G2: 8-pin plastic SOP (5.72 mm (225))

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 230 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 1 time.	IR30-00-1
Vapor Phase Soldering	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 1 time.	VP15-00-1
Wave Soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature).	WS60-00-1
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Type of Through-hole Device

μPC4061C: 8-pin plastic DIP (7.62 mm (300))

Process	Conditions
Wave Soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each lead).

Caution For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

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