



3.3V CMOS OCTAL D-TYPE FLIP-FLOP WITH RESET, POSITIVE EDGE TRIGGER, AND 5 VOLT TOLERANT I/O

IDT74LVC273A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 3.3V ± 0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4μ W typ. static)
- Rail-to-rail output swing for increased noise margin
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP and TSSOP packages

DRIVE FEATURES:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

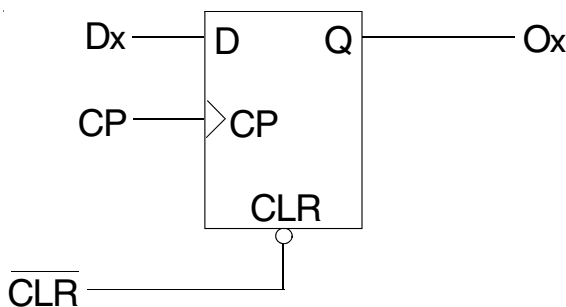
- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

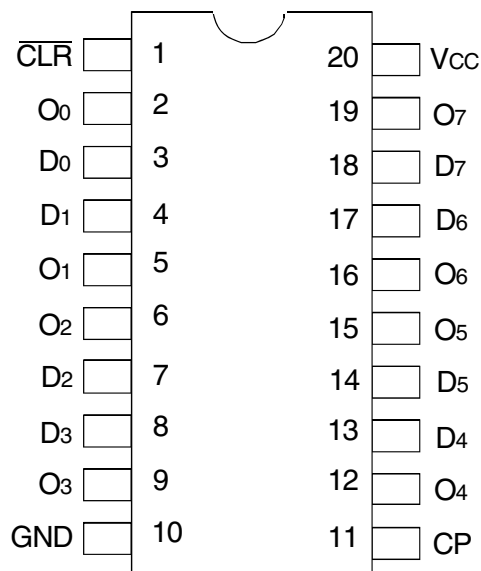
The octal D-type flip-flop with reset, positive edge trigger is built using advanced dual metal CMOS technology. This high-speed, low power device is ideal for driving high capacitance loads such as memory address and data buses.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +6.5	V
TSTG	Storage Temperature	−65 to +150	°C
IOUT	DC Output Current	−50 to +50	mA
IIK IOK	Continuous Clamp Current, Vi < 0 or Vo < 0	−50	mA
ICC ISS	Continuous Current through each Vcc or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOU = 0V	5.5	8	pF
C/I/O	I/O Port Capacitance	VIN = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
CLR	Clear Input
CP	Clock Input
Ox	Data Outputs
Dx	Data Inputs

FUNCTION TABLE ⁽¹⁾

Inputs			Internal	Outputs	Function
CLR	CP	Dx	Q Value	Ox	
L	X	X	L	L	Clear Register
H	↑	L	L	L	Load Input Data
H	↑	H	H	H	Load Input Data

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	500	μA

NOTES:

1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3\text{V}$		2.4	—	
		$V_{CC} = 3\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.
 $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$C_L = 0pF$, $f = 10MHz$	—	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		—	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, CP to Ox	1.5	9.5	1.5	8.5	ns
t_{PHL}	Propagation Delay, $\overline{CLR}$ to Ox	1.5	9.5	1.5	8.5	ns
t_S	Data Setup Time, Dx to CP	2.5	—	2.5	—	ns
t_H	Data Hold Time, Dx to CP	1.5	—	1.5	—	ns
t_{REC}	$\overline{CLR}$ Recovery Time, $\overline{CLR}$ to CP	2	—	2	—	ns
t_{WCLR}	$\overline{CLR}$ Pulse Width, LOW	3.3	—	3.3	—	ns
t_{WCP}	CLK Pulse Width, HIGH or LOW	3.3	—	3.3	—	ns
$t_{SK(0)}$	Output Skew ⁽²⁾	—	—	—	500	ps

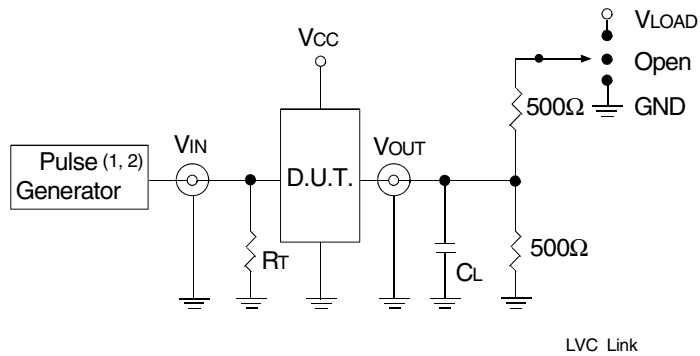
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

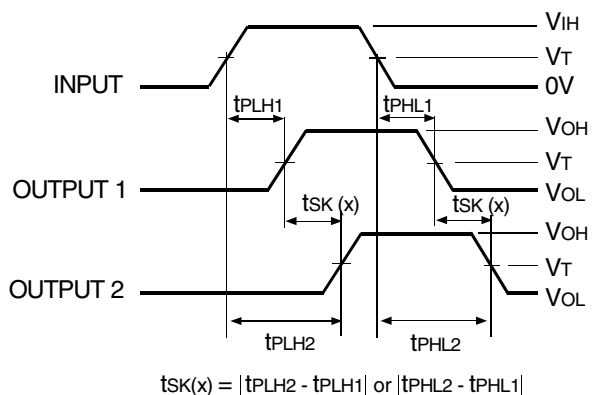
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

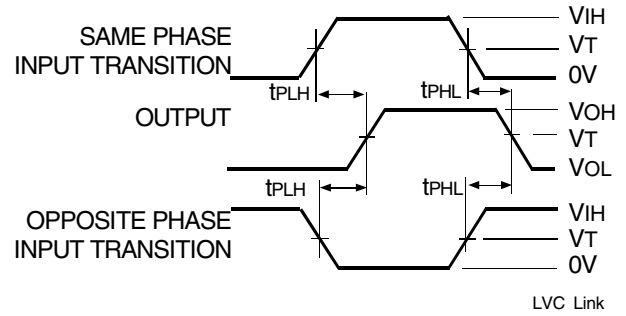
Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



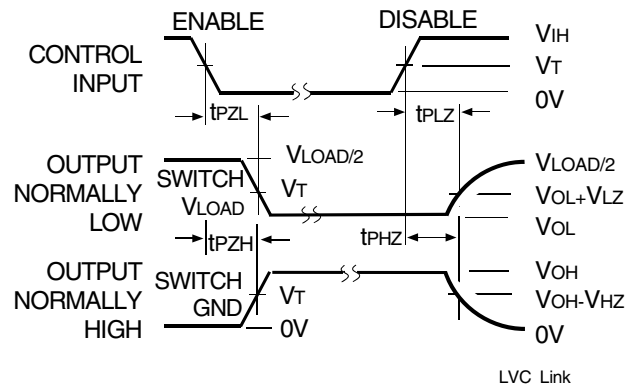
Output Skew - ts(x)

NOTES:

1. For ts(x) OUTPUT1 and OUTPUT2 are any two outputs.
2. For ts(b) OUTPUT1 and OUTPUT2 are in the same bank.



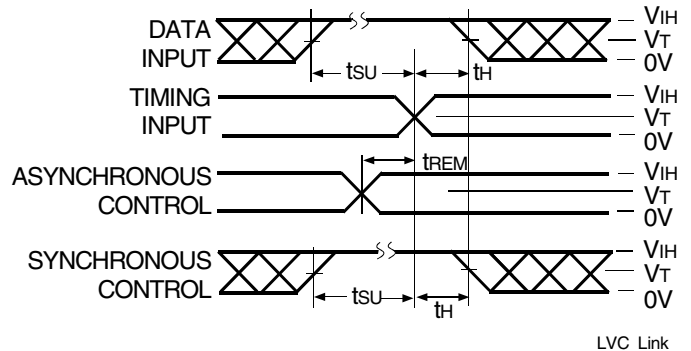
Propagation Delay



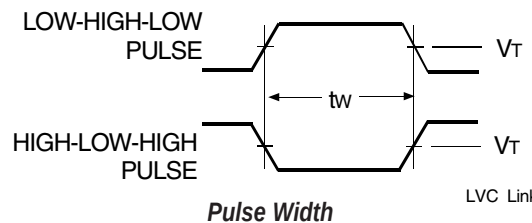
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

<u>XX</u>	<u>LVC</u>	<u>X</u>	<u>XXXX</u>	<u>XX</u>	
Temp. Range		Bus-Hold	Device Type	Package	
				PY	Shrink Small Outline Package
				PYG	SSOP - Green
				PG	Thin Shrink Small Outline Package
				PGG	TSSOP - Green
			273A		Octal D-Type Flip-Flop with Reset, Positive Edge Trigger, 5V Tolerant I/O
				Blank	No Bus-hold
				74	-40°C to +85°C



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