



# AP4405AEN

Ultra-Low Power Voltage Detector with P and N-Channel MOSFET Switch

## 1. General Description

The AP4405AEN is an ultra-low power consumption, 0.010 $\mu$ A, voltage detector IC that integrates MOSFET switches and gate logic circuits. The AP4405AEN's polarity of voltage detection result is selectable and the gate logic can be controlled separately from input detection voltage. On-chip P-ch MOSFET and N-ch MOSFET on & off control action along with voltage detection result is utilized as a load switch function. The AP4405AEN achieves best in class low power consumption and offers smaller PCB area than conventional voltage detector ICs with discrete logics and external MOSFETs. The IC is suitable for various applications, such as over charge/discharge protection of Lithium-ion batteries and Lithium-ion capacitors, power management function of energy harvesting devices and load switch of wearable devices.

## 2. Features

- Power management function
  - Voltage detection circuit
  - Control logic with independent power supply
  - On-chip P-channel and N-Channel MOSFETs
- Wide range for detection voltage
 

Detection Voltage "High" (VDETH)	1.8 ~ 4.4V (Options)
Detection Voltage "Low" (VDETL)	1.7 ~ 4.3V (Options)
- Voltage detection accuracy
 

	$\pm 35\text{mV}$ (VDETH, VDETL >3.0V)
	$\pm 20\text{mV}$ (VDETH, VDETL $\leq 3.0\text{V}$ )
- Ultra-low power consumption
 

	0.010 $\mu$ A typical
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- Response Time
 

	0.5msec typical
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- On resistance
 

	On-chip P-ch MOSFET 1.3 $\Omega$ typical
	On-chip N-ch MOSFET 2.3 $\Omega$ typical
- Operation temperature
 

	-40 ~ +85 $^{\circ}\text{C}$
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- Package
 

	16-pin HWQFN (3.0 x 3.0mm 0.5mm pitch)
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4. Block Diagram

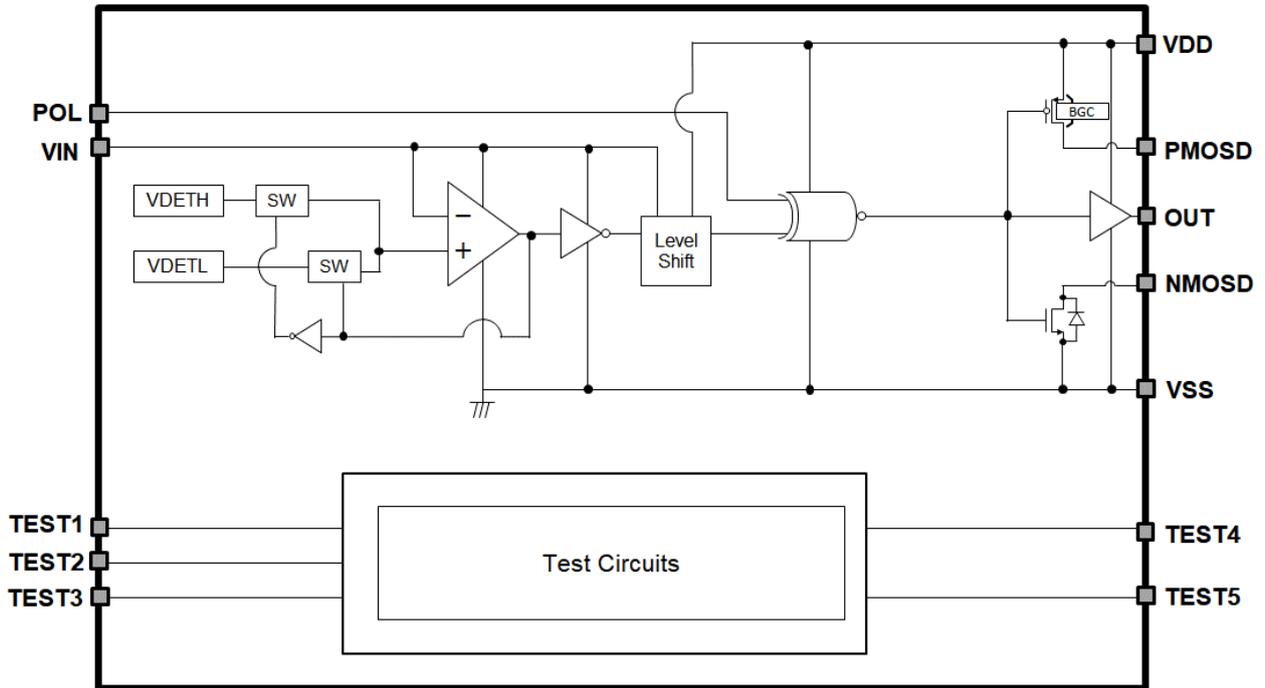
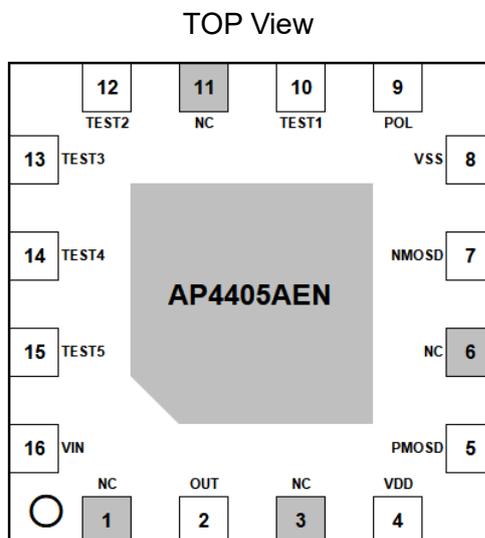


Figure 1. Block Diagram

**5. Pin Configuration and Function**

**5.1 Pin Configuration**  
 • 16-pin HWQFN



**5.2 Function**

Pin #	Name	I/O	Function
1	NC	-	Not Connected
2	OUT	Output	Logic output
3	NC	-	Not Connected
4	VDD	Power	Power supply
5	PMOSD	Input/Output	PMOS drain pin
6	NC	-	Not Connected
7	NMOSD	Input/Output	NMOS drain pin
8	VSS	Ground	Ground
9	POL	Input	Polarity cotrol pin. Do not set this pin in the floating state.
10	TEST1	-	For test purposes. This pin should be connected to VSS.
11	NC	-	Not Connected
12	TEST2	-	For test purposes. This pin should be connected to VSS.
13	TEST3	-	For test purposes. This pin should be connected to VSS.
14	TEST4	-	For test purposes. This pin should be connected to VSS.
15	TEST5	-	For test purposes. This pin should be connected to VSS.
16	VIN	Power	Detection voltage input pin
-	TAB	-	Connecting the exposed pad that is located on the bottom of the package(EPAD) to VSS is recommended. The pad can be left floating if needed.

### 5.3 Unused Pins

Following tables show recommended handling of unused pins.

- In the case of on-chip Pch-MOSFET is not used.

Pin #	Name	I/O	Recommended Handling	Remarks
5	PMOSD	Input/Output	Open	

- In the case of on-chip Nch-MOSFET is not used.

Pin #	Name	I/O	Recommended Handling	Remarks
7	NMOSD	Input/Output	Open	

- In the case of OUT pin is not used.

Pin #	Name	I/O	Recommended Handling	Remarks
2	OUT	Output	Open	

**6. Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Unit
Pin Voltage (*1)	VIN VDD	-0.3	6.5	V
	OUT POL	VSS-0.3	VDD + 0.3	V
	PMOSD	-0.3	6.5	V
	NMOSD	-0.3	6.5	V
Output Current	OUT pin Current (I <sub>out</sub> )	-10	+10	mA
Power Dissipation (*2)	Pd	-	2.56 (EPAD→VSS) 0.94 (EPAD→Float)	W
Storage Temperature	T <sub>stg</sub>	-55	+150	°C

Notes:

\*1. All voltages are with reference to VSS = 0 V.

\*2. The value is derived from condition below. Figure 2 shows the simulation results.

74mm□-1.6t-4layer FR-4 PCB, using Sn-3.0Ag-0.5Cu solder

Bottom exposed PAD(EPAD) is mounted:  $\theta_{ja}=39.07$  (°C /W)

Bottom exposed PAD(EPAD) is unmounted:  $\theta_{ja}=106.04$  (°C /W)

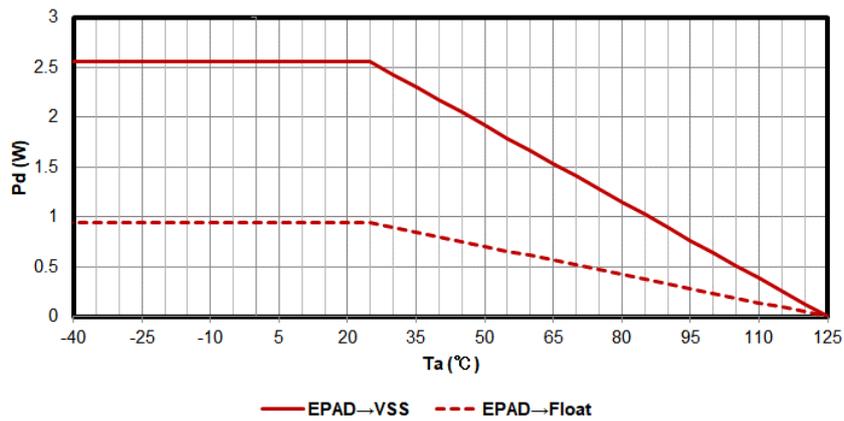


Figure 2. Power Dissipation vs Temperature

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

**7. Recommended Operating Conditions**

Parameter	Symbol	min	max	Unit
Operation Temperature	Ta	-40	+85	°C
Power Supply Voltage	VIN VDD	1.2	5.5	V

AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

<b>8. Electrical Characteristics</b>
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Ta= -40 ~ +85°C, VIN and VDD=1.2V ~ 5.5V、OUT=open、PMOSD=open、NMOSD=open, unless otherwise specified.

Parameter	Symbol	min	typ	max	Unit	Condition
Detection Voltage "High"	V <sub>DETH</sub>	V <sub>DETH</sub> -0.035	V <sub>DETH</sub>	V <sub>DETH</sub> +0.035	V	Ta=+25 °C V <sub>DETH</sub> > 3.0V VIN= "L" → "H"
		V <sub>DETH</sub> -0.020		V <sub>DETH</sub> +0.020		Ta=+25 °C V <sub>DETH</sub> ≤ 3.0V VIN= "L" → "H"
		V <sub>DETH</sub> -0.045		V <sub>DETH</sub> +0.045	V	Ta=+85 °C VIN="L" → "H"
Detection Voltage "Low"	V <sub>DETL</sub>	V <sub>DETL</sub> -0.035	V <sub>DETL</sub>	V <sub>DETL</sub> +0.035	V	Ta=+25 °C V <sub>DETL</sub> > 3.0V VIN= "H" → "L"
		V <sub>DETL</sub> -0.020		V <sub>DETL</sub> +0.020		Ta=+25 °C V <sub>DETL</sub> ≤ 3.0V VIN= "H" → "L"
		V <sub>DETL</sub> -0.045		V <sub>DETL</sub> +0.045	V	Ta=+85 °C VIN= "H" → "L"
Power Consumption	IVIN	-	0.010	0.040	μA	Consumption of VIN pin
	IVDD	-	0.0001	0.050	μA	Consumption of VDD pin (*3)
Minimum Operating Voltage	VOPL	-	-	1.0	V	(*4)
"H" Level Input Voltage	V <sub>IH</sub>	VDD ×0.8	-	-	V	
"L" Level Input Voltage	V <sub>IL</sub>	-	-	VDD ×0.2	V	
IOH	I <sub>OH</sub>	0.15	-	-	mA	VIN=V <sub>DETH</sub> +0.1V, OUT=VDD×0.8
IOL	I <sub>OL</sub>	0.2	-	-	mA	VIN=V <sub>DETL</sub> -0.1V, OUT=VDD×0.2
Response Time (*5)	t <sub>PLH</sub>	-	0.5	1.0	msec	VIN=V <sub>DETH</sub> -0.2V →V <sub>DETH</sub> +0.2V
	t <sub>PHL</sub>	-	0.5	1.0	msec	VIN= V <sub>DETL</sub> +0.2V →V <sub>DETL</sub> -0.2V
P-ch MOSFET On-resistance	R <sub>onP</sub>	-	1.3	2.7	Ω	VDD ≥ 1.7V Push current = 100mA
N-ch MOSFET On-resistance	R <sub>onN</sub>	-	2.3	5.2	Ω	VDD ≥ 1.7V Pull current = 32mA

Notes:

\*3. Output drive is not included.

\*4. VOPL is means the lowest voltage where OUT pin output voltage is guaranteed to be as "High" or "Low" when VIN voltage is same as VDD.

POL = "L": OUT pin with 10MΩ pull-up resistor

POL = "H": OUT pin with 10MΩ pull-down resistor

\*5. Response time for OUT pin

**9. Functional Description**

**9.1 Voltage Detection Function**

**1) Detection voltage(VIN) and supply voltage(VDD) both increase at a time. (POL = "L")**

The OUT pin will be in undefined status when VIN voltage is from VSS to VOPL which is the AP4405AEN minimum operating voltage(1.0V). The OUT pin outputs VSS when VIN voltage exceeds VOPL. When VIN voltage reaches to the detection voltage (VDETH), the OUT pin outputs VDD voltage.

**2) Detection voltage(VIN) and supply voltage(VDD) both decrease at a time. (POL = "L")**

When VIN voltage is higher than VDETH, the OUT pin outputs VDD. When VIN goes under the detection voltage (VDETL), the OUT pin outputs VSS. The OUT pin will be in undefined status when VIN voltage becomes lower than VOPL.

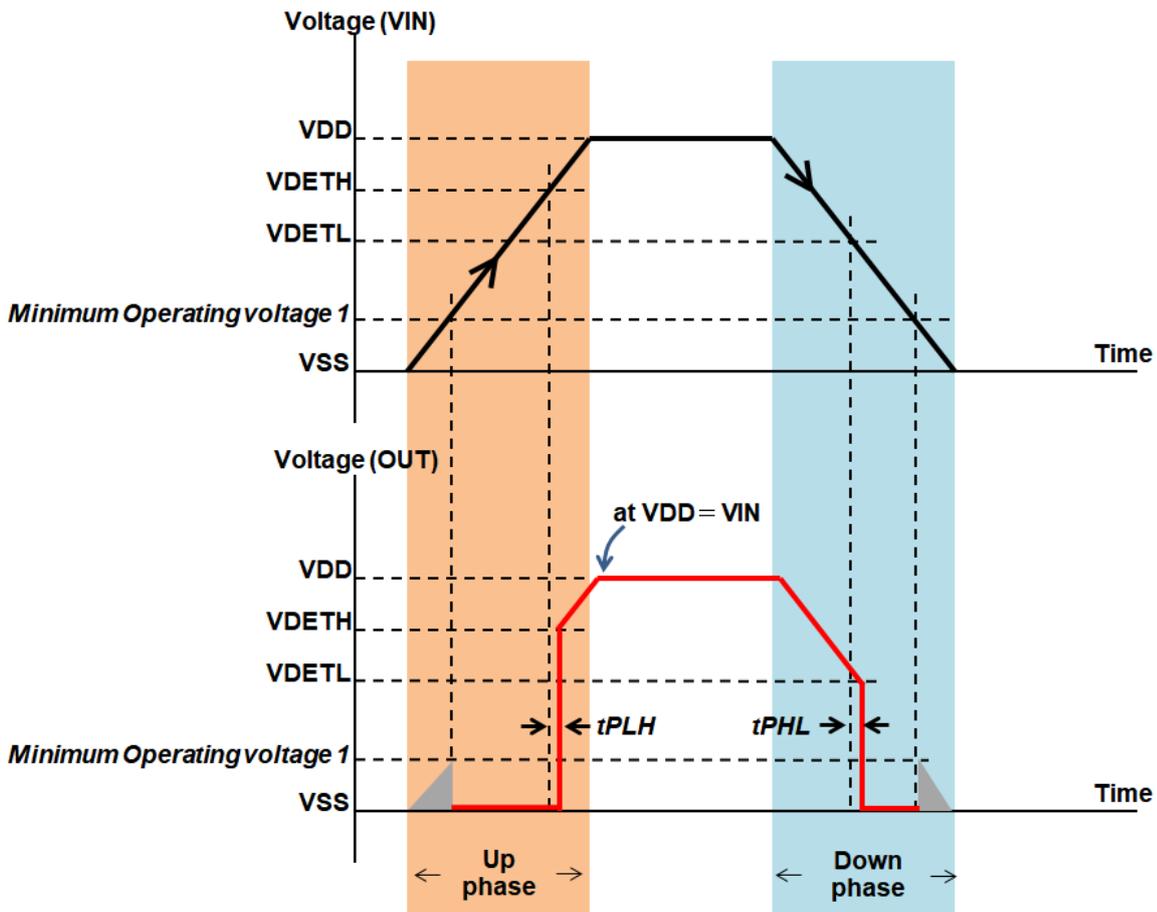


Figure 3. Voltage detection function, VIN = VDD, POL = "L"

Table 1. Voltage Detection Table, POL="L"

VDD	OUT	Note
$< V_{DETH}$	VSS	Up phase
$\geq V_{DETH}$	VDD	
$> V_{DETL}$	VDD	Down phase
$\leq V_{DETL}$	VSS	

**3) Supply voltage(VDD) is powered up and detection voltage(VIN) increases separately from VDD (POL = "L")**

When VIN voltage reaches to the detection voltage (VDETH), the OUT pin outputs VDD voltage.

**4) Supply voltage(VDD) is powered up and detection voltage(VIN) decreases separately from VDD (POL = "L")**

When VIN voltage is higher than VDETH, the OUT pin outputs VDD. When VIN goes under the detection voltage (VDETL), the OUT pin outputs VSS.

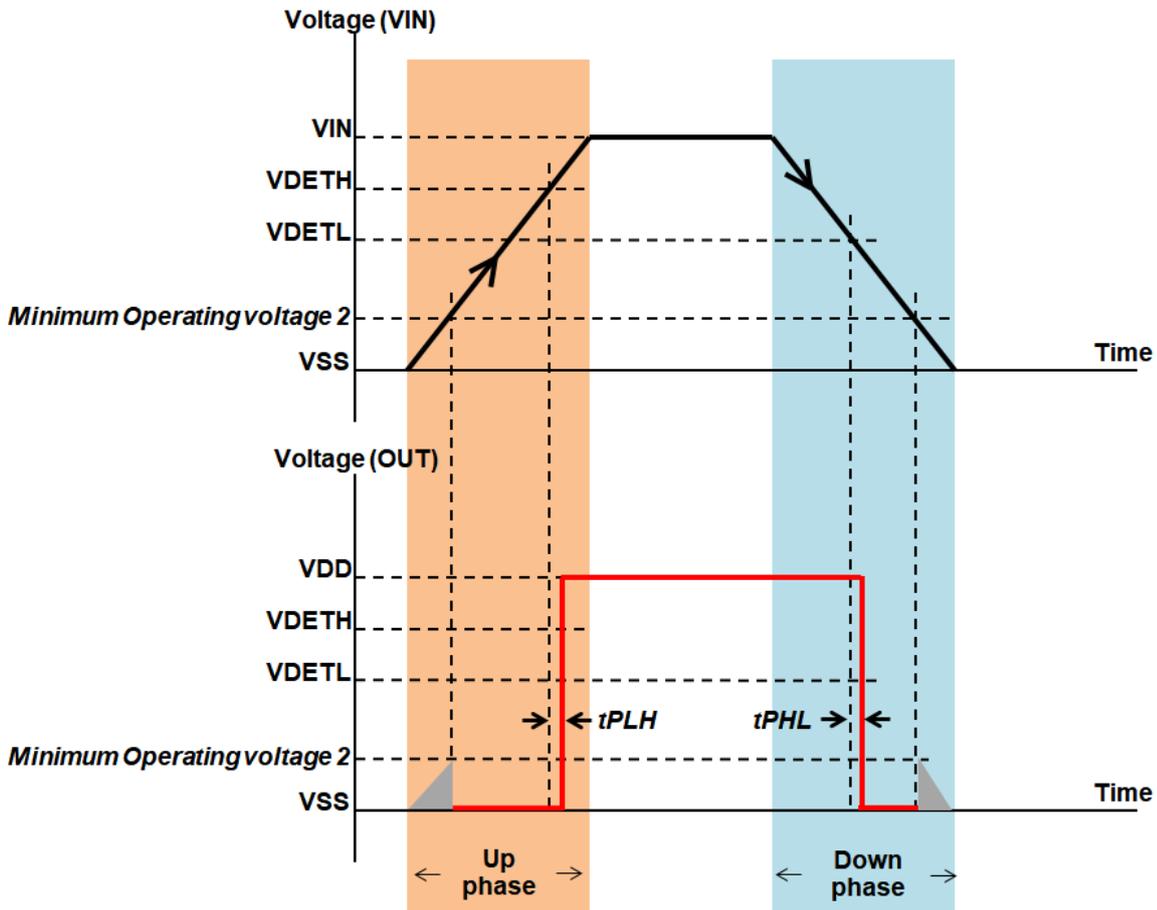


Figure 4. Voltage detection function, VIN is controlled separately from VDD, POL="L"

OUT pin polarity is controlled by POL pin. Table 2 shows MOSSETs output status and OUT pin polarity.

Table 2. OUT pin polarity

POL	VIN	PMOSD	NMOSD	OUT	Note
"L"	$V_{IN} < V_{DETH}$	ON	OFF	L	OUT: Positive Polarity
	$V_{IN} \geq V_{DETL}$	OFF	ON	H	
"H"	$V_{IN} < V_{DETH}$	OFF	ON	H	OUT: Negative Polarity
	$V_{IN} \geq V_{DETL}$	ON	OFF	L	

## 9.2 Reference Data

### 9.2.1 Reference Circuit

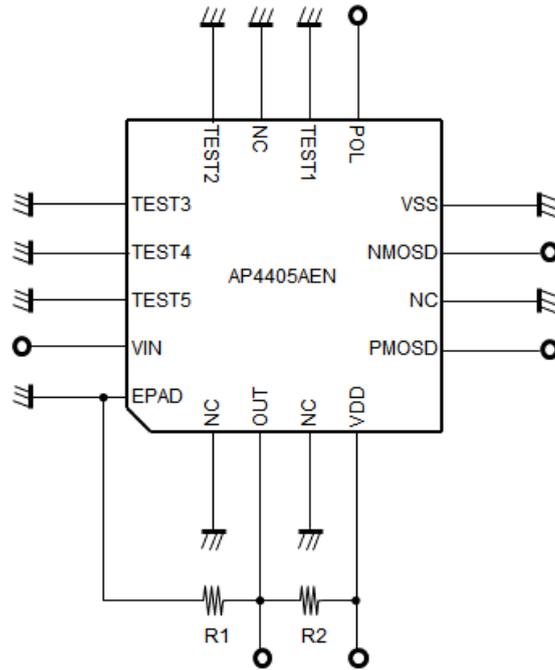


Figure 5. Reference Circuit for measurement

### 9.2.2 Detection voltage

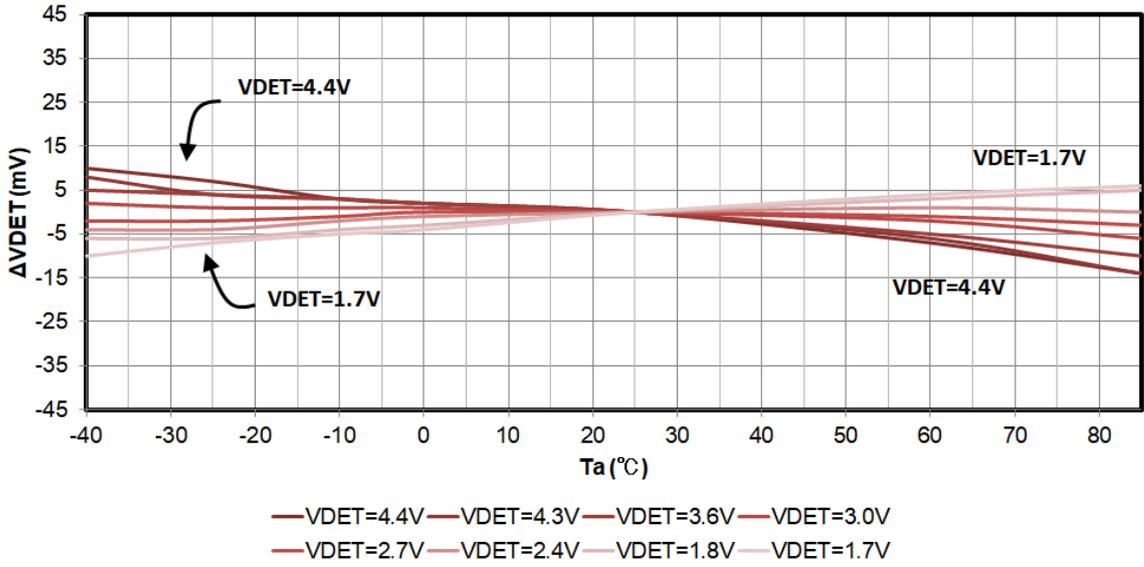


Figure 6. Temperature characteristics of  $V_{DET}$  normalized at +25°C

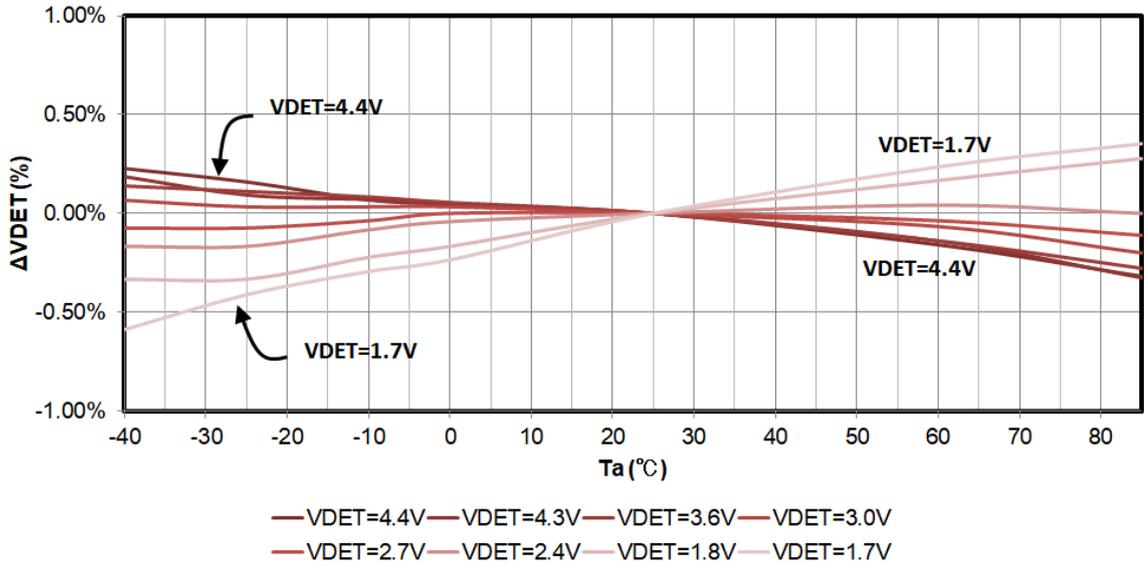


Figure 7. Temperature characteristics of  $V_{DET}$  normalized at +25°C

$$\Delta V_{DET} (\%) = \Delta V_{DET} \div V_{DET}$$

### 9.2.3 Minimum operating voltage

- VIN=VDD (VOPL), VIN and supply VDD are controlled simultaneously.

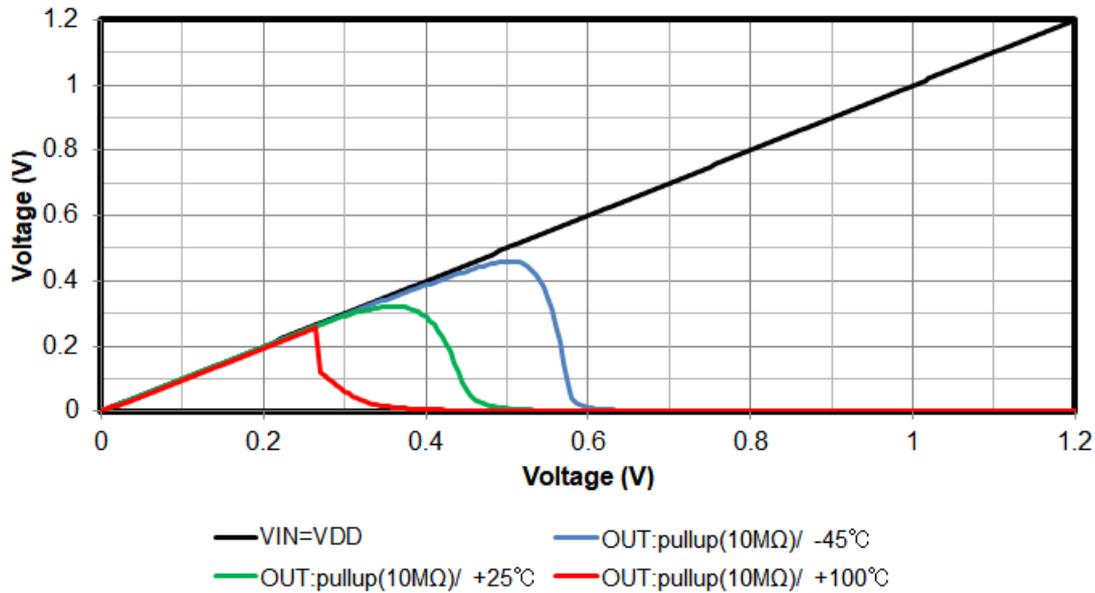


Figure 8. Minimum operating voltage POL= "L" vs Temperature (VDD=VIN)  
R1=10MΩ/ R2= DNP (Do Not Populate)

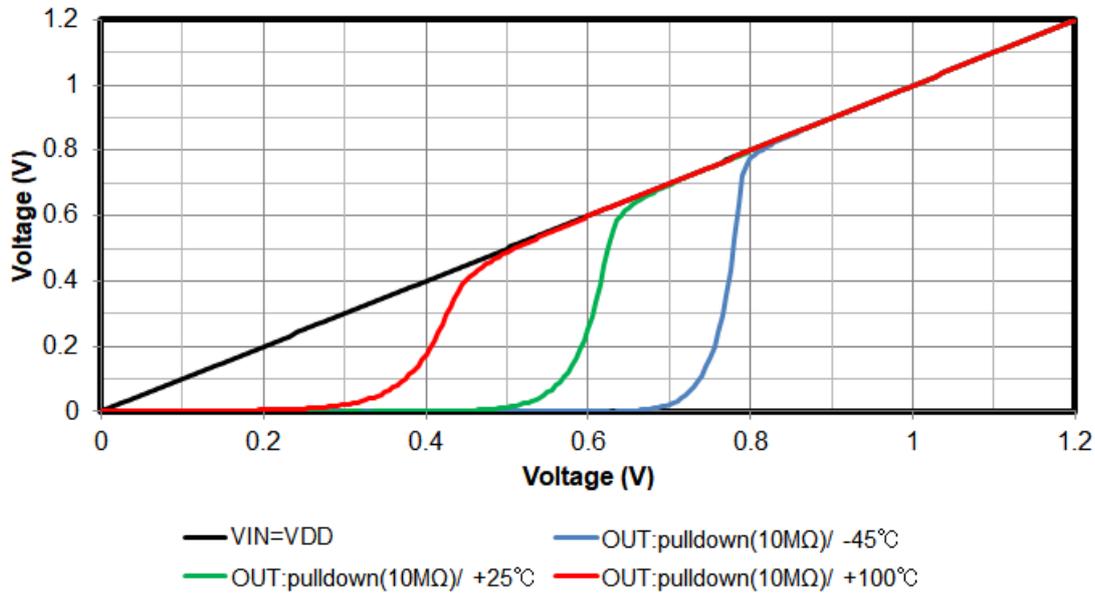


Figure 9. Minimum operating voltage POL= "H" vs Temperature (VDD=VIN)  
R1=DNP/ R2=10MΩ

- VIN and supply VDD are controlled separately. (VIN is fixed, VDD voltage is swept.)

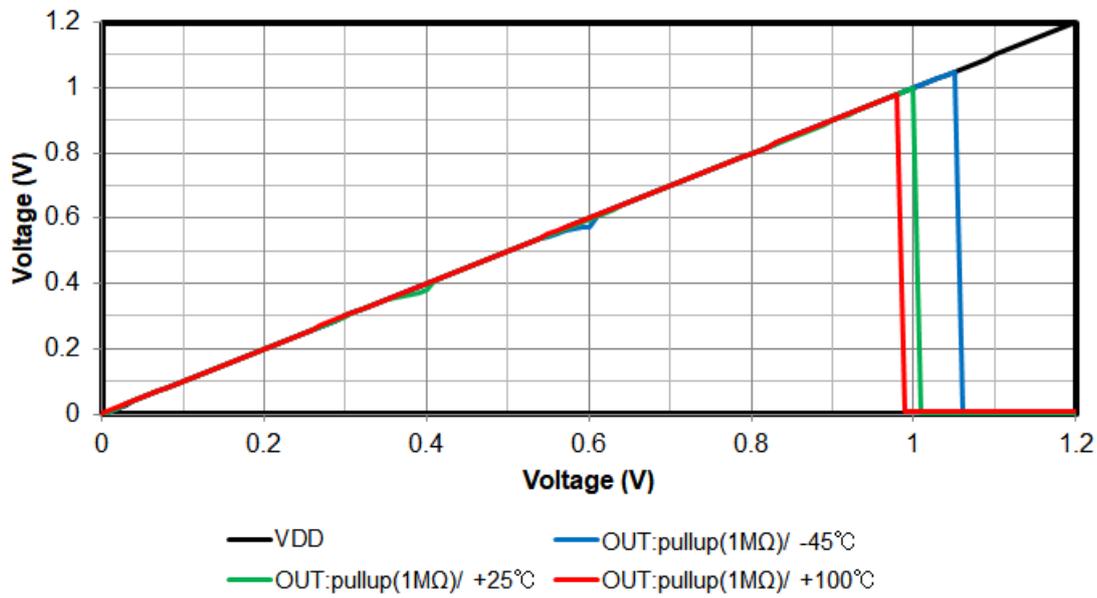


Figure 10. Minimum operating voltage at POL= "L" vs Temperature (VDD≠VIN, VIN=5.5V)  
R1=10MΩ/ R2=DNP

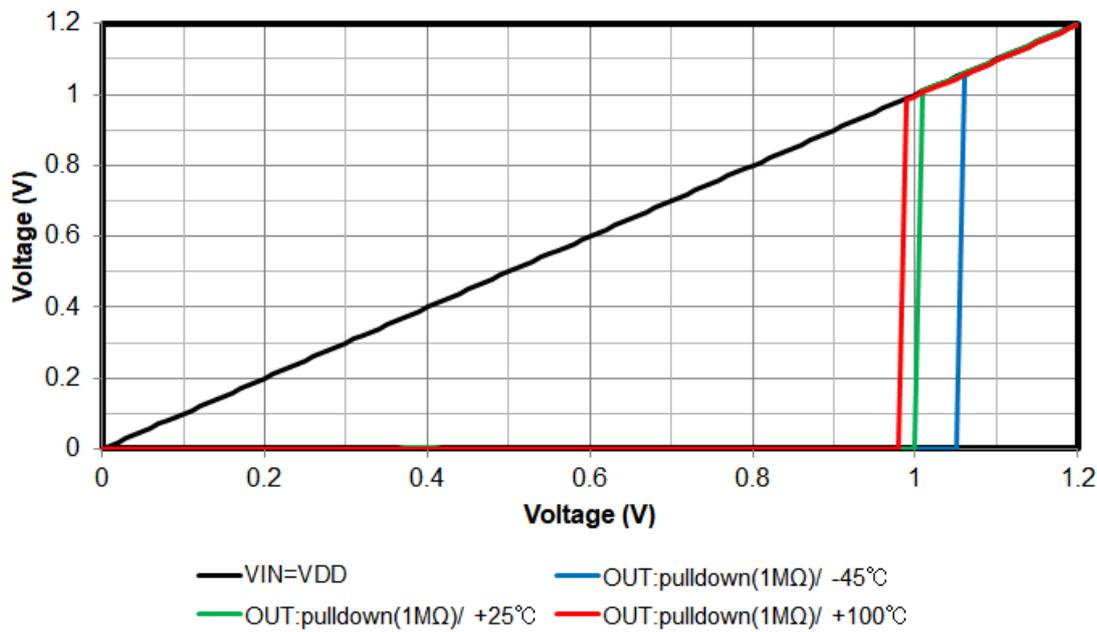


Figure11. Minimum operating voltage at POL= "H" vs Temperature (VDD≠VIN, VIN=5.5V)  
R1=10MΩ/ R2=DNP

### 9.2.3 Current consumption

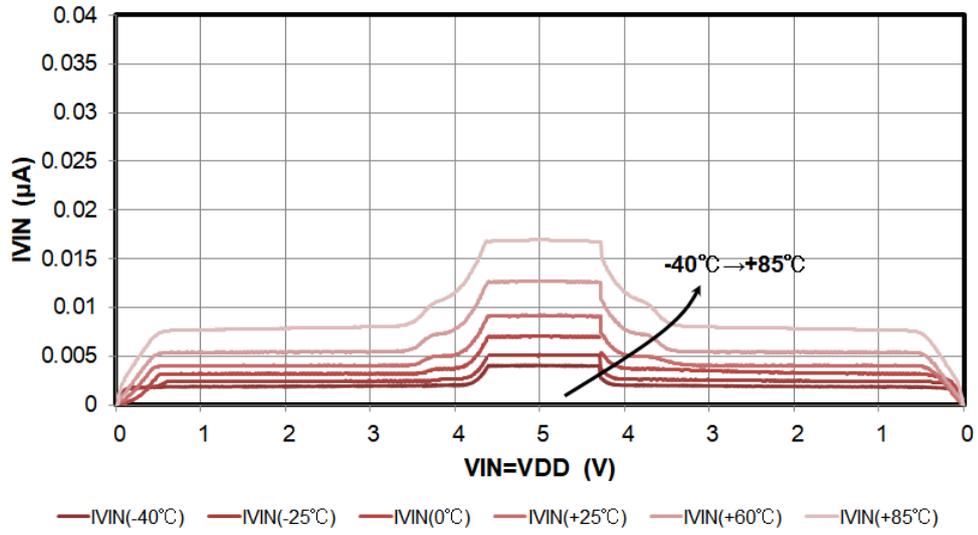


Figure 12. IVIN vs Temperature at VDETH=4.4V, VDETL=4.3V (VIN=VDD sweep), POL = "L"

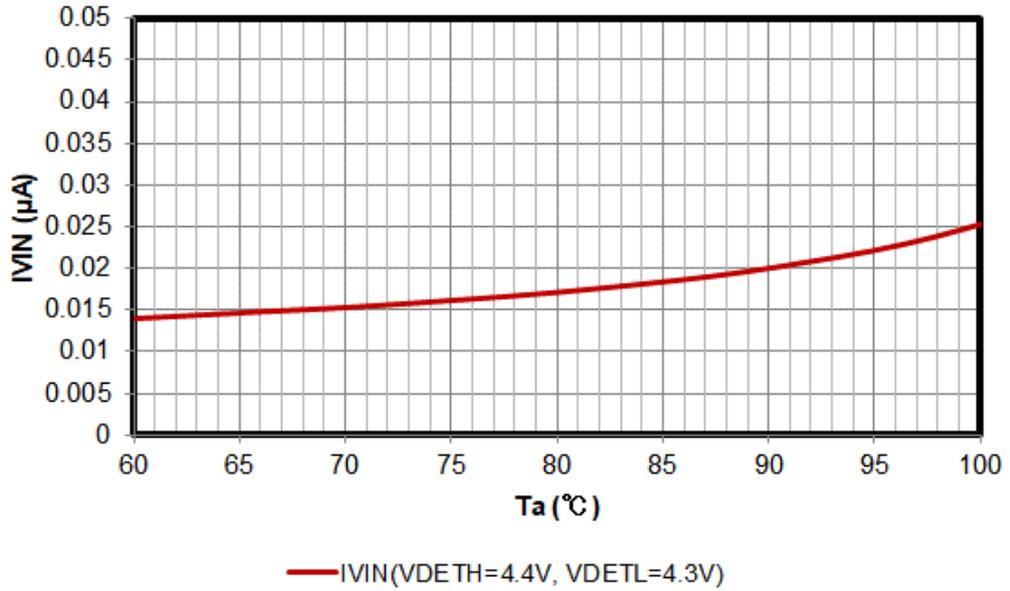


Figure 13. IVIN vs Temperature at VIN=VDD=5.5V, POL = "L"

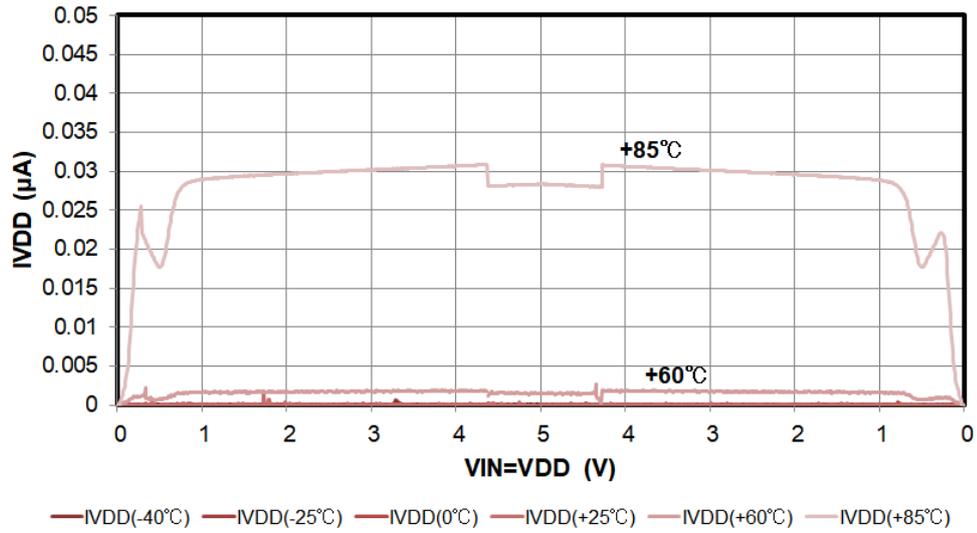


Figure 14. IVDD vs Temperature at VDETH=4.4V, VDETL=4.3V (VIN=VDD sweep), POL = "L"

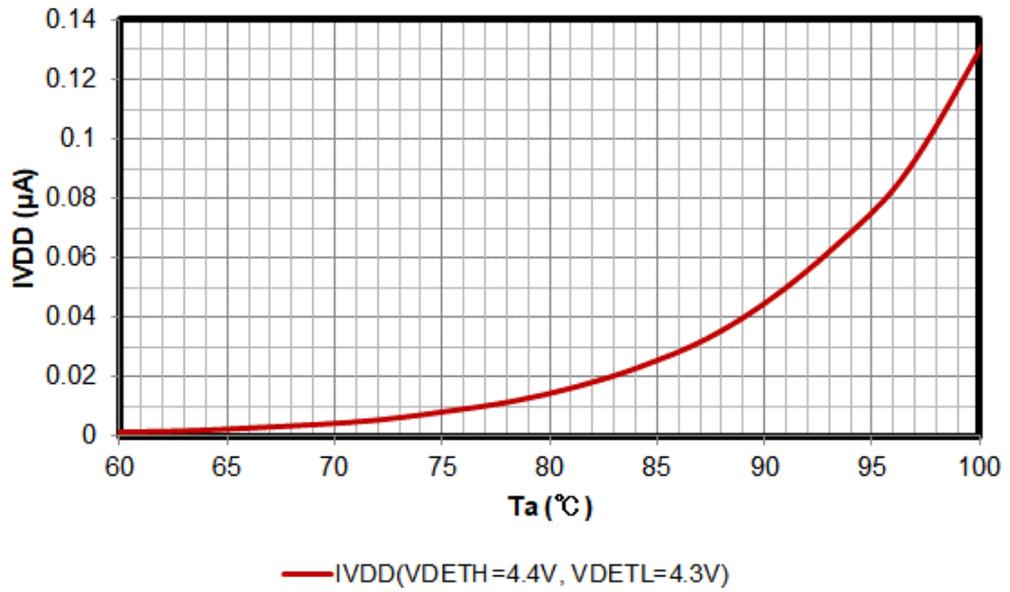


Figure 15. IVDD vs Temperature at VIN=VDD=5.5V, POL="L"

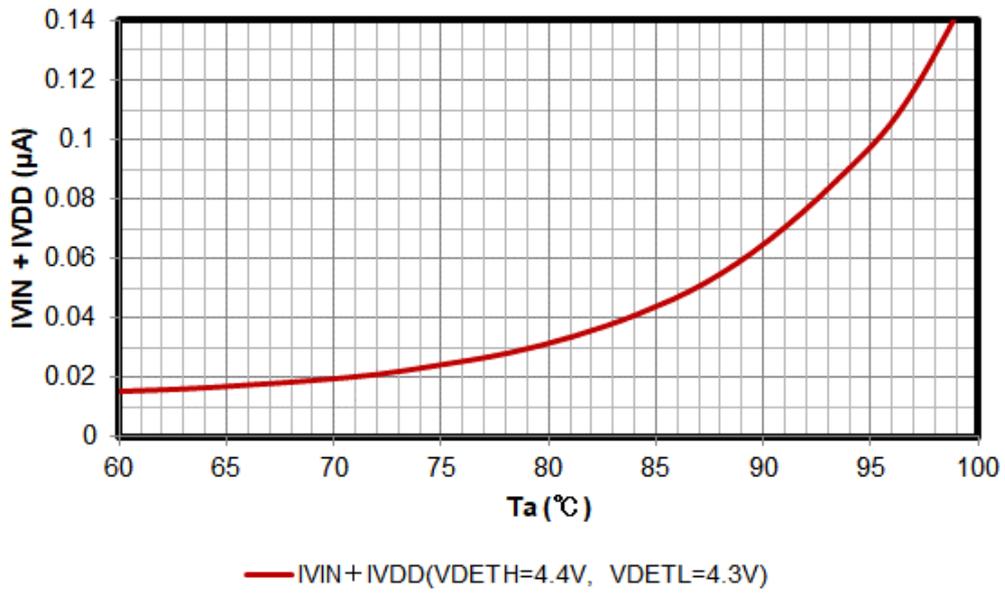


Figure 16.  $I_{VIN} + I_{VDD}$  vs Temperature



## 11. Revision History

Date (YY/MM/DD)	Revision	Page	Contents
2019 /03/05	00	-	First Edition

## IMPORTANT NOTICE

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