Automotive Motor Driver Series

3-Phase Brushless Motor Pre-driver for Automotive

BD63030EKV-C

General Description

BD63030EKV-C is a pre-driver for a 3-phase motor such as an air conditioner blower motor and a battery cooling fan motor. 180° commutation PWM drive minimizes motor drive noise. It has a built-in automatic lead angle control function for high-efficiency drive. Moreover, it has the lock protection time, over current limit detect value, over current protection detect value, external parts thermal shutdown value for various motor controls as well as adjustment of startup time externally.

Features

- AEC-Q100 Qualified [(Note 1)]
- Built-in Automatic Lead Angle Function
- Built-in Speed Feed-back Function
- 180° Commutation Sine Wave Drive (2-phase Modulation)
- Built-in Charge Pump
- Forward Rotation / Reverse Rotation Switch Function
- Variable Speed Control, Standby Command Function (PWM / DC Input Support)
- Selectable Output Modes / Dead Time
- Soft Start, Soft Stop Setup Function
- Built-in Protective Functions
  Over Voltage Protection (OVP),
  Under Voltage Lockout (UVLO),
  Over Current Limit (OCL),
  Over Current Protection (OCP),
  Lock Protection (LOCK), Thermal Shutdown (TSD),
  External Parts Thermal Shutdown (EXTSD),
  Abnormal Hall Input Detection (HALLERR)
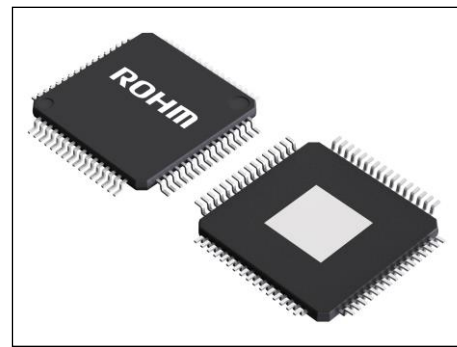 (Note 1) Grade 1

Key Specifications

- Supply Voltage Range: 6.5 V to 18 V
- Standby Current: 55 μA (Max)
- Operating Temperature Range: -40 °C to +125 °C

Package	W(Typ) x D(Typ) x H(Max)
HTQFP64AV	12.00 mm x 12.00 mm x 1.00 mm

HTQFP64AV

Applications

- Air Conditioning Blower Motor
- Battery Cooling Fan Motor

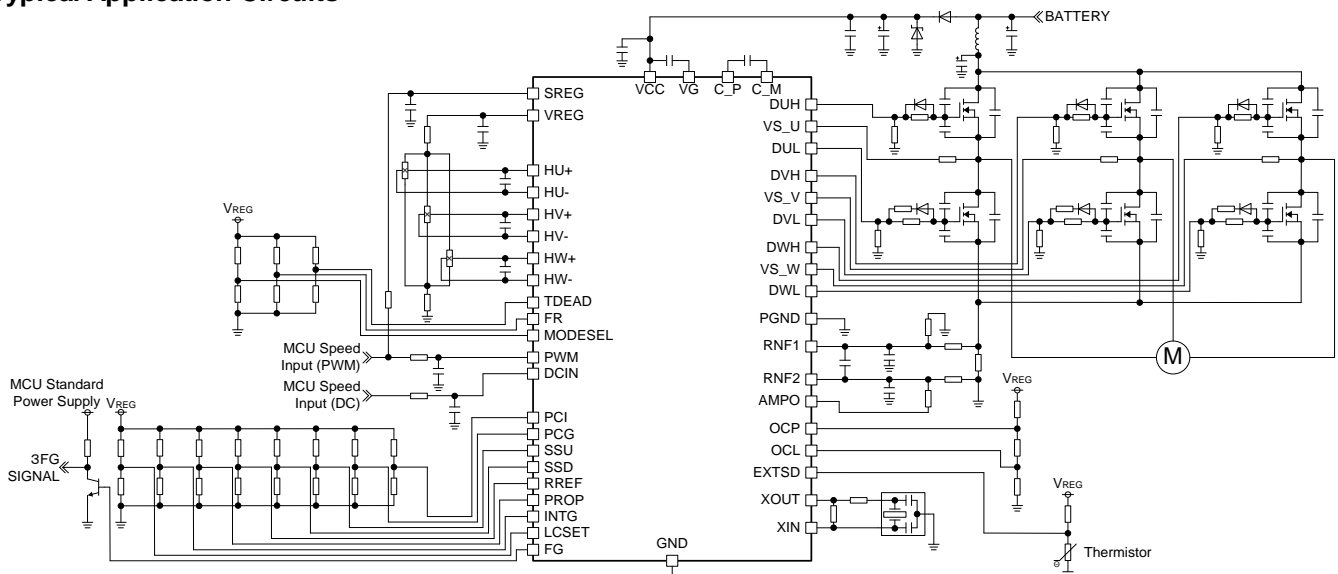## Typical Application Circuits

Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Contents

Pin Configuration

(TOP VIEW)

Figure 2. Pin Configurations

Pin Descriptions

No.	Pin Name	Function	No.	Pin Name	Function
1	PCI	Lead angle control Initial torque setup	26	N.C	-
2	TEST4	TEST4	27	DUL	U phase low side MOS-FET drive output
3	TEST3	TEST3	28	N.C	-
4	FG	Rotational speed / diagnostics result output	29	VS_U	U phase output
5	N.C	-	30	DUH	U phase high side MOS-FET drive output
6	XIN	External CLK input	31	N.C	-
7	N.C	-	32	PGND	POWER GND
8	XOUT	External CLK output	33	C_M	Charge pump capacitor minus side connection
9	N.C	-	34	N.C	-
10	EXTSD	External parts temperature detection	35	C_P	Charge pump capacitor plus side connection
11	OCL	Over current limit setup	36	N.C	-
12	OCP	Over current protection setup	37	VCC	Power supply
13	AMPO	Amplifier output	38	VG	Charge pump output
14	RNF1	Current detection 1	39	N.C	-
15	GND	GND	40	TEST1	TEST1
16	RNF2	Current detection 2	41	TEST2	TEST2
17	DWL	W phase low side MOS-FET drive output	42	GND	GND
18	N.C	-	43	HU+	U phase plus side hall signal input
19	VS_W	W phase output	44	HU-	U phase minus side hall signal input
20	DWH	W phase high side MOS-FET drive output	45	HV+	V phase plus side hall signal input
21	N.C	-	46	HV-	V phase minus side hall signal input
22	DVL	V phase low side MOS-FET drive output	47	HW+	W phase plus side hall signal input
23	N.C	-	48	HW-	W phase minus side hall signal input
24	VS_V	V phase output	49	VREG	Internal reference power supply
25	DVH	V phase high Side MOS-FET drive output	50	SREG	Internal reference power supply

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Pin Descriptions – continued

No.	Pin Name	Function	No.	Pin Name	Function
51	N.C	-	59	SSU	Soft start spin up time setup
52	DCIN	DC signal input	60	SSD	Soft start spin down time setup
53	N.C	-	61	PROP	Speed control gain setup (proportional control)
54	PWM	PWM signal input	62	INTG	Speed control gain setup (integral control)
55	TDEAD	Dead time select	63	RREF	Speed control maximum rotation setup
56	MODESEL	I/O mode select	64	PCG	Lead angle control gain setup
57	FR	Forward / Reverse select	-	EXP-PAD	Connect a EXP-PAD on GND
58	LCSET	Lock protection time setting			

Block Diagram

Figure 3. Block Diagram

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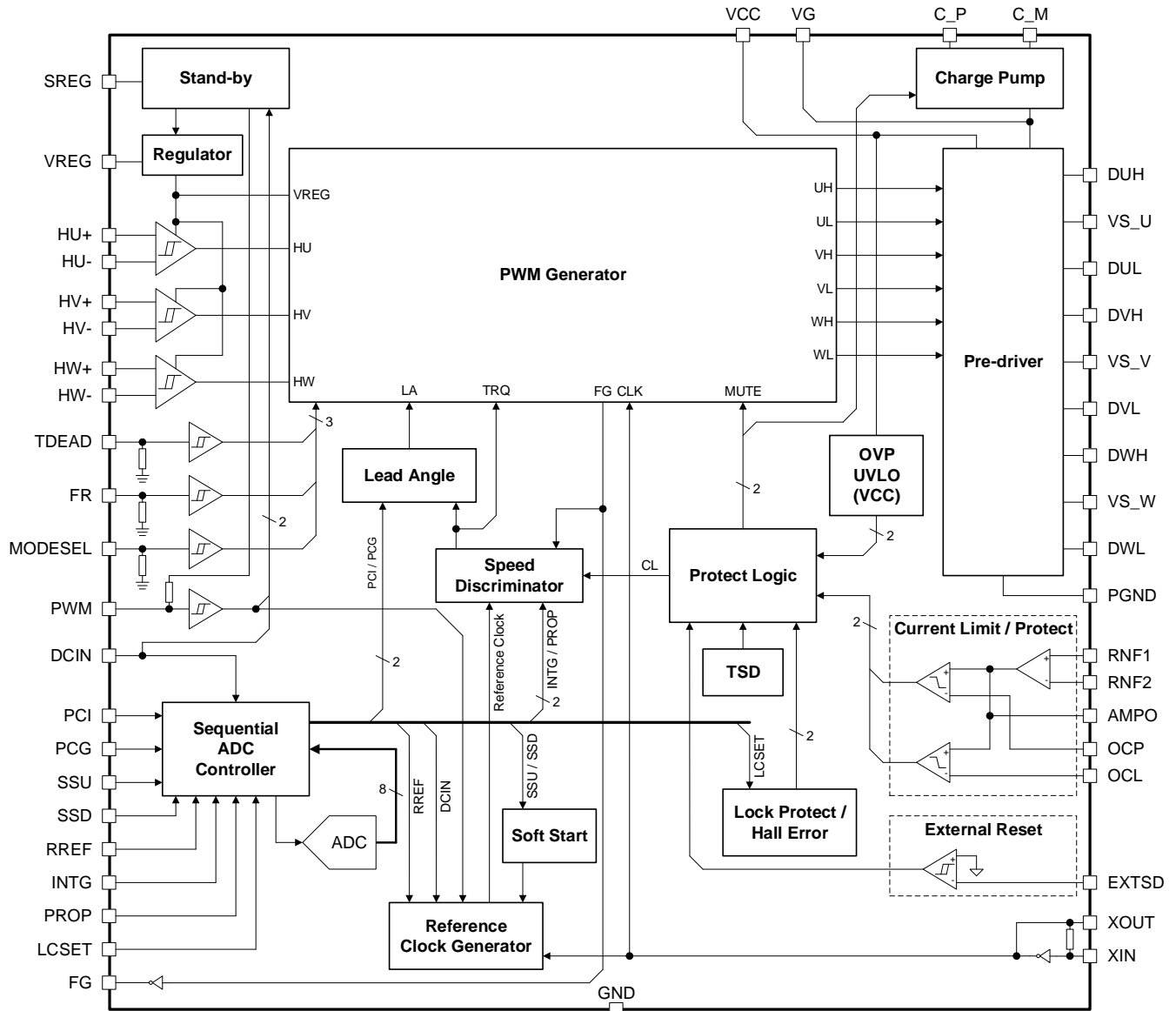## Description of Operation (Note 1)

(Note 1) The characteristic of time and frequency on condition that 10 MHz frequency is input on the XIN pin.

1. Operation Overview

(1) Operation Mode Overview (Note 2)

	FR	Low		High		Low		High	
Condition	Rotational Direction Setup	CCW (U to W to V)		CW (U to V to W)		CCW (U to W To V)		CW (U to V to W)	
	Rotational Direction Detection	CCW Direction (Reverse Rotation)		CW Direction (Forward Rotation)		CW Direction (Forward Rotation)		CCW Direction (Reverse Rotation)	
	Number of Rotation (Hall Cycle) *(Note 3)*	Below 1.59 Hz	1.59 Hz or More	Below 1.59 Hz	1.59 Hz or More	Below 1.59 Hz	1.59 Hz or More	Below 1.59 Hz	1.59 Hz or More
Normal Operation	$PWM < D_{MINOFF1}$ or $PWM > D_{MAXOFF2}$ or $PWM < D_{MINOFF3}$ *(Note 4)*	Upper and lower arms OFF (Logic of low output for all gates)							
	$D_{MINON1} < PWM < D_{MAXON2}$ or $PWM > D_{MINON3}$ *(Note 4)*	120° commutation synchronous rectification	180° commutation synchronous rectification	120° commutation synchronous rectification	180° commutation synchronous rectification	120° commutation asynchronous rectification		120° commutation asynchronous rectification	

(Note 2) Lead angle function is not enabled in 120° commutation mode but enabled in 180° commutation mode at startup.
(Note 3) The hall cycle monitors the single phase signal (Electrical angle 360°) from the sweeping down of W phase (HW). (See P.7)
(Note 4) See Electrical Characteristics1. (See P.25)

When the hall signal opposite to the setup of direction of rotation (FR) is input, it performs in the 120° commutation drive and the asynchronous rectification, and high side arm output is operated in PWM. After that one cycle of the hall cycle is operated in the 120° commutation drive and the asynchronous rectification even if the same sequence is input as the setup of rotational direction. *(Note 5)*

(Note 5) Asynchronous rectification does not operate if the hall cycle is less than 1.59 Hz.

(2) Commutation Mode Logic

120° commutation drive (synchronous rectification, without lead angle) is adopted at startup; when the hall cycle becomes 3FG and 1.59 Hz or more for three cycles in a row, it is switched to 180° commutation drive (synchronous rectification). (See Figure 49, P.32 to 33 and Figure 50. Timing Chart)
High/Low arm output logic for the hall input of 120° commutation and 180° commutation is in the following tables.

Input / Output Logic of 120° Commutation Drive *(Note 6), (Note 7)*

HU	HV	HW	CW : clockwise						CCW : counter-clockwise					
			DUH	DVH	DWH	DUL	DVL	DWL	DUH	DVH	DWH	DUL	DVL	DWL
H	L	H	L	PWM	L	H	$\overline{PWM}$	L	PWM	L	L	$\overline{PWM}$	H	L
H	L	L	L	L	PWM	H	L	$\overline{PWM}$	PWM	L	L	$\overline{PWM}$	L	H
H	H	L	L	L	PWM	L	H	$\overline{PWM}$	L	PWM	L	L	$\overline{PWM}$	H
L	H	L	PWM	L	L	$\overline{PWM}$	H	L	L	PWM	L	H	$\overline{PWM}$	L
L	H	H	PWM	L	L	$\overline{PWM}$	L	H	L	L	PWM	H	L	$\overline{PWM}$
L	L	H	L	PWM	L	L	$\overline{PWM}$	H	L	L	PWM	L	H	$\overline{PWM}$

(Note 6) It becomes the asynchronous rectification at the reversal detection, and low output for PWM reversal output logic of low side arm output.

Input / Output Logic of 180° Commutation Drive *(Note 7)*

HU	HV	HW	CW : clockwise						CCW : counter-clockwise					
			DUH	DVH	DWH	DUL	DVL	DWL	DUH	DVH	DWH	DUL	DVL	DWL
H	L	H	L	PWM	PWM	H	$\overline{PWM}$	$\overline{PWM}$	PWM	L	PWM	$\overline{PWM}$	H	$\overline{PWM}$
H	L	L	L	PWM	PWM	H	$\overline{PWM}$	$\overline{PWM}$	PWM	PWM	L	$\overline{PWM}$	$\overline{PWM}$	H
H	H	L	PWM	L	PWM	$\overline{PWM}$	H	$\overline{PWM}$	PWM	PWM	L	$\overline{PWM}$	$\overline{PWM}$	H
L	H	L	PWM	L	PWM	$\overline{PWM}$	H	$\overline{PWM}$	L	PWM	PWM	H	$\overline{PWM}$	$\overline{PWM}$
L	H	H	PWM	PWM	L	$\overline{PWM}$	$\overline{PWM}$	H	L	PWM	PWM	H	$\overline{PWM}$	$\overline{PWM}$
L	L	H	PWM	PWM	L	$\overline{PWM}$	$\overline{PWM}$	H	PWM	L	PWM	$\overline{PWM}$	H	$\overline{PWM}$

(Note 7) L = Low, H = High.

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Description of Operation – continued

(3) Pin Setup

Setup to control functions such as rotational speed command (DCIN) the speed control (RPEF, INTG, PROP), lead angle control (PCI, PCG), soft start (SSU, SSD) and lock protection time setup (LCSET) is available by applying the divided resistance voltage of V_{REG} [(Note 1)] to the corresponding pin. Zero scale is GND, and for full scale is V_{REG}.
The applied voltage is read in the A/D Converter ("ADC").
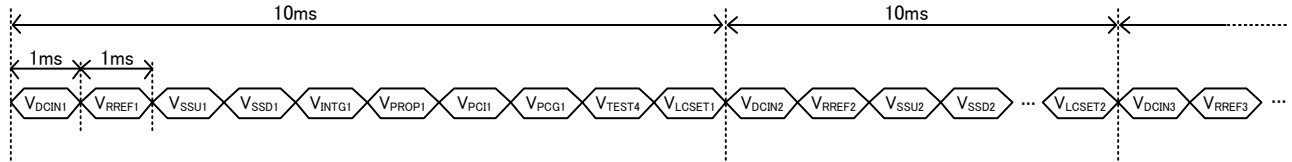
(Note 1) Set the input impedance to 5 MΩ or less.

Figure 4. ADC Operation Sequence

ADC takes samples of the pin voltage repeatedly in order to determine whether the parameter is required to update or not. The parameter does not change unless it exceeds the range of the default: ±1 LSB (V_{RREF1} in Figure 5).
Two conditions are required to be updated the parameter. To exceed the range of the default: ±1 LSB and to be within the range of ±1 LSB three times [(Note 2)] after the value has exceeded the default (V_{RREF7} in Figure 5).

(Note 2) If input is changed by resolution less than 2 LSB, the default may not be changed due to the above specifications.
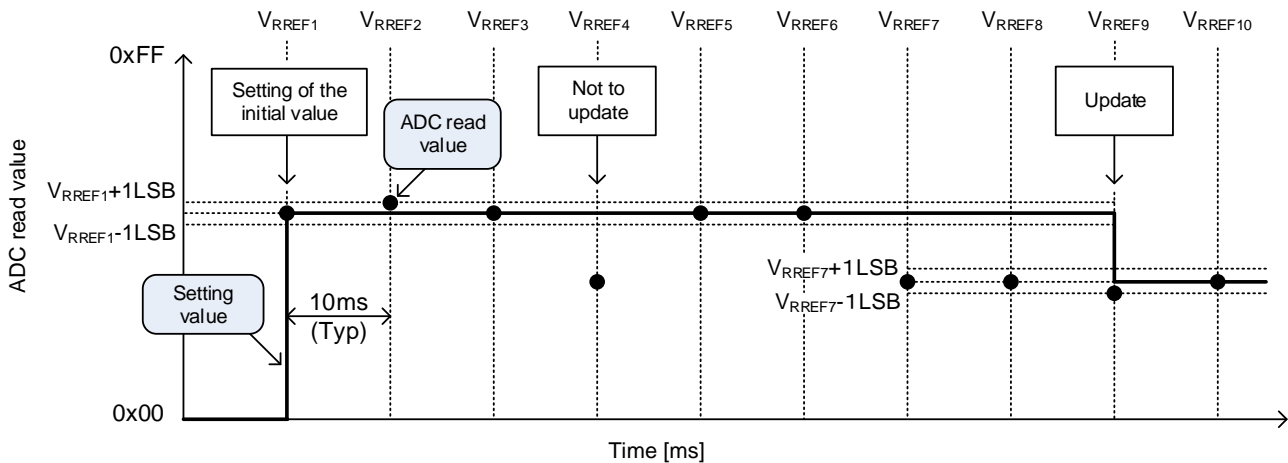

Figure 5. Update of the ADC Result

Description of Operation – continued

(4) Driving Waveform Generation

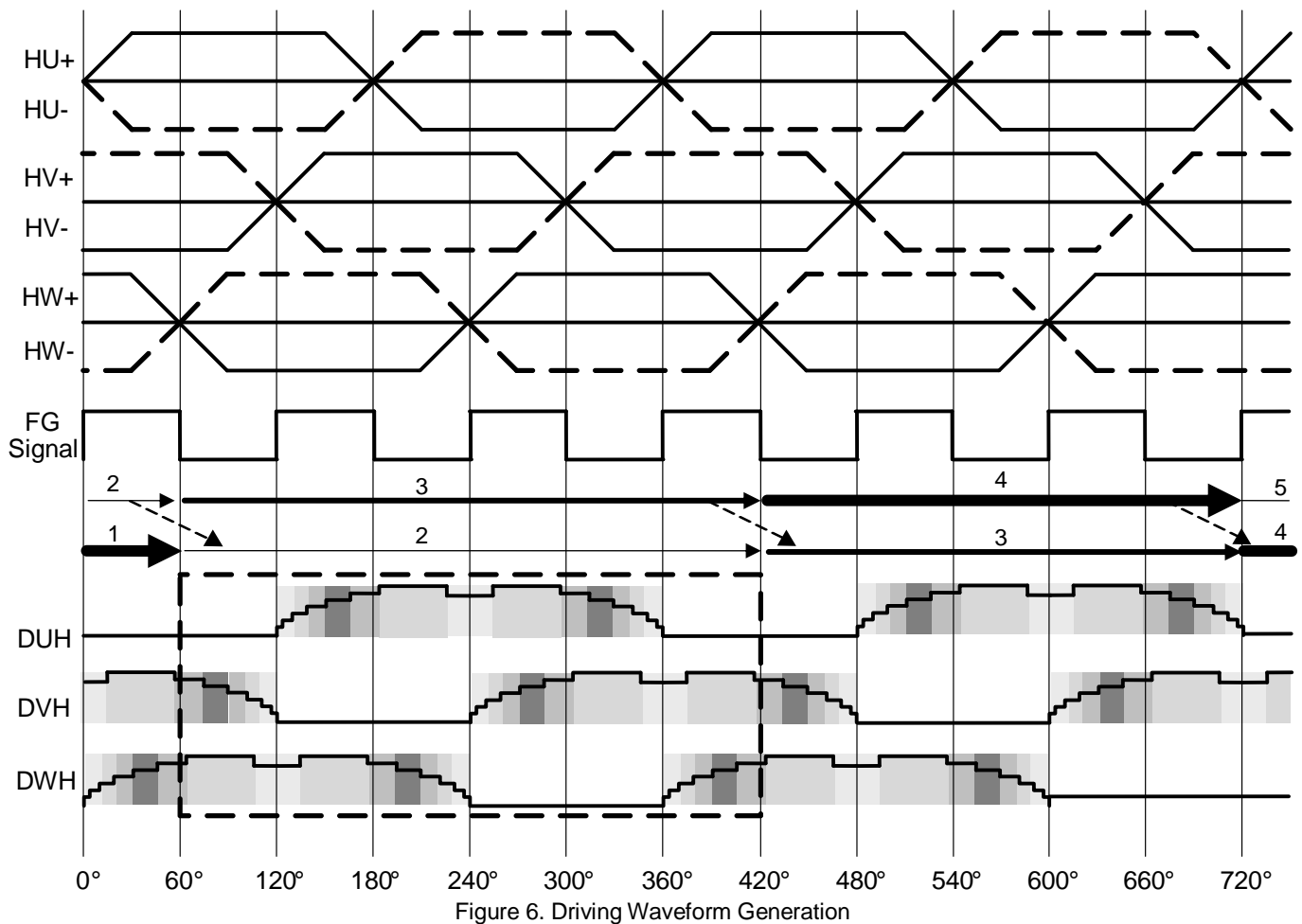Figure 6. Driving Waveform Generation

The timing to change the drive waveform is determined by monitoring of electrical angle between edges (Falling -> Rising) of W-phase (HW) hall signal (electrical angle 360°). The internal counter that generates the timing to change waveform is reset if the falling edge of the monitor signal is detected. Then the timing of change is updated.
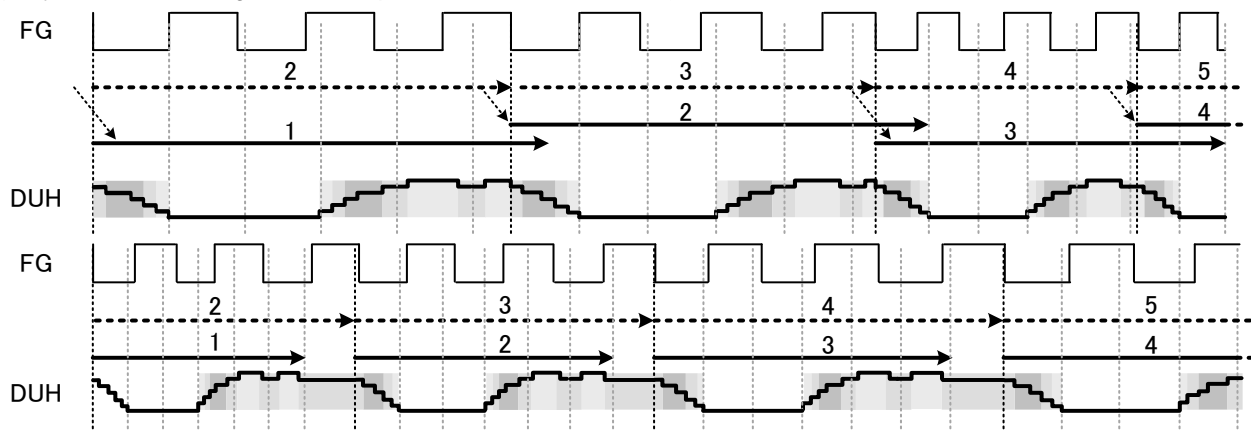(Duty is determined regardless of a phase in 120° commutation)

Figure 7. Example of Drive Waveform Generation (No lead angle) when sudden acceleration (Upper) /deceleration (Lower)

The switching point of the cycle is faster than expected when sudden acceleration. In this case the next 360° pattern is output from the switching point, the pattern is output in the expected electrical angle from the previous cycle. In reverse when sudden deceleration, the switching point of the cycle is later than expected so the duty corresponding to the finished 360° pattern is maintained. Duty becomes discontinuous when sudden acceleration or deceleration, if cycle change is larger, the current distortion is larger. The current distortion can be reduced by Soft Start that can extend the time of acceleration/deceleration. (See P.15 Soft Start).

Description of Operation – continued

(5) Standby Circuit

The PWM pin can be used as the command of rotational speed by Duty of High/Low; however, if the voltage fixed as High is applied, it turns to standby mode (It is recognized as High due to the high impedance of the PWM pin and it is fixed to the internal voltage). Standby mode is canceled (turns to Active mode) if sweeping down of the PWM pin is once detected.

Standby mode and active mode can also be switched with the DCIN pin by applying ("> 0.3 V (Typ)" in the table below) or not applying ("< 0.15 V (Typ)" in the table below) DC voltage.

The PWM input has priority if PWM and DCIN are input at the same time; however, such operation should be avoided as it may cause malfunction. (See Figure 9)

In addition, when PWM is Low and VCC power turns on, standby is maintained and a motor does not operate. Please input PWM after SREG becomes the stable.

		PWM Pin Logic	
		Fixed to Open(Hi-Z) or High [(Note 1)] or PWM ≤ 19.0 Hz, PWM ≥ 1.25 kHz	Fixed to Low [(Note 2)] or PWM(20 Hz to 800 Hz)
DCIN Pin voltage	< 0.15 V (Typ)	Standby mode	Active mode (PWM input)
	> 0.3 V (Typ)	Active mode (DC input)	Active mode (PWM input)

[(Note 1)] It is fixed to High when it is at least 513 ms(19 Hz) and PWM≥ V_{SREG} ×0.8.
[(Note 2)] It is fixed to Low when it is at least 53 ms(19 Hz) and PWM≤ V_{SREG} ×0.4.
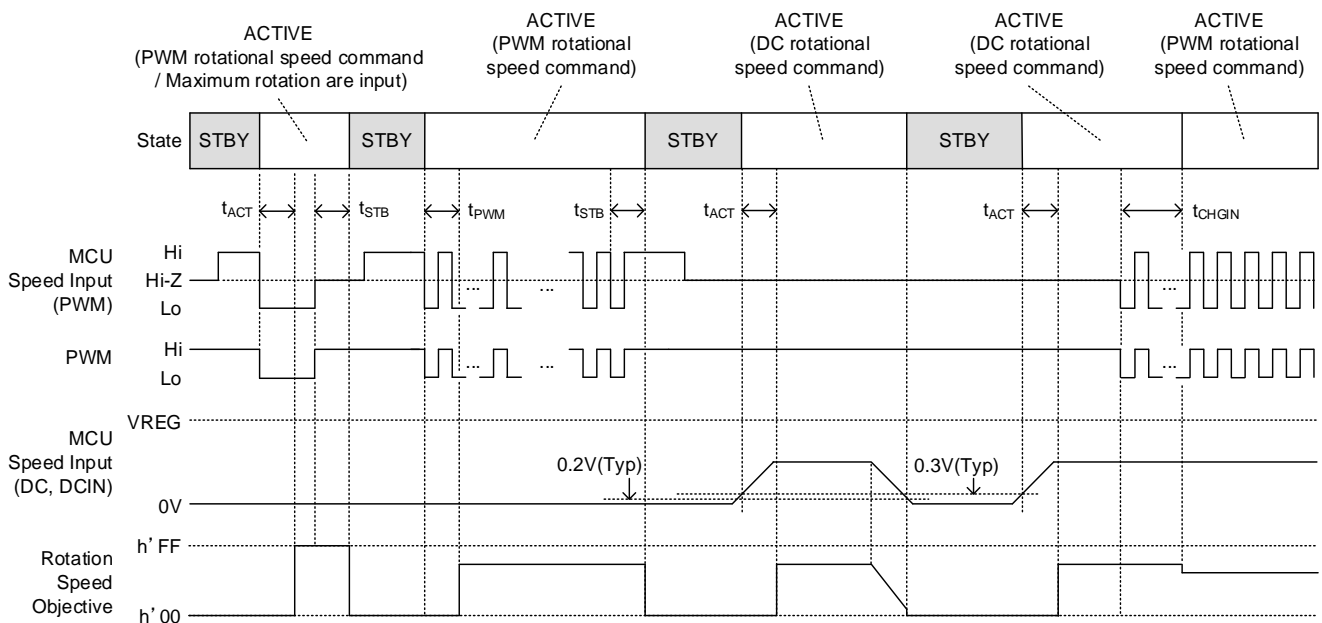

Figure 8. Transition to Standby and Recovery Operation [(Note 3)]

[(Note 3)] t_{ACT} is the time from internal power supply VREG is within guaranteed value V_{REG} to output starts, it requires max 53 ms (PWM sampling time: 19 Hz) + Approx.1 ms (Depending on clock cycle).
t_{STB} is the time before abnormal input is detected (Open or High fixed or PWM ≤ 19.0 Hz, PWM ≥ 1.25 kHz). If abnormal input more than 513 ms(Typ) is detected, it switchess to STBY. Torque to motor is changed according the time set by SSU/SSD.

(6) Rotational Speed Command

DC input or PWM input can be selected for Rotational speed command. When using the PWM input, rotation speed command value is input by changing the duty of PWM (Low active input). If frequency of PWM ≤ 19.0 Hz, PWM ≥ 1.25 kHz is input into the PWM pin, it switches to standby mode due to noise. Please insert appropriate filter [(Note 4)] for the PWM pin.

When using DC input, rotation speed command value is input by applying voltage directly to the DCIN pin. In consideration of the noise between wires when applying voltage, make sure to insert an appropriate filter [(Note 4)] not to exceed the rated voltage of the DCIN pin.

[(Note 4)] Please consider the pin impedance when filter is configured. Please refer to H level input current of each pin (PWM, DCIN) in Electrical characteristic 2.
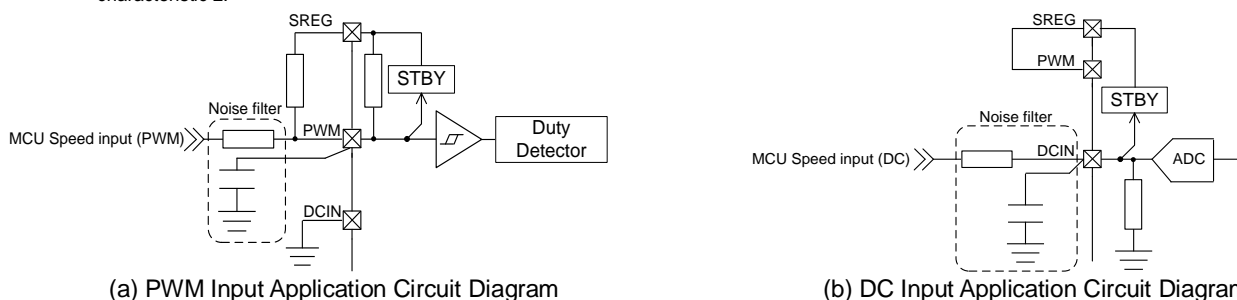
(a) PWM Input Application Circuit Diagram   (b) DC Input Application Circuit Diagram
Figure 9. Rotational Speed Command Input Application Circuit Diagram for Transition to Standby and Recovery Operation

Description of Operation – continued

(7) Input / Output Mode Select

The input/output mode can be selected with the setup voltage of the MODESEL pin.
Avoid to switch the input/output mode during operation. [(Note 1)]

(Note 1) To switch the MODESEL pin during operation is unexpected. If MODESEL is switched when PWM = 100 % input, the target value of rotational speed is changed according to soft start setup value.

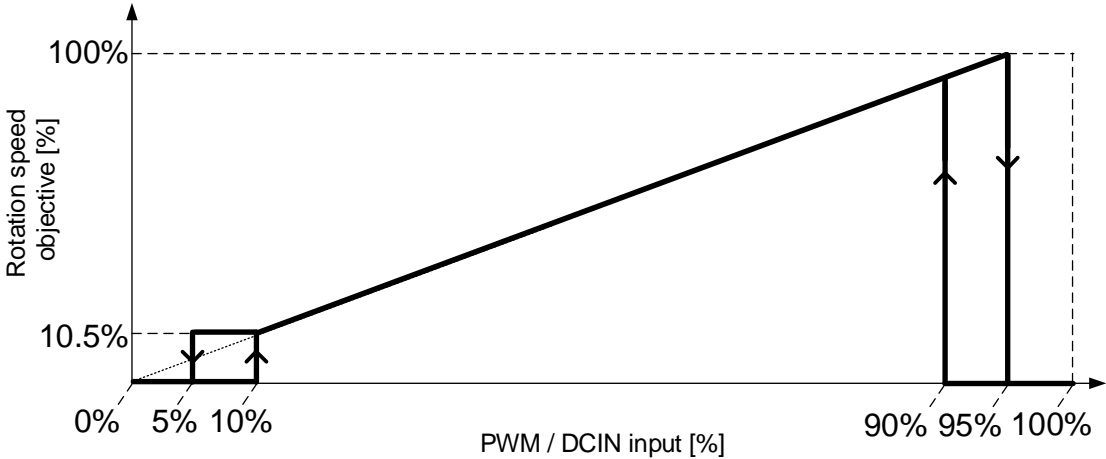|	MODESEL Pin Logic	
	Low : 0 V to V_{REG}×0.2	High : V_{REG}×0.6 to V_{REG}
Output mode	I mode	II mode

Figure 10. I Mode Rotation Speed Objective vs PWM Input Duty / DCIN Input Voltage[(Note 2)]
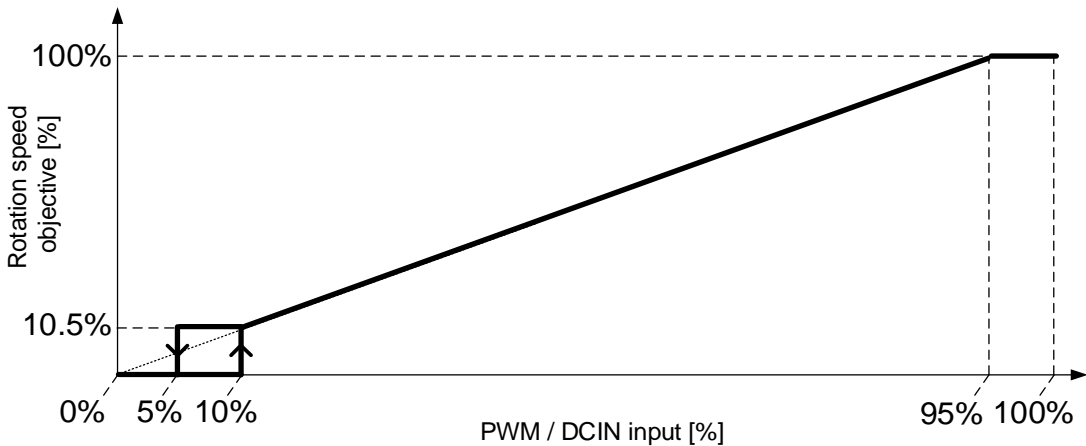(MODESEL = Low)

Figure 11. II Mode Rotation Speed Objective vs PWM Input Duty / DCIN Input Voltage[(Note 2)]
(MODESEL = High)

(Note 2) PWM input is pulse input duty and DCIN input is the ratio of DCIN voltage to VREG. These are shown in percentage as the above.

Description of Operation – continued

2. Commutation Angle Control
(8) Phase relation of Voltage and Current, Lead angle setup
Phase relation of voltage and current is shown when the lead angle on the pre-driver side is set to 0° in Figure12.
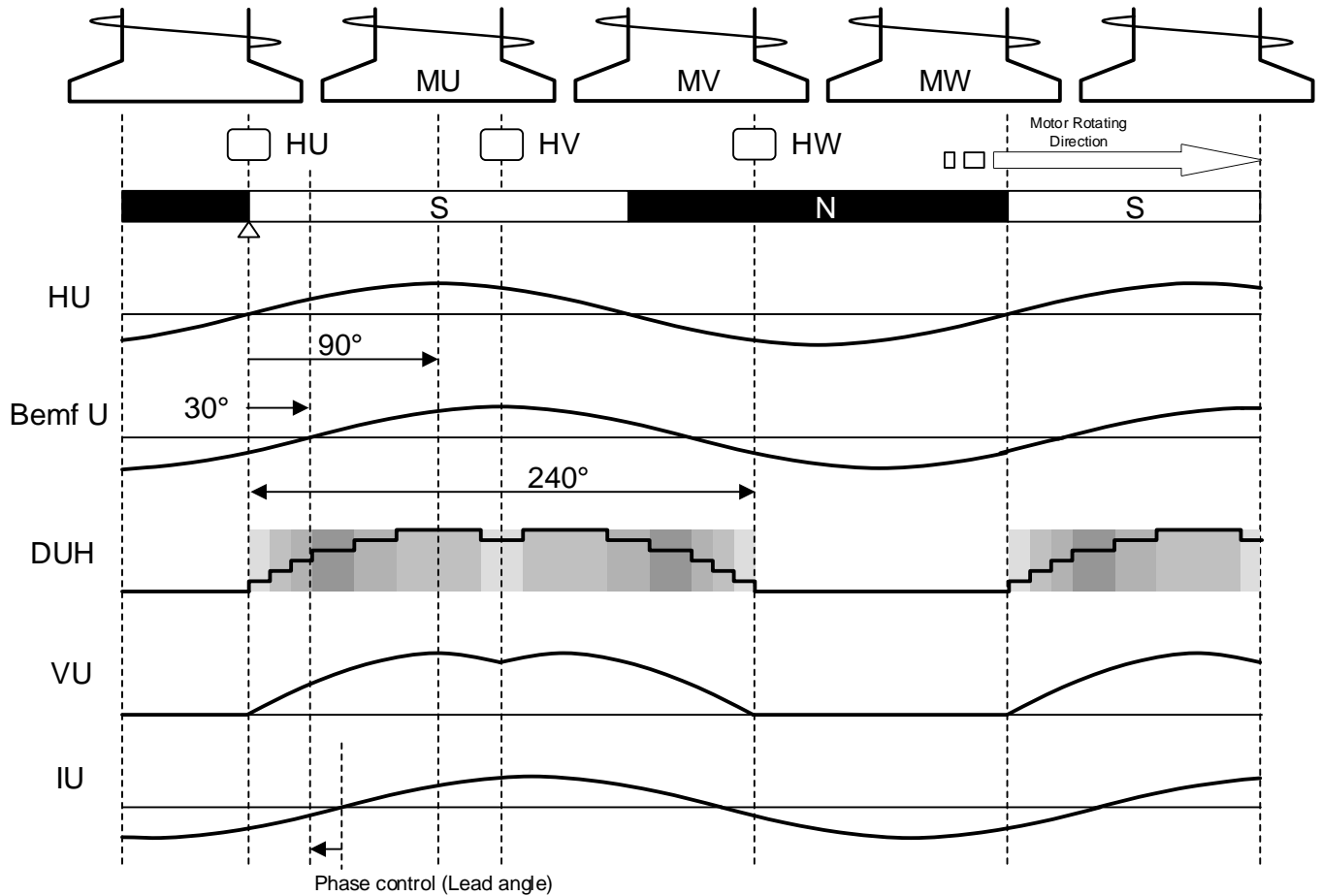
6pole, 9slot
(P:S = 2:3)

Figure 12. Phase Relation of Voltage and Current of a Brushless Motor (Delta Connection, 6 poles/ 9 slots)

The output switching of the DUH (Pre-driver U phase output High side signal) [Note 1] starts to rise U phase hall signal (HU). The zero-cross point of the U phase inductive voltage (Bemf U) is located 30° delayed from the rising of the U phase hall signal, and the phase of the U phase winding current (IU) is generally delayed than the inductive voltage. The motor power is not efficient in this state, but it can be more efficient by advancing (performing a lead angle) the phase of winding current.

To optimize, the zero-cross point of the inductive voltage and the zero-cross point of the winding current should be matched. By using the lead angle setup function of the controller, set the PCI/PCG pin voltage so that the zero-cross point of the current is located 30° delayed from the rising of the U phase hall signal.
   (Note 1) Low side output signal DUL is the inversion logic of DUH.

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Description of Operation – continued

(9) Lead Angle Control Setup

To set the lead angle value, connect the resistors (R_{PCI}, R_{PCG}) to the PCI and PCG pins as follows.

The torque to start the lead angle control can be adjusted with a constant of R_{PCI} and the tilt of the lead angle amount against torque can be adjusted with a constant of R_{PCG}.　The torque is equivalent to D*H output and D*L output Duty (TRQ Duty). The lead angle value coupled with torque can be calculated based on TRQ Duty [Note 1]. In addition, maximum lead angle is 30°. Please consider that the lead angle value is saturated at 30° although the lead angle value is set to more than 30° by RPCG.

(Note 1) See <TEST Pin>. (P.23) for the description of TRQ Duty.

To set a fixed lead angle, set the PCI pin and the PCG pin to GND and adjust the stator and hall positions [Note 2] as shown in Figure 13. (In the example in Figure 13, the stator and the hall are located to set the lead angle to zero.)

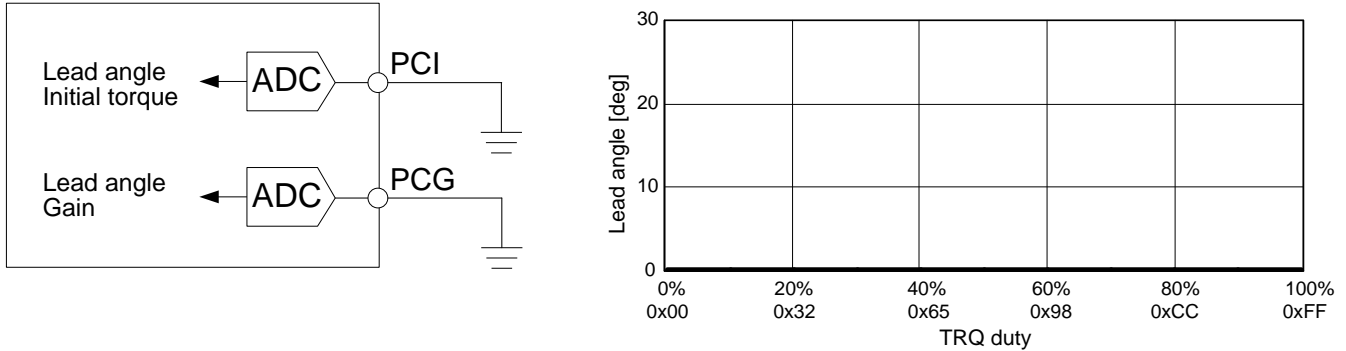*(Note 2)* See Figure 12 and design for the phase relation of the stator and hall positions.

Figure 13. Example of Fixed Lead Angle Setup (Zero lead angle in Driver Side)

To set a lead angle that is changed along with the torque TRQ Duty, an external circuit can be configured as shown in Figure 14.
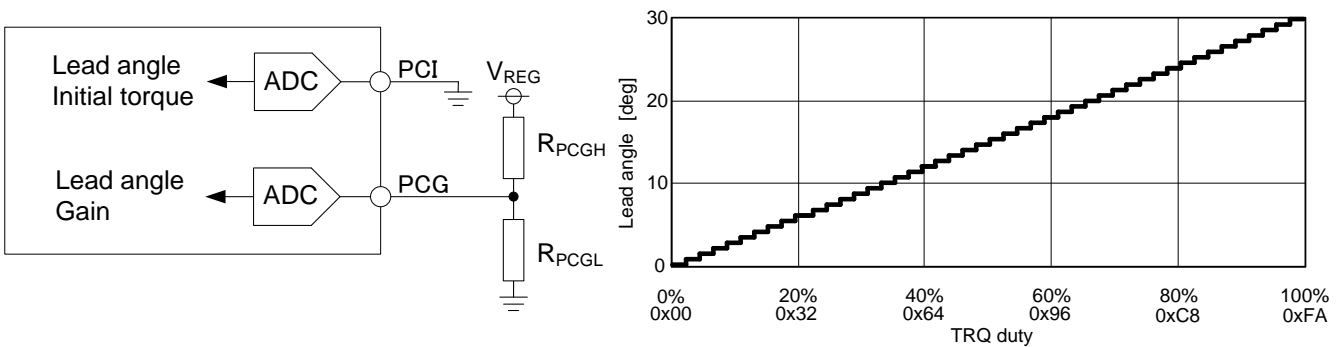

Figure 14. Example 1 of the Lead Angle Gain Setup Changed Along with the Torque

The lead angle amount G_{PCG} against TRQ Duty [%] is calculated using the below formula. *(Note 3)*

(Note 3) Minimum resolution of lead angle setup is 0.47°.　Lead angle value does not change unless the lead angle value in the following formula is more than 0.47° resolution.

$$G_{PCG} = \frac{R_{PCGL}}{R_{PCGH} + R_{PCGL}} \times 119.85 \times TRQ\,Duty\,[\text{deg}]$$

$$\therefore G_{PCG} \leq 30\,[\text{deg}]$$

Example) When $\dfrac{R_{PCGL}}{R_{PCGH} + R_{PCGL}} = \dfrac{1}{2}$, TRQ duty = 75 %,

$$\frac{1}{2} \times 119.85 \times 0.75 \geq 30, \quad \therefore G_{PCG75\%} = 30\,[\text{deg}]$$

When TRQ duty = 25 %,

$$\frac{1}{2} \times 119.85 \times 0.25 = 14.98 \quad \therefore G_{PCG25\%} = 14.57\,[\text{deg}]$$

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Conduction Angle Control Setting – continued
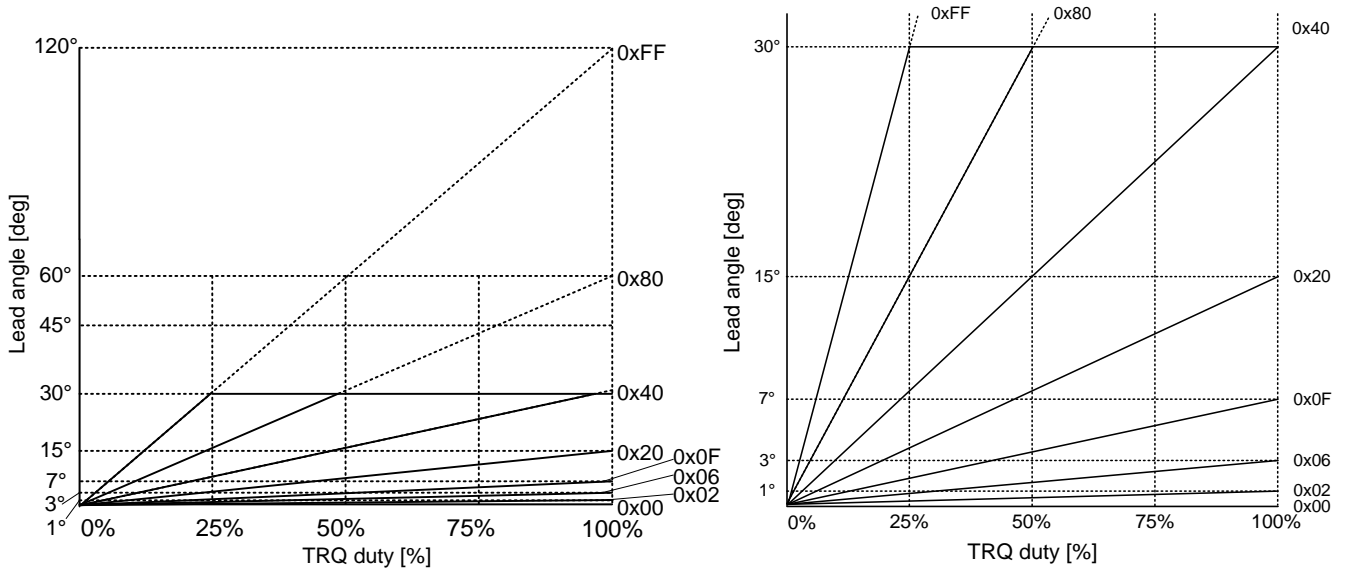
(a) Example 2 of the Torque Lead Angle Gain Setup   (b) Example 2 of the Torque Lead Angle Gain Setup (Enlarged)
Figure 15. Example 2 of the Lead Angle Gain Setup Changed Along with the Torque

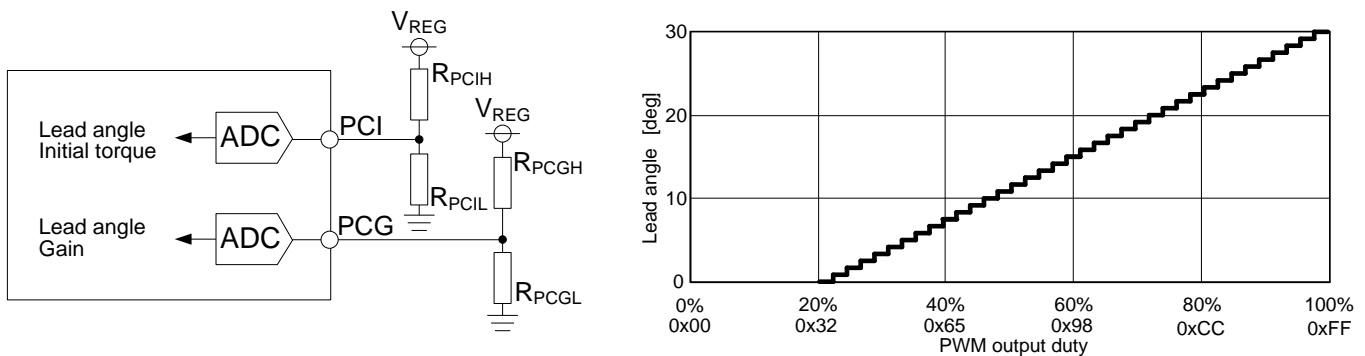The torque T_{PCI} to start the lead angle can be calculated by using the formula below.

Figure 16. Example 3 of the Lead Angle Initial Torque Setup Changed Along with the Torque

The torque T_{PCI} to start the lead angle can be calculated by using the formula below.

$$T_{PCI} = \frac{R_{PCIL}}{R_{PCIH} + R_{PCIL}} \times 100 [\%]$$

Example) When $\dfrac{R_{PCIL}}{R_{PCIH} + R_{PCIL}} = \dfrac{1}{2}$, the lead angle initial torque will be: $T_{PCI} = \dfrac{1}{2} \times 100\% = 50\%$

The lead angle value is updated every eight cycles of the W phase hall signal, and the change in value per one update is 0.47° step.
For example, when the lead angle setup is changed from 0° to 30°, the lead angle will be changed from 0° to 30° in 255 revolutions with a 4-pole motor.
With a 6-pole motor, the lead angle will be changed from 0° to 30° in 170 revolutions.

4-pole motor: $\dfrac{30[\text{deg}] \times 8[\text{period}]}{0.47[\text{deg}] \times 4[\text{pole}]/2} = 255 \text{ [revolutions]}$

6-pole motor: $\dfrac{30[\text{deg}] \times 8[\text{period}]}{0.47[\text{deg}] \times 6[\text{pole}]/2} = 170 \text{ [revolutions]}$

10-pole motor: $\dfrac{30[\text{deg}] \times 8[\text{period}]}{0.47[\text{deg}] \times 10[\text{pole}]/2} = 102 \text{ [revolutions]}$

Description of Operation – continued

3. Speed Control

(10) Speed Control

The rotational speed of the motor is controlled by the feedback to be constant rotation according to the rotational speed commands input from the PWM pin or the DCIN pin (Figure 18). The target of rotational speed by the feedback (REFCLK) is set with "the maximum rotational speed determined by RREF" and with "the ratio of the rotational speed target against the maximum rotational speed determined by PWM Duty or the DCIN voltage for V_{REG}" (Figure 18. 1, 2).

[Setup of the Maximum Rotation Speed]

The maximum rotational speed can be set by applying voltage divided from V_{REG} on RREF. Set the resistance ratio of RREF in reference to the theoretical formula below.

$$f_{MAXRPM} = (300-50) \times \frac{R_{REF}}{V_{REG}} + 50 \text{ [Hz]}$$
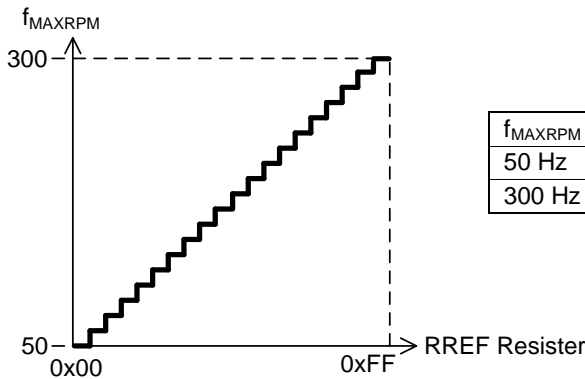
f_{MAXRPM}	Pole = 4	Pole = 6	Pole = 10
50 Hz	1500 rpm	1000 rpm	600 rpm
300 Hz	9000 rpm	6000 rpm	3600 rpm

Figure 17. Setup of the Maximum Rotational Speed

REFCLK is calculated with the following formula.

$$f_{MAXRPM} \times Duty_{PWM} = 160\text{Hz} \times 0.5 \text{ [Hz]}$$

[Example] If $f_{MAXRPM} = 160\text{Hz}$, $pole = 10$, $Duty_{PWM} = 50\%$, $REFCLK = 80\text{Hz}(960\text{rpm})$.

The frequency of REFCLK and FG generated in the hall comparator are compared and the difference is input to the loop filter in order to determine the torque (TRQ) of the motor. (Figure 18. 3, 4, 7)
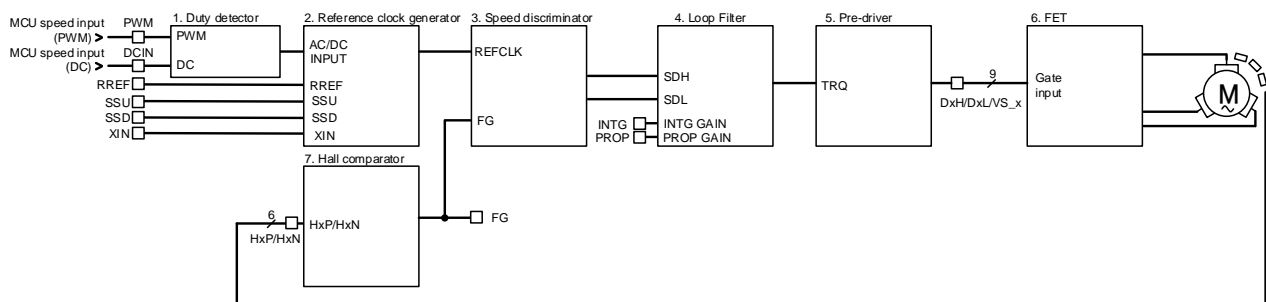
Figure 18. Configuration of Speed Control

f_{MAXRPM} depends on CLK signal to input on the XIN pin[Note 1] (Refer to [Setup of Maximum Rotational Speed] in case f_{XIN} is 10 MHz.

(Note 1) Refer to (18) XIN, XOUT (P.17) for the XIN and XOUT pins.

If command value is input from DCIN, ADC filter is operated as mentioned in "1-(3) Pin Setup". Command values for DCIN are changed with 2 LSB step but no change with 1 LSB or less because setup values are updated if the values changes more than 1 LSB.

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Speed control – continued

Torque (TRQ) of Speed Control is set as follows.
Block configuration of Speed Control is as follows.
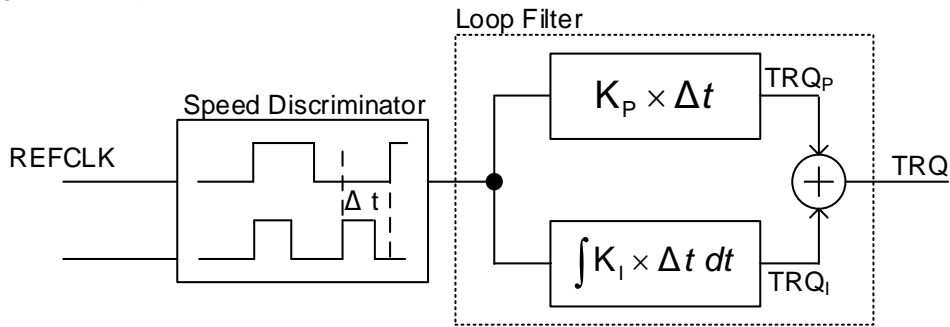
Figure 19. Block Configuration of Speed Control

Cycle difference Δt of target rotational speed (REFCLK) and actual rotational speed (FG) is counted. Based on Δt, torque calculated at proportioned control: TRQ_P and torque calculated at integral control: TRQ_I are added to determine torque. Formula is as follows.

$$TRQ = TRQ_P + TRQ_I ,$$

$$TRQ_P = K_P \times \Delta t , \quad TRQ_I = \int (K_I \times \Delta t) dt \qquad \therefore K_P = PROP , \quad K_I = INTG$$

Convergence time (From generation of motor rotational fluctuation to stability as target rotational speed) is determined by that the KP (constant of proportionality) set by the PROP pin and the KI (constant of integration) set by the INTG pin. Torque gain is set by K_P and K_I, TRQ_P and TRQ_I are changed as Figure 20.
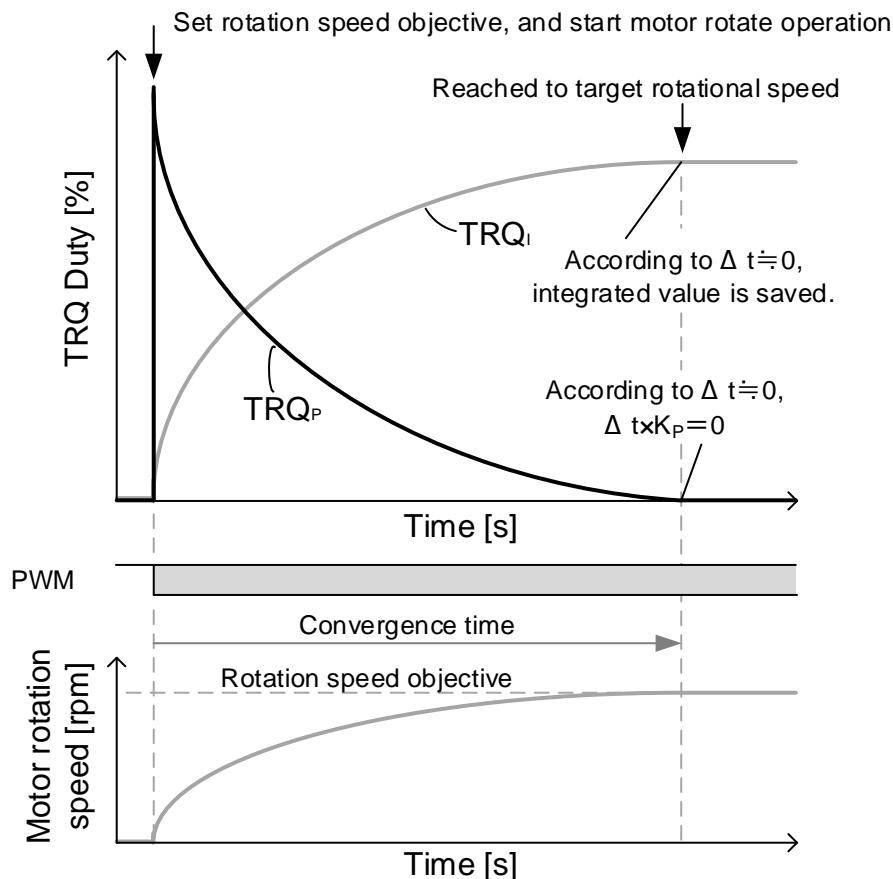
Figure 20. Transitions of TRQ_P and TRQ_I by Speed Control

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Description of Operation – continued

(11) Soft Start

A driving torque is input into a motor to get closer to the target rotational speed when the rotational speed command value is input by PWM or DCIN. The reliability of MOSFET may be damaged by inrush current if there is large torque in starting at once, etc.

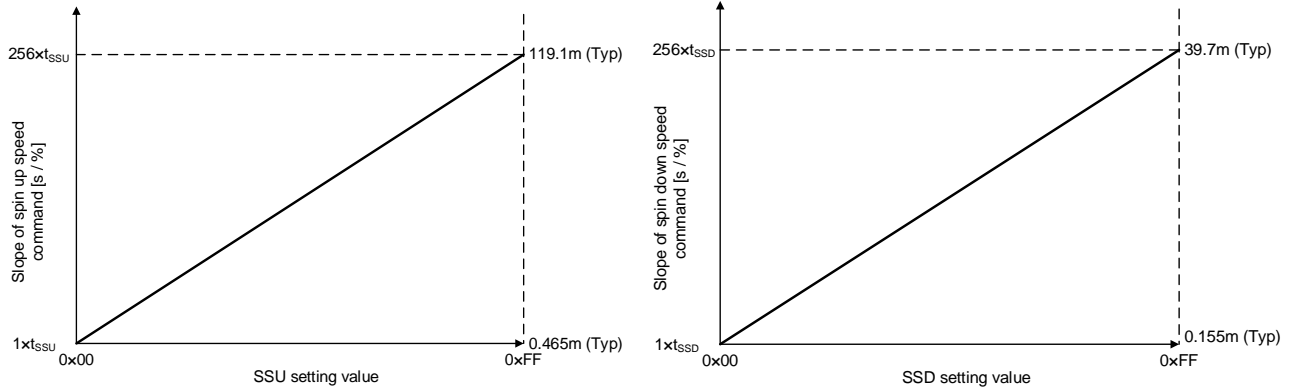Inrush current on MOSFET can be suppressed by setting a slope for the target rotational speed and setting time of Spin up/down. The SSU pin is to set Spin up time and SSD is to set Spin down time. The slopes for change of rotational command against time are specified.

(a) Spin Up Time Setup   (b) Spin Down Time Setup

Figure 21. Spin Up / Down Time Setup

The slope of the shift of rotational speed command during Spin up/down can be set in integral multiple (1 to 256) of minimum set point t_{SSU} and t_{SSD} Spin up / Spin down.

t_{SSU} = 0.465m [s/%] (Typ)
t_{SSD} = 0.155m [s/%] (Typ)

For example, the slope of the target rotational speed command value during Spin up is in 0.1 [s/%],

$$\frac{0.1[s/\%]}{0.465m[s/\%]} = 215.1$$

Apply voltage divided resistance from V_{REG} voltage on SSU at the resistance ratio of 215/256.
If Spin down time is set in 0.01 [%/s],

$$\frac{0.01[s/\%]}{0.155m[s/\%]} = 64.5$$

Apply voltage divided resistance from V_{REG} voltage on SSD at the resistance ratio of 65/256.
The behavior of the target rotational speed against time is shown in Figure 22 if Spin up time is set as 119.1m [s/%] and Spin down time as 39.7m [s/%].
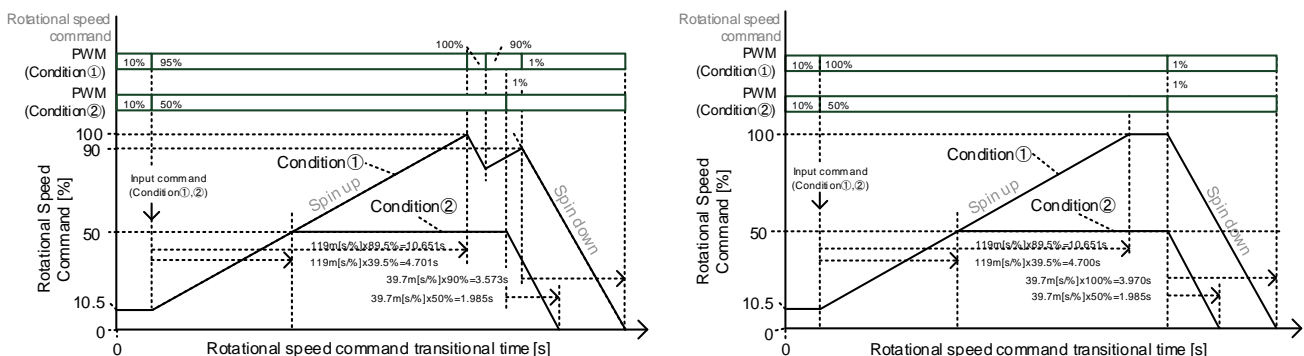
(a) Spin Up / Down in MODESEL=H   (b) Spin Up / Down in MODESEL=L

Figure 22. Change of the Rotational Speed Command Value (Condition: $V_{SSU} = V_{REG}$, $V_{SSD} = V_{REG}$)

If a rotational speed command value is input 10 % or more and Spin up like Figure 22, soft start operates from 10 % of max rotational speed in the slope of SSU setup value. If 100 % of rotational speed command value is input in 95 % like Figure 22 (a), soft down operates from 95 % of max rotational speed in the slope of SSD setup value. If a rotation speed command value is 0 % during the motor rotation, output goes Hi-Z and a motor stops with idling.

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Description of Operation – continued

4. Pin Function

(12) Charge Pump Circuit

The charge pump circuit to drive the external MOS-FET on the High side is built in.

Connect a 0.1 µF capacitor between C_M and C_P as well as a 0.1 µF capacitor between VG and VCC. Make sure to put the capacitor as close to the pin as possible to prevent voltage drop of the VG voltage.

If the over voltage protection circuit is activated, the charge pump is stopped and the boosting operation is stopped.

(13) Dead Time Setup Pin

Output dead time is set up on each output stage of the pre-driver (DUH and DUL, for example) so that the external MOS-FETs (High/Low) are not turned on at the same time.

The output dead time can be changed on the TDEAD pin.

	TDEAD Pin Logic	
	Low : 0 V to V_{REG} x 0.2	High : V_{REG} x 0.6 to V_{REG}
Output dead time	1.0 µs (Typ)	0.5 µs (Typ)

(14) VREG Output Pin

VREG output (5.0 V Typ) is built-in for the hall element bias, phase control setup and pull up of PINs.

Consider the maximum output current I_{VREG} when using. For stabilization, make sure to connect the capacitor at least 1 µF against GND.

If there is short failure against grounded capacitor or grounded by short between GND line and wire, VREG goes over maximum output current. Consider to put limit resistance, etc. if there may be grounded configuration or layout.

(15) Hall Input Pin

Set the bias current to the hall element so that the hall input voltage amplitude will be minimum input voltage of at least 35 mVpp and the in-phase input voltage range will be 0 V to V_{REG}-1.2 V.

If the hall input is affected by noise, put the capacitor as close to the pin as possible between inputs to eliminate noise.

(16) The FR Pin

The direction of rotation can be selected by the FR pin.

See Figure 49 and Figure 50 for the Timing Chart.

If FR signal is switched during motor rotation, the load is applied on MOS-FET by inrush current. Please consider allowable current of MOS-FET.

	FR Pin Logic	
	Low : 0 V to V_{REG} x 0.2	High : V_{REG} x 0.6 to V_{REG}
Rotation Mode	Reverse Rotation	Forward Rotation

(17) The FG Pin

FG output is 3 pulses output with electrical angle 360°.

If HALL signal cycle is 360° and less than 1.59 Hz (Low rotation detection = High), it outputs by Exclusive-OR of 3-phase HALL comparator output of HALL signal and the signal is changed to switch to High/Low in the cycle 1.59 Hz or more and electrical angle 360° divided by 6. FG signal with electrical angle 360° is not always output three pulses if motor is accelerated or decelerated rapidly as FG switching cycle is updated by electrical angle 360°.
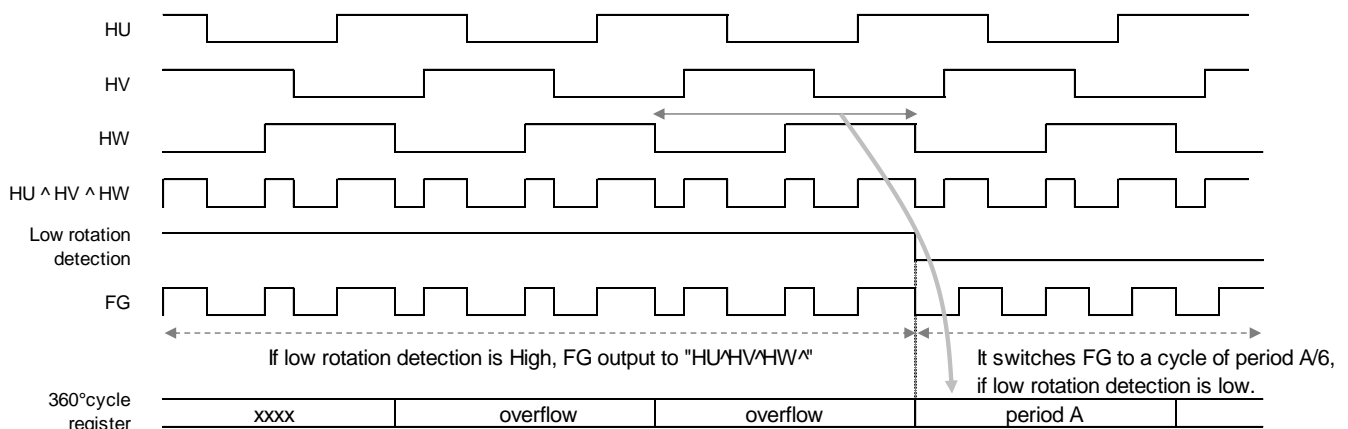

Figure 23. FG Signal

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The FG Pin – continued

If the protection is operated properly, Duty of FG signal can be changed by DIAG function [Note 1].
FG signal cycle is fixed as 10 Hz (Typ) when DIAG function is operated.
If protected time is shorter than 1 cycle of DIAG output, DIAG function works for three pulses at least.
FG signal Duty is output as follows according to each protection mode.
(Note 1) Duty of DIAG function is written as High active in FG pin logic. Please note that logic is reverted if connecting to an open collector circuit.

Protection mode	FG Signal Duty	DIAG Priority
Lock Protection, Abnormal Hall Input Detection	10 %	Low
Over Current Protection, Over Current Limit	90 %	↓
Thermal Shutdown, External Parts Thermal Shutdown	30 %	
Over Voltage Protection, Under Voltage Lockout	70 %	High

(18) The XIN, XOUT Pins
Please input the wave form of 10 MHz (Typ) frequency into XIN.
If oscillating circuit is necessary; connect a feedback resistance and
a ceramic resonator "CSTNE10M0G55A" between XIN and XOUT. [Note 2]
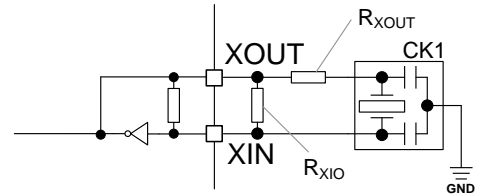*(Note 2)* Please refer to P. 34 Application Example for R_{XOUT} or R_{XIO}.

Figure 24. Example of Resonator Circuit Diagram

5. Protection
(19) Protection Mode
As the protection functions, Over Current Protection (OCP), Over Current Limit (OCL), Lock Protection (LOCK), Under Voltage Lockout (UVLO), Over Voltage Protection (OVP), Thermal Shutdown (TSD) External Parts Thermal Shutdown (EXTSD) and Abnormal Hall Input Detection (HALLERR) are built in. The protection is operated as follows except for Over Current Limit.

Protection Mode	Pre-driver Output (D*H)	Pre-driver Output (D*L)	Charge Pump Output (C_P, C_M)	Output Priority
Lock Protection	Low	Low	ACTIVE	Low
Abnormal Hall Input Detection				
Over Current Protection				
External Parts Thermal Shutdown				
Under Voltage Lockout				
Thermal Shutdown	Hi-Z	Hi-Z	Hi-Z	Mid
Over Voltage Protection [Note 3]	Low	High	MUTE	High

(Note 3) When Over Voltage Protection is activated, the charge pump output is turned to MUTE by pre-driver as the short brake regardless of other protection operations.

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Description of Operation – continued

(20) Over Current Protection

The over current protection circuit and the over current limit circuit can be configured, connecting a low resistor (Figure 25 R_{RNF}) for detection of current on the GND side of the external output stage, by an amplifier to amplifier the voltage of the both edges of R_{RNF} and a comparator to compare an amplifier output (AMPO) with the rated voltage the OCP, OCL pins.

If AMPO pin voltage goes over than the value set on the OCP pin due to generated voltage on R_{RNF}, all output stages of the pre-driver are switched to Low and latched at the same state. The filter is built in for the over current protection circuit to prevent malfunction. If the OCP comparator output is less than the noise mask time (10 μs Typ), it is ignored (See Figure 27 a). Please switch to STBY mode one time in order to deactivate over current protection.
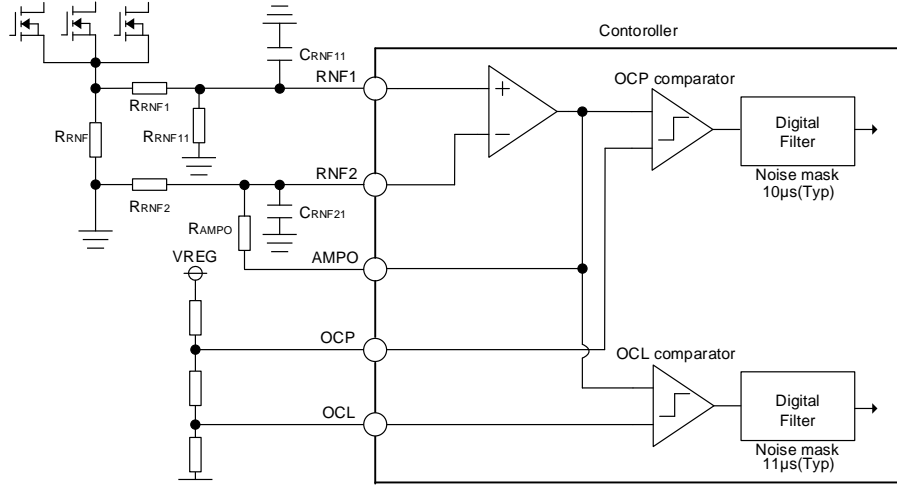

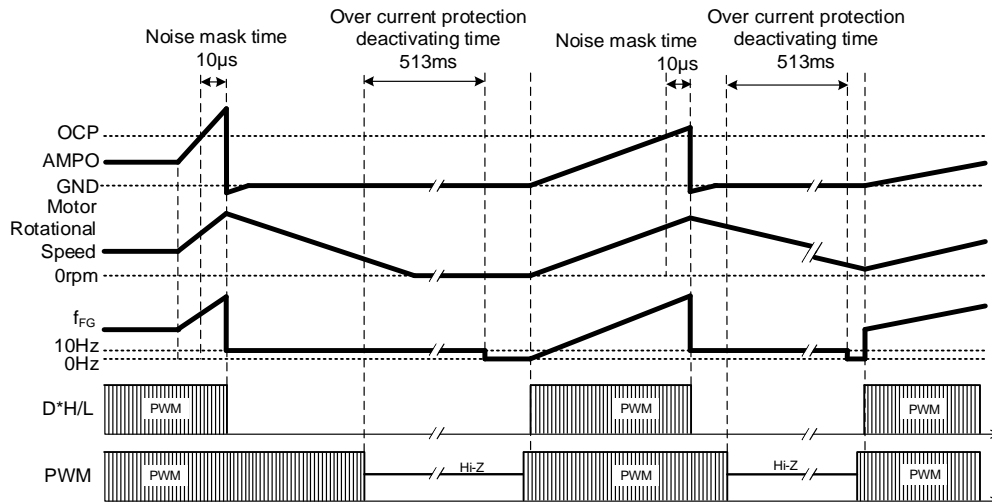Figure 25. Circuit Diagram Around Over Current Protection

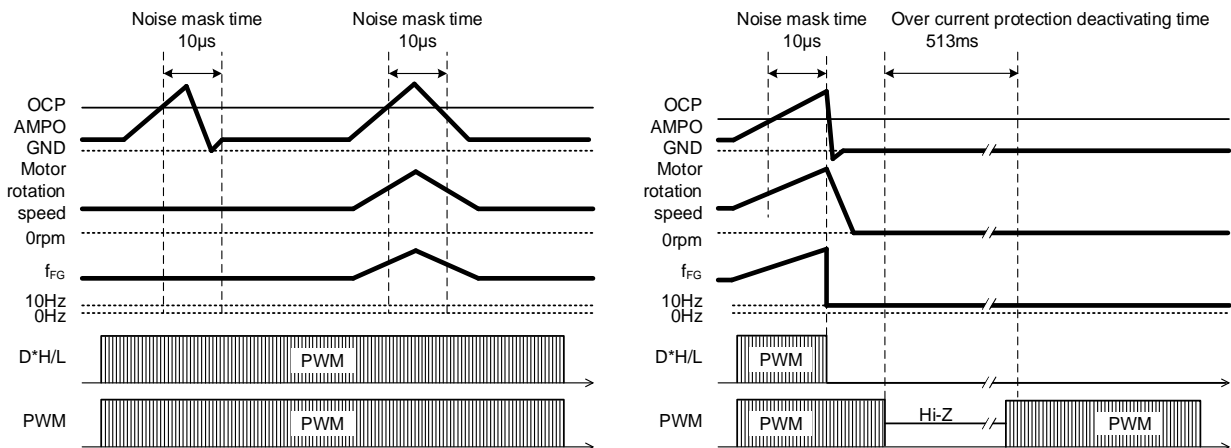Figure 26. Over Current Protection 1

(a) Noise Filter Operation
(No Over Current Detected in Mask Time)

(b) Over Current Protection Detection / Deactivating Operation
(No Recovery if not PWM Duty = 0 % During 513 ms)

Figure 27. Over Current Protection 2

Over Current Protection – continued

If a malfunction occurs due to noise that exceeds the mask time, it is recommended to add the external RC filter (See Figure 25 for R_{RNF1}, R_{RNF2}, C_{RNF11}, C_{RNF21}) while reviewing the board pattern. In this case, however, the external filter will increase the delay time until the protection circuit starts to operate. Make sure not to exceed the area of safety operation (ASO) of the external output stage MOSFET.

In addition, it is DIAG function works in Figure 26, Figure 27(b), but DIAG function stops with Standby mode to deactivate latch of protection state.

(21) Over Current Limit

Same as over current protection If the AMPO pin voltage goes over than the value set on the OCL pin due to generated voltage on R_{RNF} (Figure 25), it switches to the over current limit mode to limit torque to a motor. The over current limit mode is not able to be controlled against speed fluctuation because internal torque signal is reduced to less than OCL voltage. Please note that rotational speed is changed if the power supply voltage or load is changed.

Same as over current protection the filter is built in for the over current limit circuit to prevent malfunction. The pulse input less than the noise mask time (11 µs Typ) is ignored. DIAG function works in Figure 28. If the detection and recovery for shorter time than one cycle as over current limit, DIAG function works at least for three pulses.
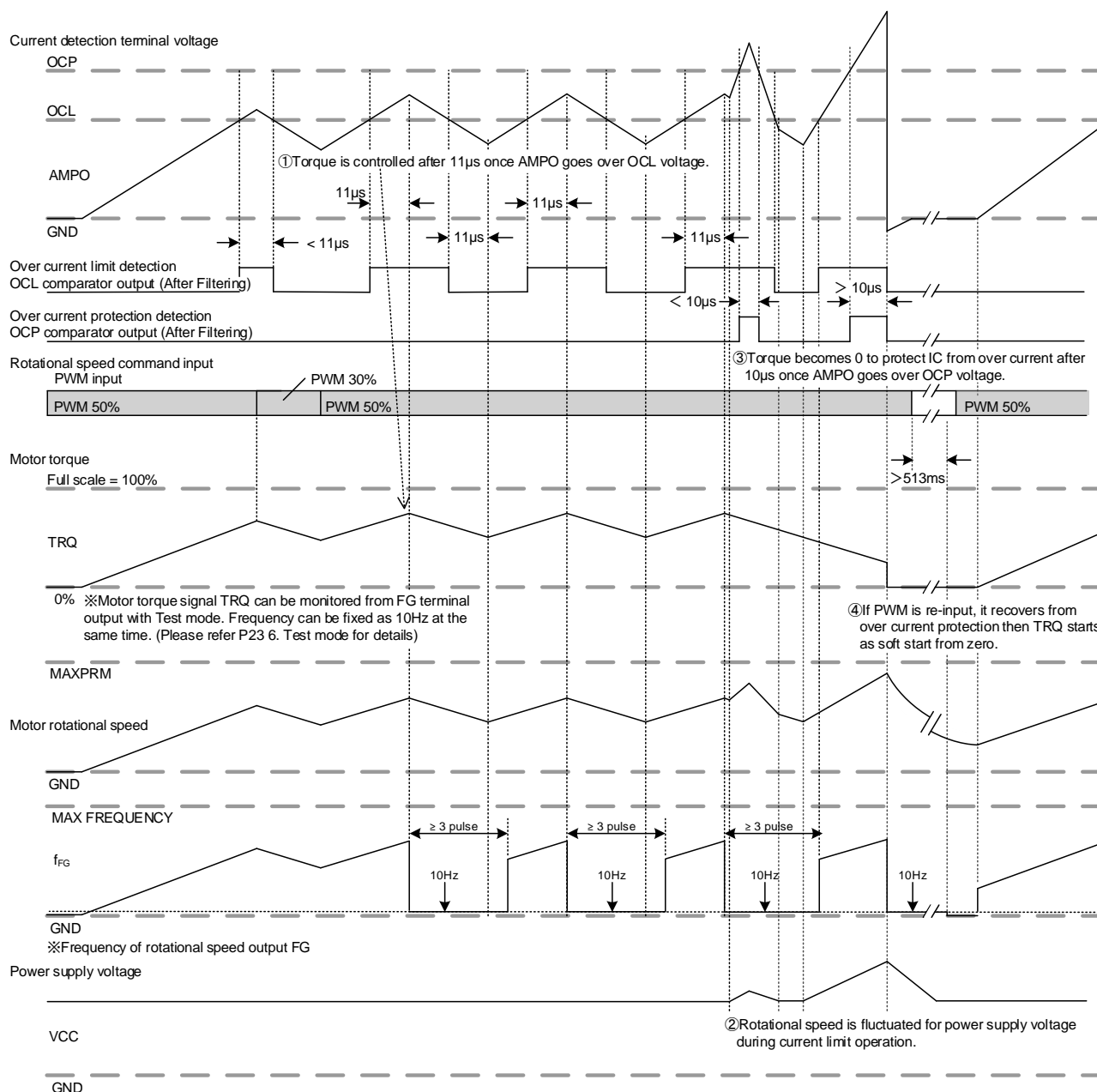

Figure 28. Over Current Limit Circuit Operation

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Description of Operation – continued

(22) Lock Protection

All the output stages of the pre-driver are set as Low and latched in that state when it is detected that the motor has been locked for a certain time. Select standby mode one time in order to deactivate lock protection.

The lock detection time t_{LOCK} can be set from 1.68 s to 15.05 s by applying voltage divided resistance from VREG on LCSET pin.
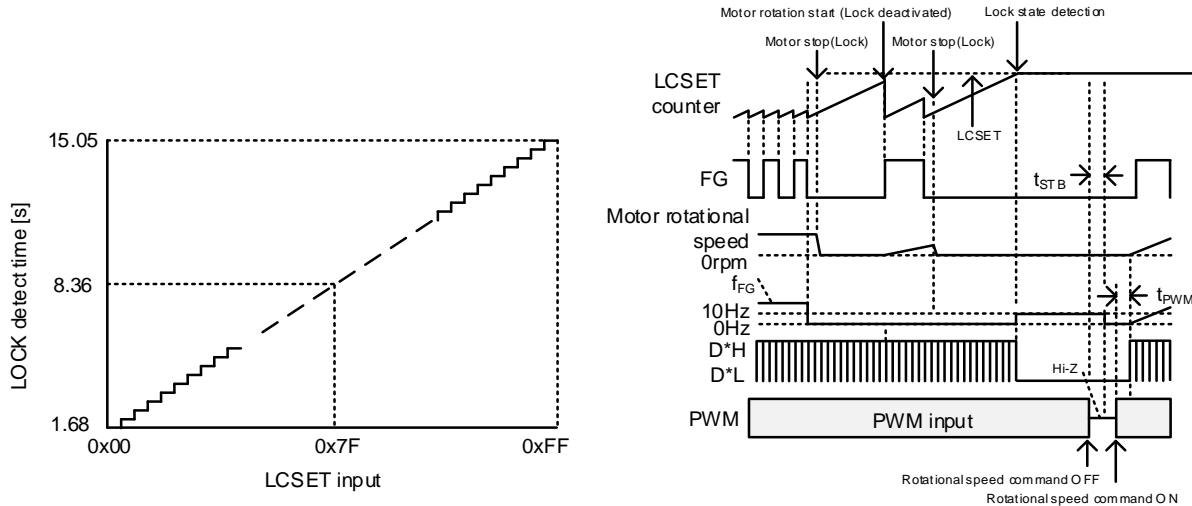
(a) Lock Protection Time vs LCSET   (b) Detection of the Lock Protection and Return Operation

Figure 29. Lock Protection Operation

(23) Under Voltage Lockout

The under voltage lockout circuit is provided to prevent malfunction of IC if VCC pin voltage goes less than the minimum power supply voltage for the driver IC operation. If the power supply voltage is lower than the setup voltage (5.5 V Typ), all the output stages of the pre-driver become Low.

If the power voltage increases (6.0 V Typ), the protection is deactivated and it goes back to the normal operation with TRQ Duty according to the motor rotation state.

Please note that under voltage lockout is not operated if VCC goes less than 4.5 V (Min).
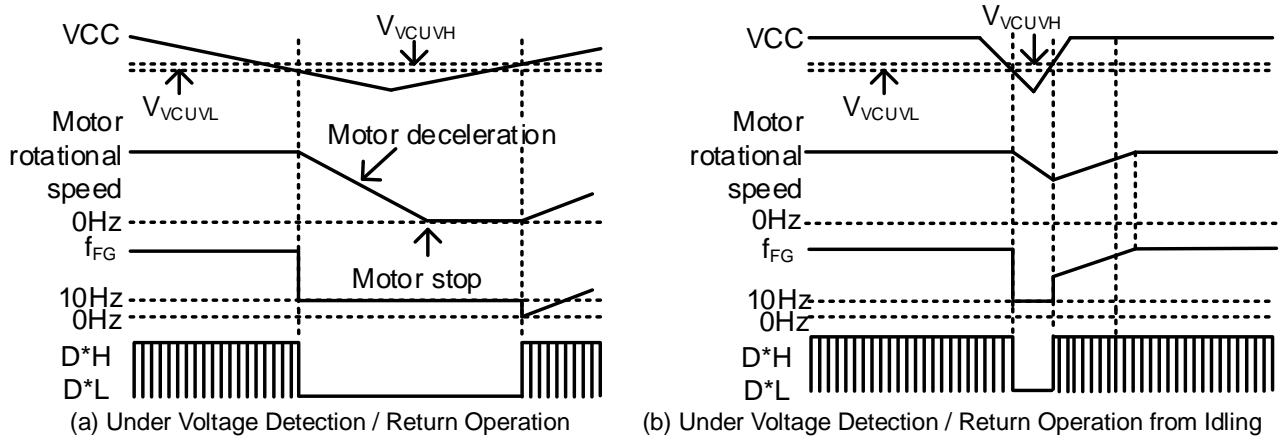
(a) Under Voltage Detection / Return Operation   (b) Under Voltage Detection / Return Operation from Idling

Figure 30. Under Voltage Lockout Operation

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Description of Operation – continued

(24) Over Voltage Protection

If the VCC power-supply voltage is increased and exceeds the specified voltage for VCC over voltage detection (20 V Typ), the over voltage protection circuit is activated. At this time, the output stages of the pre-driver become High side to Low and Low side to High. If the VCC power supply voltage is reduced and lower than the specified voltage to deactivate the VCC over voltage protection (19 V Typ), and back to the normal operation by TRQ Duty according to the state of motor rotation.

This function is only available when the active mode is turned on as the operating condition; it is not activated when it is in the standby mode since current supply to the IC is stopped.

The over voltage protection is built in but make sure that the power-supply voltage should not to exceed the absolute maximum rating as it may be destroyed.

(a) Over Voltage Detection / Return Operation from a Stop (b) Over Voltage Detection / Return Operation from All Over the Turn
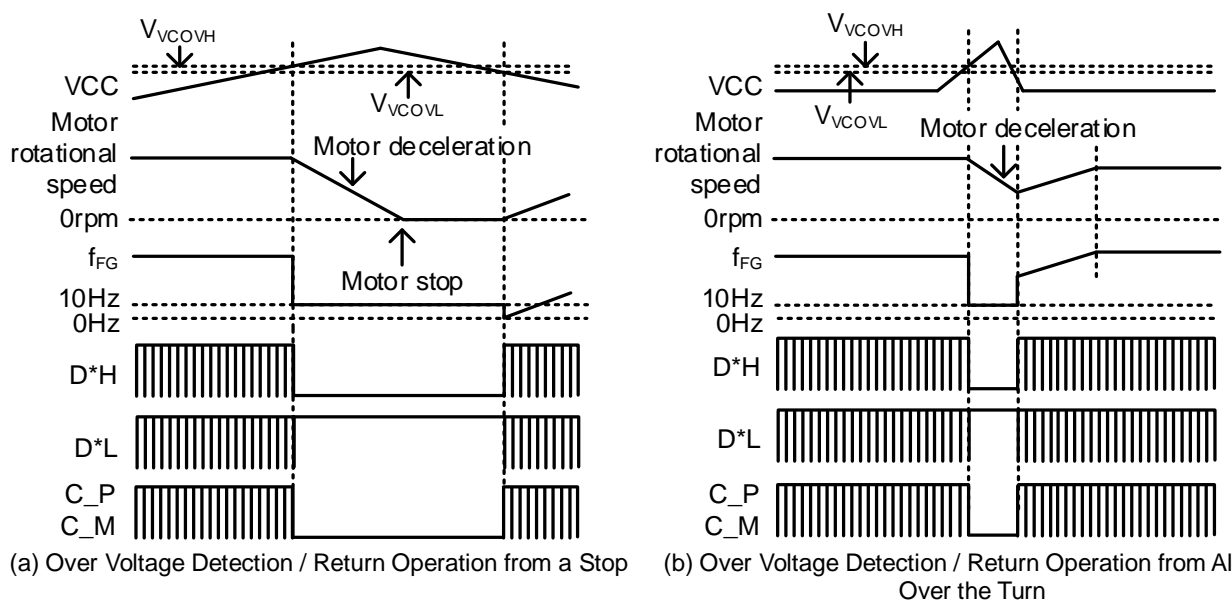
Figure 31. Over Voltage Protection Operation

(25) Thermal Shutdown

If the junction temperature of the driver IC increases and exceeds the specified temperature (175 °C Typ), the thermal shutdown circuit is activated.

At this time, all the output stages of the pre-driver and the charge pump become Hi-Z. If the junction temperature decreases (150 °C Typ), the protection is deactivated for the normal operation by TRQ Duty according to the state of motor rotation.

The thermal shutdown circuit is to shut down the driver IC from thermal runway. The operation guaranteed temperature is exceeded at the time of activation of this circuit. Make sure to consider a thermal design with a sufficient margin so that it should not be used continuously after the activation of this circuit or designed on the assumption of the activation of this circuit.

The above setting temperature is the guaranteed designed values and no measurement with increasing temperature was done.

(a) Thermal Shutdown Detection / Return Operation from a Stop. (b) Thermal Shutdown Detection / Return Operation from All Over the Turn
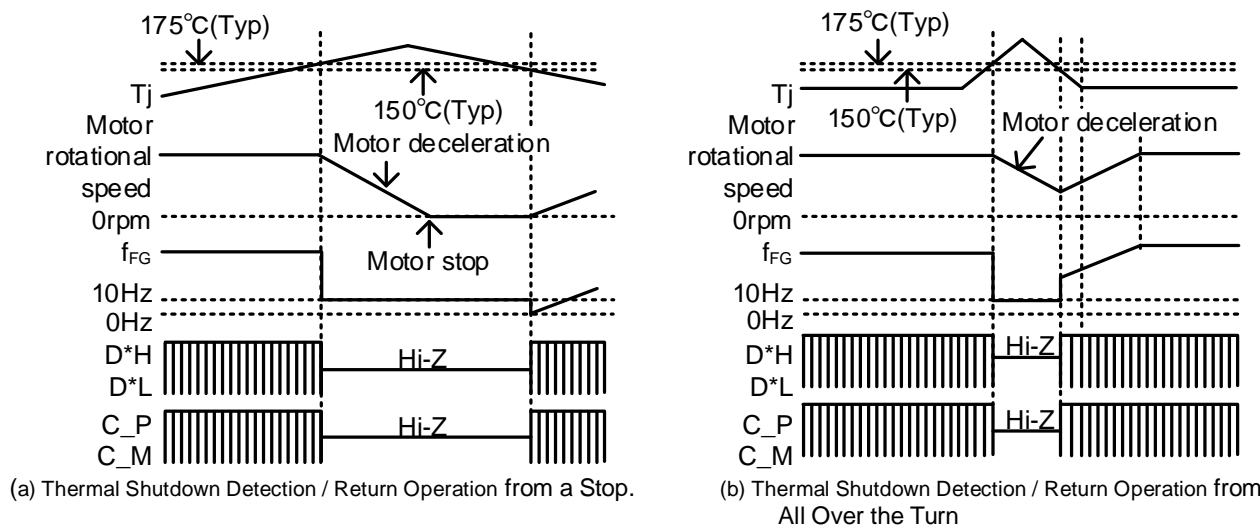
Figure 32. Thermal Shutdown Operation

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Description of Operation – continued

(26) External Parts Thermal Shutdown

To detect temperature increase in an external part and turn off output of the driver IC can be configured in the circuit. The thermistor is set adjacent to a part that requires temperature protection. If the voltage generated in the thermistor falls below the internal reference voltage VTHON (2.5 V Typ), all output stages of the pre-driver become Low. If the protection is deactivated, the operation starts in TRQ Duty according to the motor rotational state.
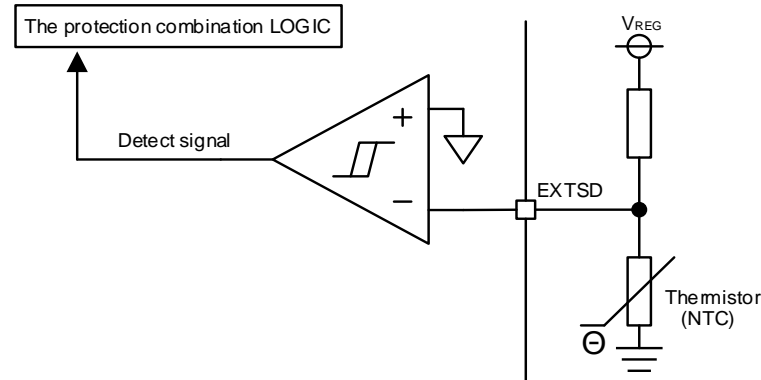
Figure 33. External Parts Temperature Detection Circuit Diagram

(a) External Parts Temperature Detection / Recovery Operation from a Stop

(b) External Parts Temperature Detection / Recovery Operation from All Over the Turn
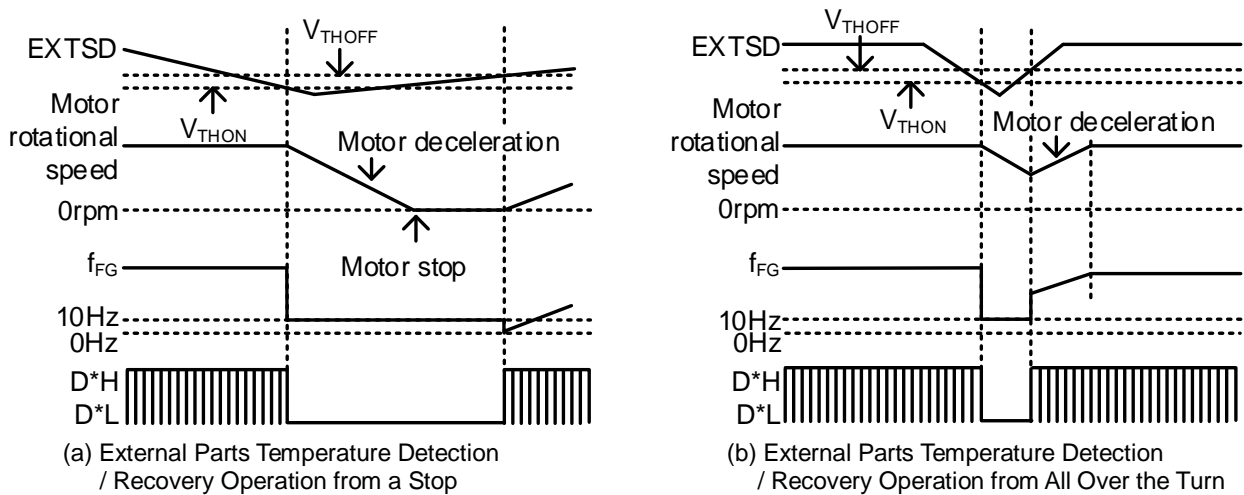
Figure 34. External Parts Thermal Shutdown Operation

(27) Abnormal Detection of Hall Input

If any abnormality occurs in a hall element or a circuit around hall element and single phase of hall input signal does not switch, the hall signal logic detects the state there is no input with the normal sequence. (See Figure 49, Figure 50) Then if the hall input of other phase switches 7 times, it is judged as abnormal hall input signal and all output stages of pre-driver go to Low. Please switch to standby mode one time in order to deactivate the protection state after any abnormality of hall input is detected. If 2 or 3 phase hall input does not switch, the motor is locked and the lock protection is operated. If 3-phase hall input is fixed as Low or High, the driver output becomes Low until the hall input signal switches to normal.
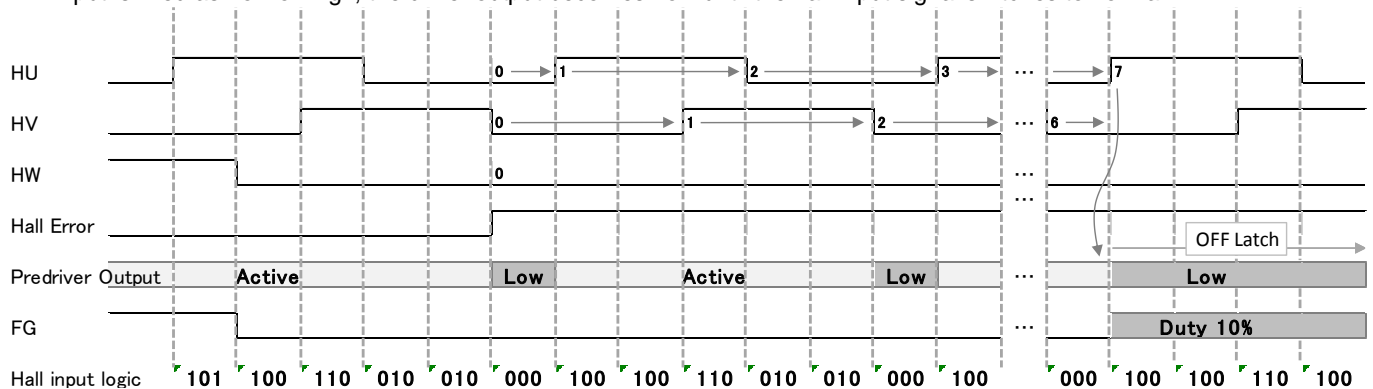
Figure 35. Abnormal Detection Operation of Hall Input

Description of Operation – continued

6. Test Mode
(28) The TEST Pin
The TEST1, TEST2, TEST3 and TEST4 pins are for shipping inspection. Short TEST1 to TEST3 with GND. And short TEST4 with VREG.
Set TEST1 = TEST3 = GND, TEST2 = TEST4 = VREG as the test mode so that the torque can be monitored with Duty of FG.
For the torque, High Duty of the DUH output is output as High Duty of the FG output.
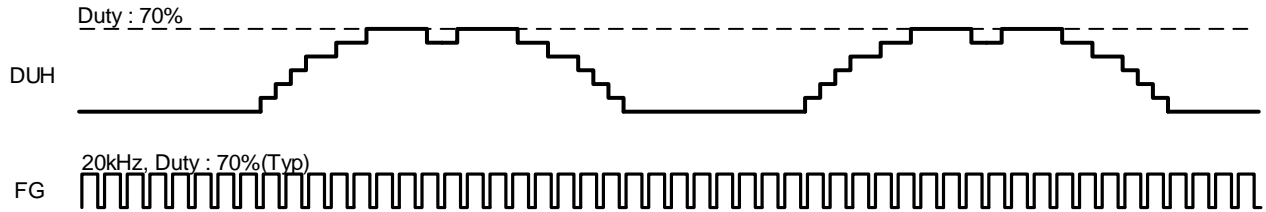
Figure 36. TRQ Duty Monitor

7. Supplemental Characteristic
(29) Boosting Voltage Characteristic
Booster circuit is built in to drive High side N chanel MOS-FET.
Boosting voltage characteristic changes according to conditions of load, voltage, temperature and element variation.
Figure 37 is characteristic of voltage and temperature without connecting load.
Considering loading conditions [Note 1] and element variation, Boosting volatge VG is:

$V_G = 2 \times V_{CC} - 2.218\ V$ [Note 2]

(Note 1) It is the measuring value when connecting with 10000 pF capacitor to output as an external MOS-FET gate capacitance
(Note 2) It is the measuring value for V_{CC} = 6.5 V to 11.5 V. Please use it as a reference.
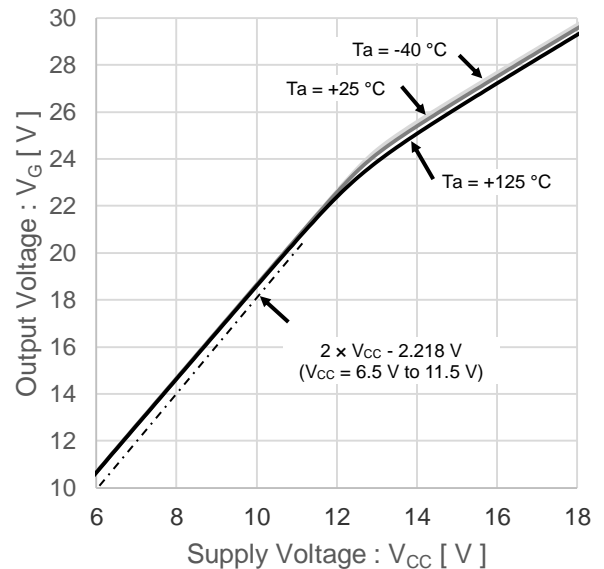
Figure 37. Output Voltage vs Supply Voltage
Boosting Voltage Temperature, Voltage Characteristic

Absolute Maximum Ratings (Ta = 25°C)

Parameter		Symbol	Rating	Unit
Supply Voltage	VCC, VG	V_{CC}, V_G	50	V
Input Voltage [(Note 1)]	PWM, DCIN	V_{PWM}, V_{DCIN}	V_{SREG}	V
	TDEAD, FR, MODESEL, LCSET, PCI, PCG, SSU, SSD, RREF, INTG, PROP, TEST1, TEST2, TEST3, TEST4	V_{TDEAD}, V_{FR}, $V_{MODESEL}$, V_{LCSET}, V_{PCI}, V_{PCG}, V_{SSU}, V_{SSD}, V_{RREF}, V_{INTG}, V_{PROP}, V_{TEST1}, V_{TEST2}, V_{TEST3}, V_{TEST4}	V_{REG}	V
	RNF1, RNF2, OCP, OCL, EXTSD, XIN	V_{RNF1}, V_{RNF2}, V_{OCP}, V_{OCL}, V_{EXTSD}, V_{XIN}		
	HU+, HU-, HV+, HV-, HW+, HW-	V_{HU+}, V_{HU-}, V_{HV+}, V_{HV-}, V_{HW+}, V_{HW-}		
Output Voltage	VREG	V_{REG}	6	V
	SREG	V_{SREG}	6	V
	AMPO, FG, XOUT	V_{AMPO}, V_{FG}, V_{XOUT}	V_{REG}	V
	DUH, DVH, DWH	V_{DUH}, V_{DVH}, V_{DWH}	50	V
	VS_U, VS_V, VS_W, C_P	V_{VSU}, V_{VSV}, V_{VSW}, V_{CP}		
	DUL, DVL, DWL, C_M	V_{DUL}, V_{DVL}, V_{DWL}, V_{CM}	15	V
Current Capability [(Note 2)]	VREG	I_{VREG}	-40	mA
	SREG	I_{SREG}	-10	mA
	FG	I_{FG}	±500	µA
Storage Temperature Range		Tstg	-55 to +150	°C
Maximum Junction Temperature		Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Pull it up in VREG etc., configure an external circuit so that it does not surpass VREG voltage.

(Note 2) For the current item, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

Recommended Operating Conditions

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	6.5	12	18	V
Operating Temperature	Topr	-40	+25	+125	°C

Thermal Resistance[(Note 2)]

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s[(Note 4)]	2s2p[(Note 5)]	
HTQFP64AV				
Junction to Ambient	θ_{JA}	69.8	23.6	°C/W
Junction to Top Characterization Parameter[(Note 3)]	Ψ_{JT}	11	10	°C/W

(Note 2) Based on JESD51-2A(Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via[(Note 6)]	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connects with the copper pattern of all layers.

Electrical Characteristics 1 (Unless otherwise specified V_{CC} = 6.5 V to 18 V, Tj = -40 °C to +125 °C, 0.1 µF between C_P to C_M, 0.1 µF between VG to VCC, VS_U/VS_V/VS_W=GND, f_{XIN}=10 MHz)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[General]						
Circuit Current 1	I_{CC1}	-	26	55	µA	V_{PWM} = V_{SREG}, V_{DCIN} = 0 V
Circuit Current 2	I_{CC2}	-	18	35	mA	V_{DCIN} = 2.5 V
VREG Voltage	V_{REG}	4.8	5.0	5.2	V	I_{VREG} = -40 mA
SREG Voltage	V_{SREG}	3.6	4.75	5.6	V	I_{VSREG} = -10 mA
Boosted Voltage 1	V_{G1}	$2 \times V_{CC}$-2.0	$2 \times V_{CC}$-1.0	$2 \times V_{CC}$	V	V_{CC} = 6.5 V to 11.5 V, f_{PWM} = 625 Hz (Duty = 1 %)
Boosted Voltage 2	V_{G2}	V_{CC}+9	V_{CC}+11.5	V_{CC}+13	V	V_{CC} = 11.5 V to 18 V f_{PWM} = 625 Hz (Duty = 1 %)
Boosted Voltage Load Fluctuation	V_{G3}	-	0.8	1.3	V	I_{VG} = -5 mA, VCC = 6.5 V to 11.5 V, f_{PWM} = 625 Hz (Duty = 1 %)
Boosted Voltage Load Fluctuation	V_{G4}	-	0.6	1.0	V	I_{VG} = -5 mA, VCC = 11.5 V to 18 V, f_{PWM} = 625 Hz (Duty = 1 %)
Switching Frequency for Voltage Boost	f_{CP}	250	312.5	375	kHz	
[ADC]						
ADC Updating Cycle	t_{ADC}	9	10	11	ms	Update V_{DCIN}, V_{PCI}, V_{PCG}, V_{SSU}, V_{SSD}, V_{INTG}, V_{PROP}, V_{RREF}, V_{LCSET} with the cycle t_{ADC}
[Hall Input]						
Input Bias Current	I_{HALL}	-10	0	+10	µA	
Input Amplitude Voltage	$V_{HALLMIN}$	35	-	-	mVpp	
Common-mode Input Voltage Range	V_{HALLCM}	0	-	V_{REG}-1.2	V	
[Rotation Speed Instruction][(Note 1)]						
Minimum Rotation Speed Instruction ON Duty 1	D_{MINON1}	8	10	12	%	$V_{MODESEL}$ = Low
Minimum Rotation Speed Instruction OFF Duty 1	$D_{MINOFF1}$	3	5	7	%	$V_{MODESEL}$ = Low
Hysteresis 1	D_{HYS1}	3	5	7	%	$V_{MODESEL}$ = Low
Maximum Rotation Speed Instruction OFF Duty 2	$D_{MAXOFF2}$	93	95	97	%	$V_{MODESEL}$ = Low
Maximum Rotation Speed Instruction ON Duty 2	D_{MAXON2}	88	90	92	%	$V_{MODESEL}$ = Low
Hysteresis 2	D_{HYS2}	3	5	7	%	$V_{MODESEL}$ = Low
Minimum Rotation Speed Instruction ON Duty 3	D_{MINON3}	8	10	12	%	$V_{MODESEL}$ = High
Minimum Rotation Speed Instruction OFF Duty 3	$D_{MINOFF3}$	3	5	7	%	$V_{MODESEL}$ = High
Hysteresis 3	D_{HYS3}	3	5	7	%	$V_{MODESEL}$ = High
[Output Dead Time][(Note 2)]						
Dead Time 1	t_{DT1}	0.55	1.0	1.45	µs	V_{TDEAD} = Low
Dead Time 2	t_{DT2}	0.05	0.5	0.95	µs	V_{TDEAD} = High

For the current item, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

(Note 1) If a rotational speed command in DCIN is input, a ratio against the VREG voltage is shown.
(Note 2) Pull down DUH and DUL at 10 kΩ to specify the time that the output changes from 10 % to 90 % or from 90 % to 10 %.
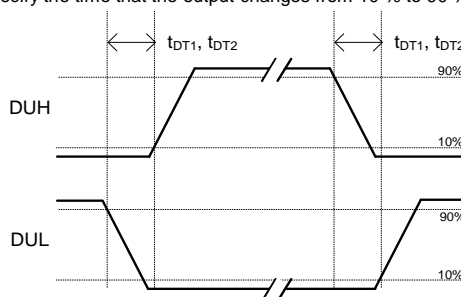

Figure 38. Dead Time Limit

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Electrical Characteristics 2 (Unless otherwise specified V_{CC} = 6.5 V to 18 V, Tj = -40 °C to +125 °C, 0.1 µF between C_P to C_M, 0.1 µF between VG to VCC, VS_U/VS_V/VS_W=GND, f_{XIN}=10 MHz)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Mode Change : FR, MODESEL, TDEAD]						
H Level Input Voltage	V_{INH}	V_{REG}×0.6	-	V_{REG}	V	
L Level Input Voltage	V_{INL}	0	-	V_{REG}×0.2	V	
Hysteresis Voltage	V_{INHYS}	-	V_{REG}×0.11	-	V	
H Level Input Current	I_{INH}	25	50	100	µA	V_{IN} = 5 V
L Level Input Current	I_{INL}	-10	0	+10	µA	V_{IN} = 0 V
[The PWM Pin]						
H Level Input Voltage	V_{PWMH}	V_{SREG}×0.8	-	V_{SREG}	V	
L Level Input Voltage	V_{PWML}	0	-	V_{SREG}×0.4	V	
Hysteresis Voltage	V_{PWMHYS}	-	V_{SREG}×0.11	-	V	
L Level Input Current	I_{PWML}	-100	-50	-	µA	V_{PWM} = 0 V
H Level Input Current	I_{PWMH}	-20	0	+20	µA	V_{PWM} = V_{SREG}
Pin Open Detect Time	t_{STB}	-	513	530	ms	V_{PWM} = 0 V→open, R_{SREG} = 10 kΩ
Pin Open Release Time	t_{PWM}	-	-	53	ms	V_{PWM} = open→0 V, R_{SREG} = 10 kΩ
Input Switching Time	t_{CHGIN}	-	-	53	ms	V_{DCIN} = V_{REG}, V_{PWM} = open→0 V, R_{SREG} = 10 kΩ
[The DCIN Pin]						
Input Voltage Setup Range	$V_{DCRANGE}$	0.25	-	V_{REG}×0.95	V	
H Level Input Current	I_{DCINH}	-	50	100	µA	
L Level Input Current	I_{DCINL}	-20	0	+20	µA	
DCIN STBY Release Voltage	V_{STBOFF}	0.15	0.30	0.45	V	V_{PWM} = High
DCIN STBY Detect Voltage	V_{STBON}	0.05	0.15	0.25	V	V_{PWM} = High
DCIN STBY Hysteresis Voltage	V_{STBHYS}	0.05	0.15	0.25	V	V_{STBOFF} - V_{STBON}
[The FG Pin]						
H Level Output Voltage	V_{FGH}	4.0	-	-	V	I_{FG} = -500 µA
L Level Output Voltage	V_{FGL}	-	-	0.3	V	I_{FG} = 500 µA
H Output Leak Current	I_{LKFGH}	-10	-	-	µA	V_{FG} = 0 V
L Output Leak Current	I_{LKFGL}	-	-	10	µA	V_{FG} = 5 V
[Reference Clock Input Pin XOUT]						
XOUT H Voltage	V_{XOH}	V_{REG} -1.0	V_{REG} -0.2	V_{REG}	V	V_{XIN} = 0 V, I_{XOUT} = -2 mA
XOUT L Voltage	V_{XOL}	0	0.3	0.5	V	V_{XIN} = 5 V, I_{XOUT} = 2 mA

For the current item, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

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Electrical Characteristics 3 (Unless otherwise specified V_{CC} = 6.5 V to 18 V, Tj = -40 °C to +125 °C, 0.1 μF between C_P to C_M, 0.1 μF between VG to VCC, VS_U/VS_V/VS_W=GND, f_{XIN}=10 MHz)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Maximum rotation Speed Setup]						
Maximum Rotation Speed Setup Tolerance	f_{MAXRPM}	257	264	271	Hz	R_{RREFH} = 27 kΩ, R_{RREFL} = 160 kΩ *(Note 1)*
[The SSU,SSD Pin]						
Rotation Speed Instruction Rise Time*(Note 2)*	t_{SSU}	-	0.492	-	ms	V_{SSU} = GND, V_{RREF} = V_{REG}
Rotation Speed Instruction Rise Time*(Note 2)*	t_{SSD}	-	0.164	-	ms	V_{SSD} = GND, V_{RREF} = V_{REG}
[Phase Control]						
Lead Angle Gain Setup*(Note 3)*	G_{PCG}	14	15	16	°	V_{PCG} = VREG/4, V_{PCI} = GND, f_{PWM} = 625 Hz (Duty = 50 %), TRQ duty = 50 %
Lead Angle Initial Torque Setup	T_{PCI}	46	50	54	%	V_{PCI} = V_{REG}/2, V_{PCG} = V_{REG}/2
Maximum Lead Angle	P_{MAX}	29	30	31	°	V_{PCG} = V_{REG}, V_{PCI} = V_{PWM} = GND
[Pre-driver Output Pin]*(Note 4)*						
D*H/ D*L Output Oscillating Frequency	f_{OSC}	18	20	22	kHz	f_{XOUT} = 10 MHz
D*H High Voltage1	V_{OUTHH1}	23	-	31	V	V_{CC} = 18 V
D*H Low Voltage1	V_{OUTHL1}	-	0	0.2	V	V_{CC} = 18 V
D*L High Voltage1	V_{OUTLH1}	9	-	13	V	V_{CC} = 18 V
D*L Low Voltage1	V_{OUTLL1}	-	0	0.2	V	V_{CC} = 18 V
D*H High Voltage2	V_{OUTHH2}	10.5	-	13.5	V	V_{CC} = 6.5 V
D*H Low Voltage2	V_{OUTHL2}	-	0	0.2	V	V_{CC} = 6.5 V
D*L High Voltage2	V_{OUTLH2}	4.5	-	7	V	V_{CC} = 6.5 V
D*L Low Voltage2	V_{OUTLL2}	-	0	0.2	V	V_{CC} = 6.5 V
D*H Slew Rate Rising 1	V_{OHUSR1}	10	-	55	V/μs	V_{CC} = 18 V
D*H Slew Rate Falling 1	V_{OHDSR1}	30	-	120	V/μs	V_{CC} = 18 V
D*L Slew Rate Rising 1	V_{OLUSR1}	2	-	40	V/μs	V_{CC} = 18 V
D*L Slew Rate Falling 1	V_{OLDSR1}	8	-	85	V/μs	V_{CC} = 18 V
D*H Slew Rate Rising 2	V_{OHUSR2}	6	-	45	V/μs	V_{CC} = 6.5 V
D*H Slew Rate Falling 2	V_{OHDSR2}	6	-	70	V/μs	V_{CC} = 6.5 V
D*L Slew Rate Rising 2	V_{OLUSR2}	1	-	10	V/μs	V_{CC} = 6.5 V
D*L Slew Rate Falling 2	V_{OLDSR2}	6	-	55	V/μs	V_{CC} = 6.5 V
Diode Voltage Between VS_U / VS_V / VS_W to GND	V_{DI}	-1.35	-0.72	-0.40	V	I_{SINK} = -50 mA

For the current item, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

(Note 1) According to the resistance ratio for the RREF voltage setting, VREG x 0.855 is applied to RREF.
(Note 2) The time required for rotational command to fluctuate 1 % is defined.
       This characteristic does not the shipment inspection.
(Note 3) This characteristic does not the shipment inspection.
(Note 4) Slew rate items are the rated value when a 10000 pF capacitor is connected to output as a gate capacity of an external MOS-FET.

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Electrical Characteristics 4 (Unless otherwise specified V_{CC} = 6.5 V to 18 V, Tj = -40 °C to +125 °C, 0.1 µF between C_P to C_M, 0.1 µF between VG to VCC, VS_U/VS_V/VS_W=GND, f_{XIN}=10 MHz)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Lock Protection]						
Lock Protection Detect Time *(Note 1)*	t_{LOCK}	-	8.36	-	s	V_{LCSET} = V_{REG}/2
[Over Current Detect Amplifier]						
Input Offset Voltage	$V_{AMPOFST}$	-8	0	+8	mV	V_{RNF2} = V_{AMPO}, V_{RNF1} = 200 mV $V_{AMPOFST}$ = V_{AMPO} - V_{RNF1}
Common-mode Input Range	V_{INRNG}	0.2	-	2.5	V	V_{RNF2} = V_{AMPO}, $V_{AMPOFST}$ ≤ |8 mV|
Source Current	I_{AMPSRC}	-	-	-50	µA	V_{RNF2} = V_{AMPO}, V_{RNF1} = 2.5 V V_{AMPO} ≥ 2.0 V
Sink Current	I_{AMPSNK}	50	-	-	µA	V_{RNF2} = V_{AMPO}, V_{RNF1} = 0 V V_{AMPO} ≤ 0.2 V
Output Voltage Range	V_{OUTRNG}	0.2	-	2.5	V	V_{RNF2} = V_{AMPO}, $V_{AMPOFST}$ ≤ |8 mV|
Voltage Gain Range	A_{OC}	31	32	33	dB	R_{RNF1} = R_{RNF2} = 10 kΩ, R_{RNF11} = R_{AMPO} = 400 kΩ
[Over Current Protection]						
OCP Detect Comparator Offset	$V_{OCPOFST}$	-10	-	+10	mV	V_{RNF2} = V_{AMPO}, V_{RNF1} = Sweep, V_{OCP} = 500 mV
OCP Detect Time	t_{OCPON}	-	10	35	µs	
[Over Current Limit]						
OCL Detect Comparator Offset	$V_{OCLOFST}$	-10	-	+10	mV	V_{RNF2} = V_{AMPO}, V_{RNF1} = Sweep, V_{OCL} = 1.0 V
OCL Detect time	t_{OCLON}	-	11	35	µs	
OCL Release Time	t_{OCLOFF}	-	11	35	µs	
[Under Voltage Lockout]						
UVLO Release Voltage	V_{VCUVH}	5.5	6.0	6.5	V	
UVLO Detect Voltage	V_{VCUVL}	5.0	5.5	6.0	V	
UVLO Hysteresis Voltage	$V_{VCUVHYS}$	0.3	0.5	0.7	V	
[Over Voltage Protection]						
OVP Detect Voltage	V_{VCOVH}	17.3	20.0	22.7	V	
OVP Release Voltage	V_{VCOVL}	16.5	19.0	21.5	V	
OVP Hysteresis Voltage	$V_{VCOVHYS}$	0.4	1.0	1.6	V	
[External Parts Thermal Shutdown]						
External Parts Thermal Shutdown Detect Voltage	V_{THON}	V_{REG}×0.47	V_{REG}×0.50	V_{REG}×0.53	V	
External Parts Thermal Shutdown Release Voltage	V_{THOFF}	V_{REG}×0.55	V_{REG}×0.58	V_{REG}×0.61	V	
[DIAG Output Function Using FG Duty]						
DIAG1 (LOCK / HALLERR) FG Duty	D_{DIAG1}	5	10	15	%	Lock Protection, Abnormal Hall Input
DIAG2 (OCP / OCL) FG Duty	D_{DIAG2}	85	90	95	%	Over Current Protection, Over Current Limit
DIAG3 (TSD / EXTSD) FG Duty	D_{DIAG3}	25	30	35	%	Thermal Shutdown, External Parts Thermal Shutdown
DIAG4 (OVP / UVLO) FG Duty	D_{DIAG4}	65	70	75	%	Over Voltage Protection, Under Voltage Lockout

For the current item, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

(Note 1) This characteristic does not the shipment inspection

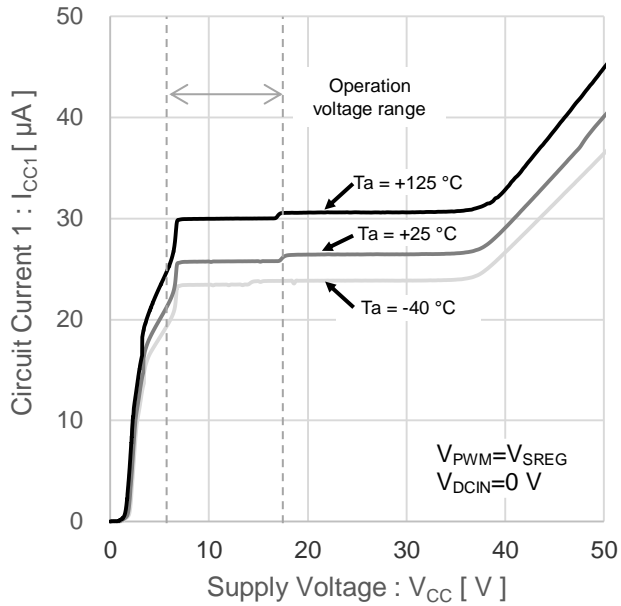## Typical Performance Curves

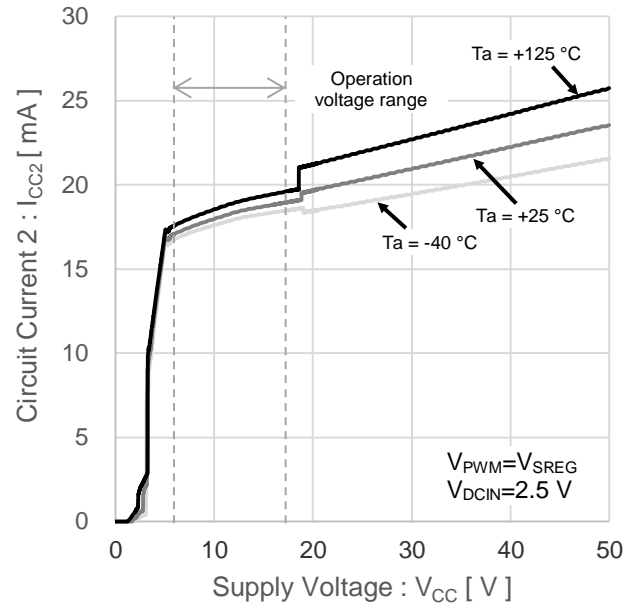Figure 39. Circuit Current 1 vs Supply Voltage

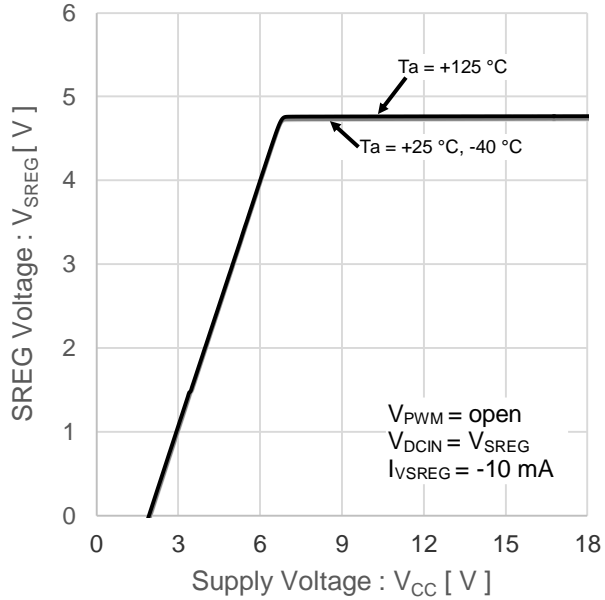Figure 40. Circuit Current 2 vs Supply Voltage

Figure 41. SREG Voltage vs Supply Voltage

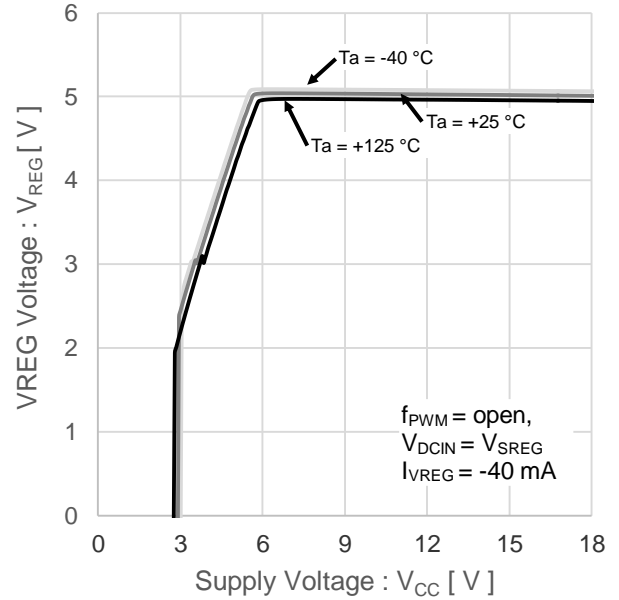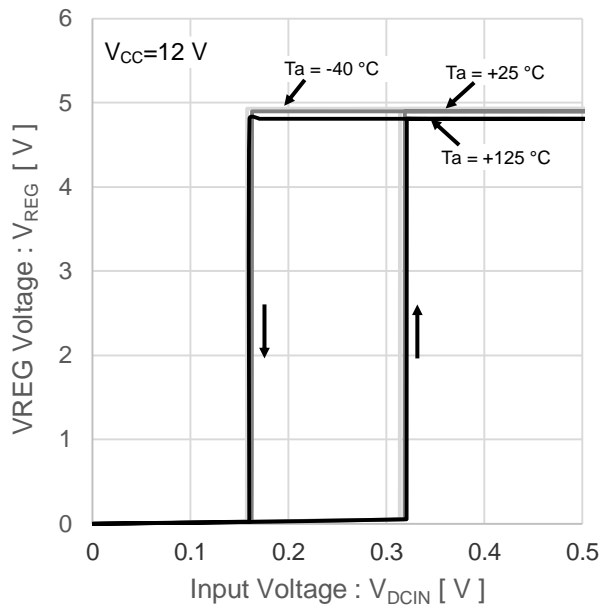Figure 42. VREG Voltage vs Supply Voltage

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Typical Performance Curves – continued

Figure 43. VREG Voltage vs Input Voltage
(The DCIN Pin STBY Detection Release / Detection Voltage)
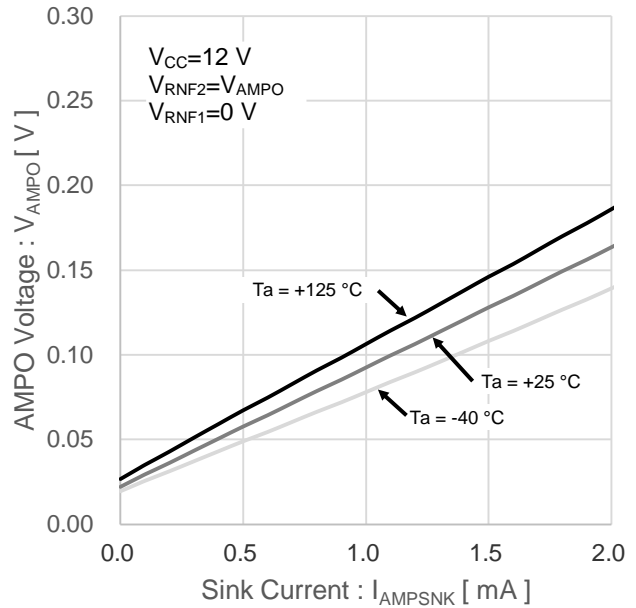

Figure 44. AMPO Voltage vs Sink Current
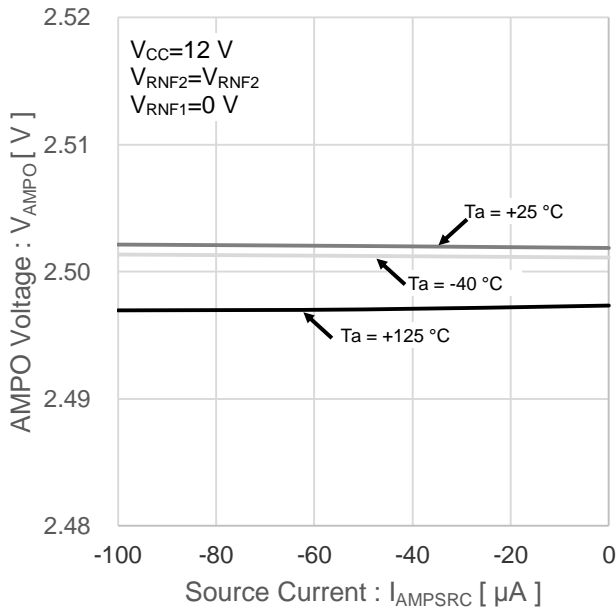(Over Current Detection Amp Sink Capacity)

Figure 45. AMPO Voltage vs Source Current
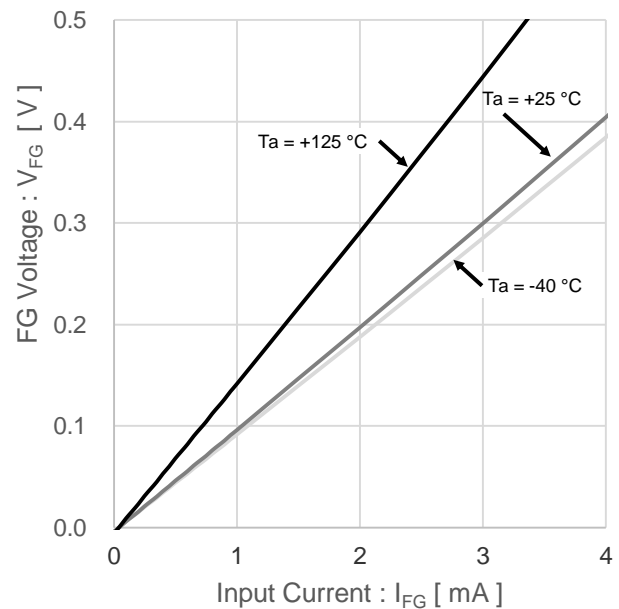(Over Current Detection Amp Source Capacity)

Figure 46. FG Voltage vs Input Current
(The FG Pin L Level Output Voltage)

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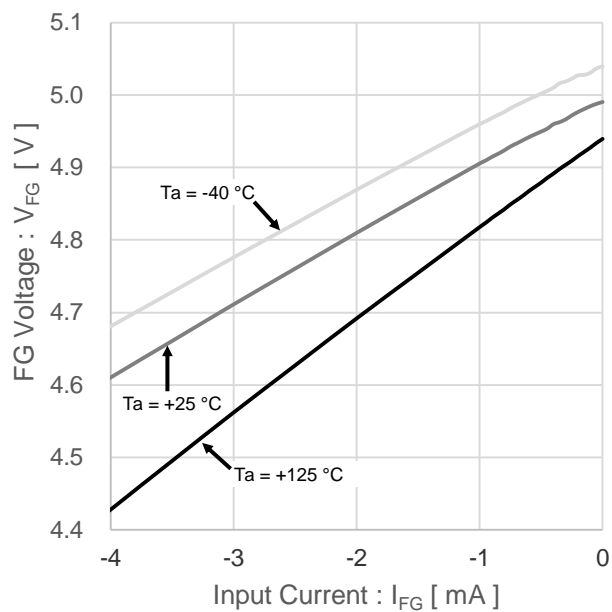
Typical Performance Curves – continued

Figure 47. FG Voltage vs Input Current
(The FG Pin H Level Output Voltage)

Figure 48. VS_U Voltage vs Input Current
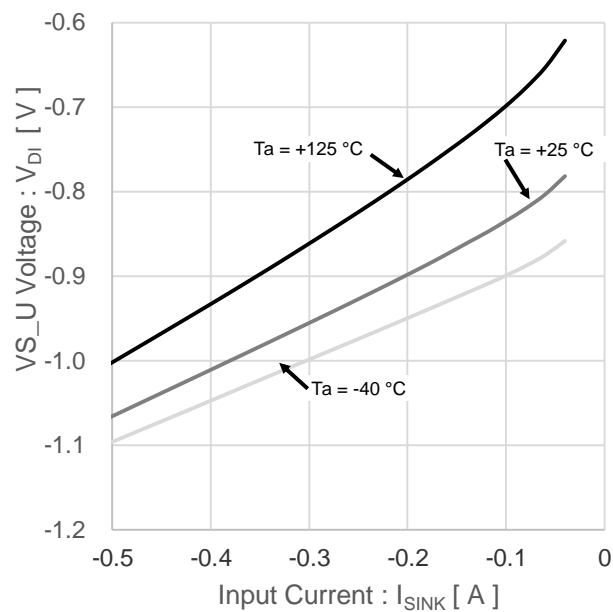(Diode Voltage between VS_U / VS_V / VS_W and GND)

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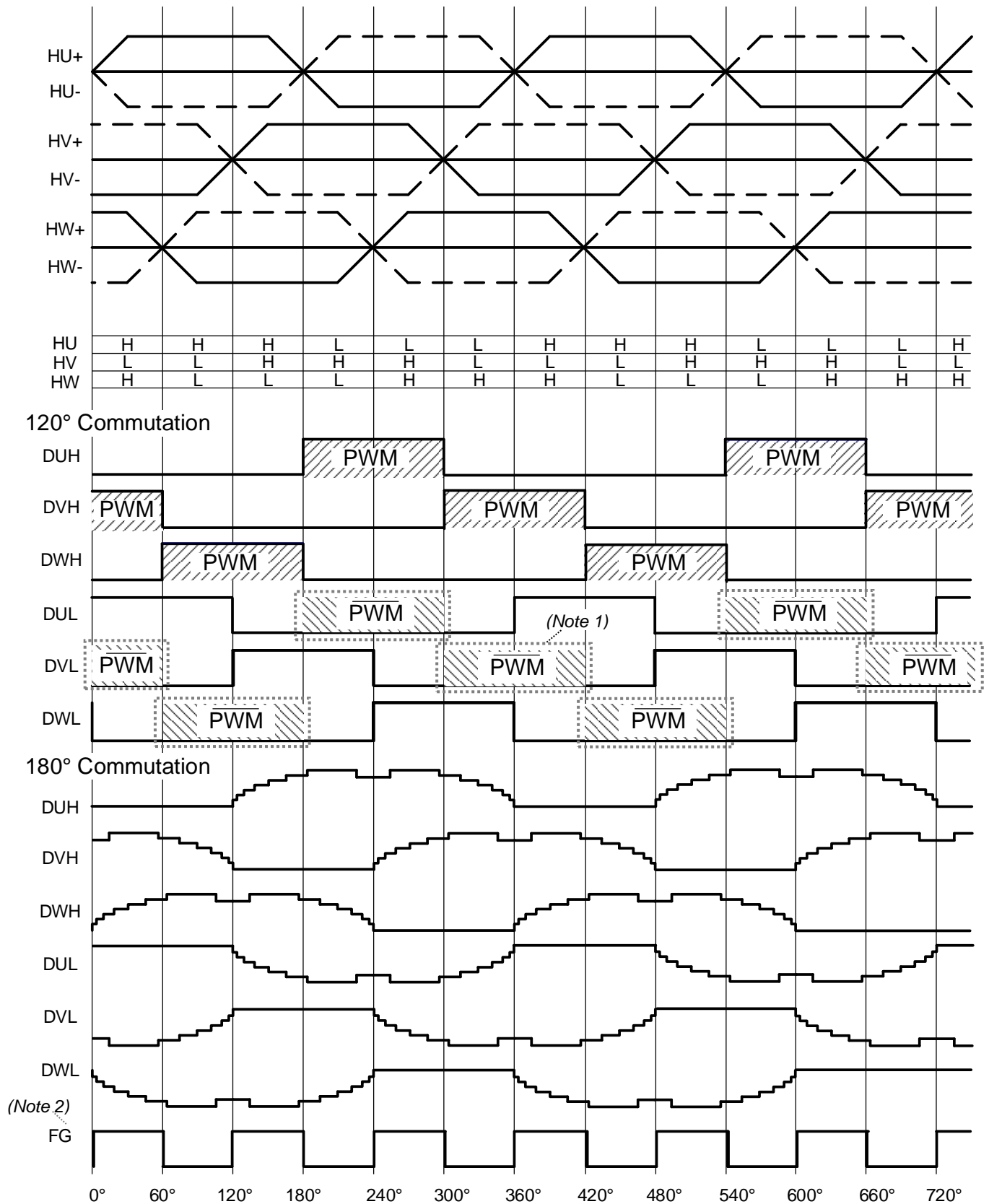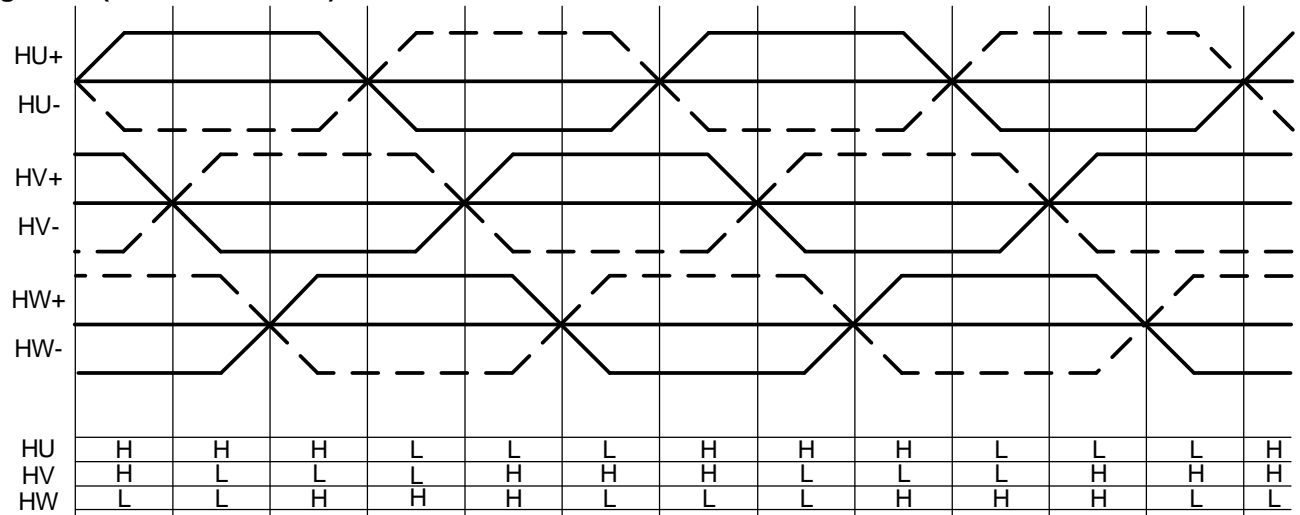
Timing Chart (Forward Rotation)

Figure 49. Timing Chart (FR=H Forward Rotation)

(Note 1) PWM sections: DUL, DVL and DWL surrounded by dotted lines, are fixed as Low and low side arm turns OFF for asynchronous rectification.
(Note 2) FG switching timing is generated from the electrical angle saved in the internal IC and it does not match always with a hall signal of U, V or W-phase.

Timing Chart (Reverse Rotation)

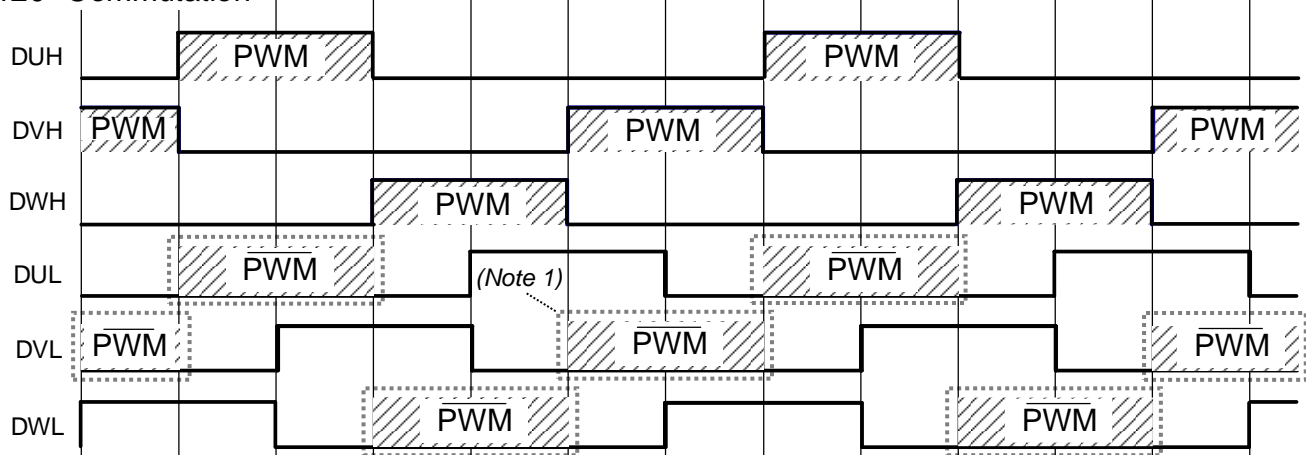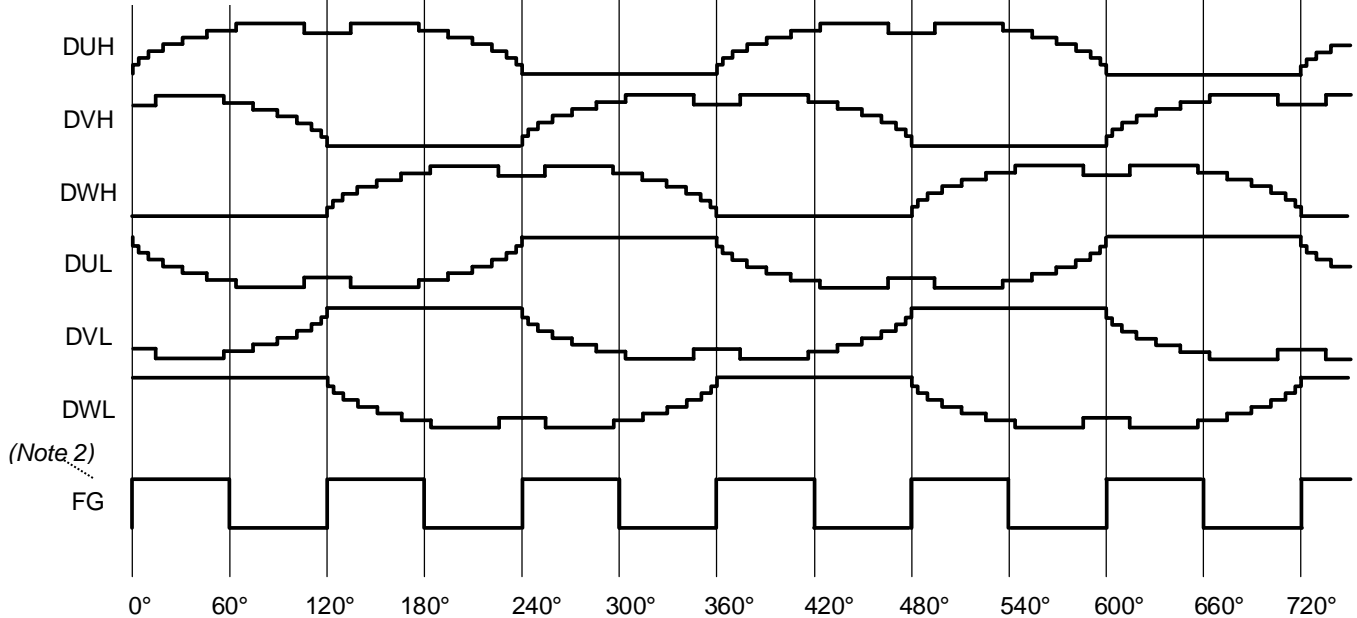Figure 50. Timing Chart (FR=L Reverse Rotation)

(Note 1) PWM sections: DUL, DVL and DWL surrounded by dotted lines, are fixed as Low and low side arm turns OFF for asynchronous rectification.
(Note 2) FG switching timing is generated from the electrical angle saved in the internal IC and it does not match always with a hall signal of U, V or W-phase.

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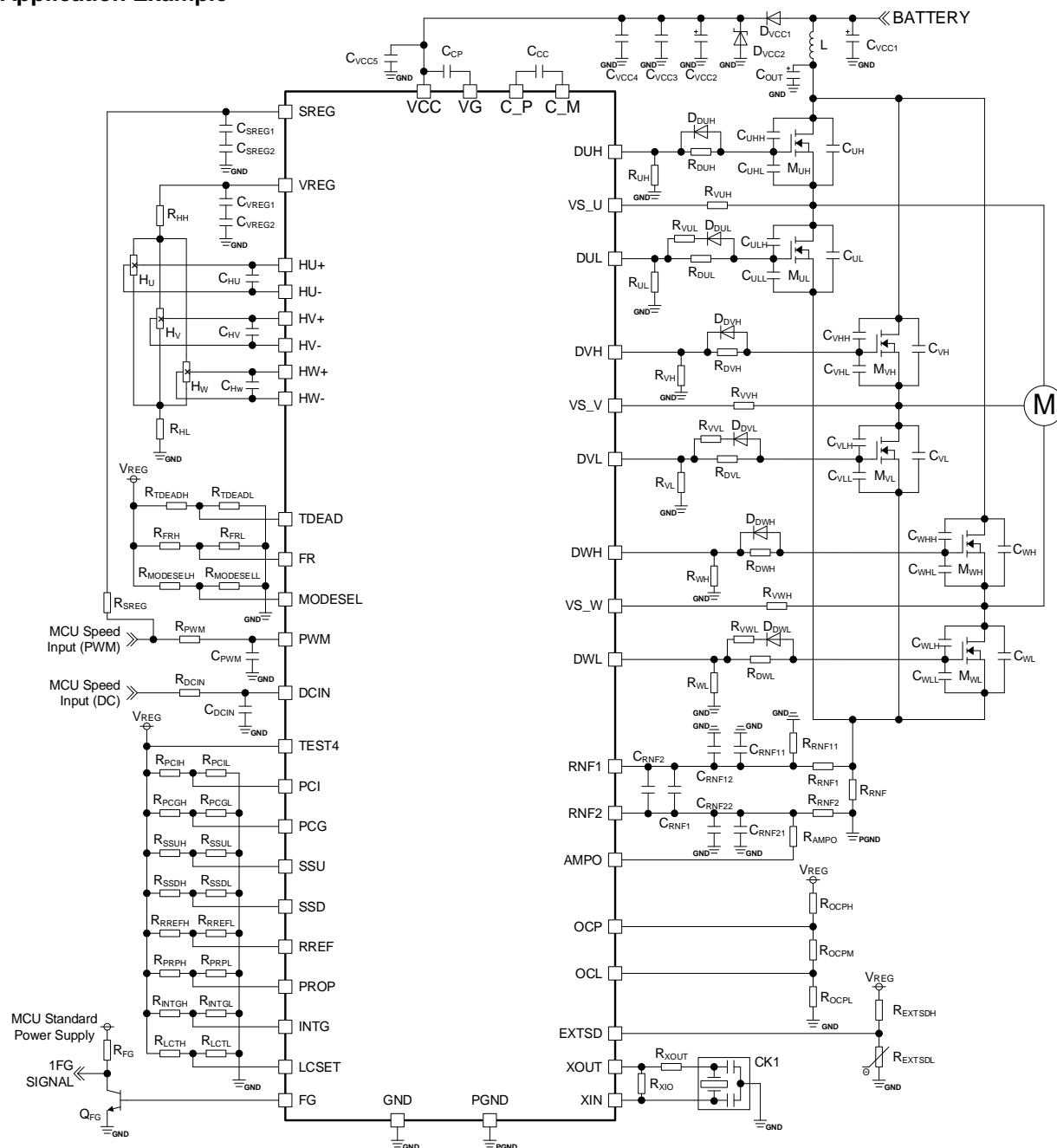
Application Example

Figure 51. Application Example

Recommended Circuit Component

This IC is designed and evaluated based on the assumption that the recommended components listed below are used.
If the application circuit is designed without the following recommended components, make sure to select components after carefully checking in the characteristics.

No.	Component Name	Component Value	Description
1	D_{VCC1}	1.0 A	Rectifier
2	D_{VCC2}	30 V	Zener Diode
3	L	100 μH	Inductor
4	C_{VCC1}	220 μF / 35 V	Electrolytic Capacitor
5	C_{VCC2}	100 μF / 50 V	Electrolytic Capacitor
6	C_{VCC3}	0.1 μF / 50 V	Ceramic Capacitor
7	C_{VCC4}	100 pF / 50 V	Ceramic Capacitor
8	C_{VCC5}	0.1 μF / 50 V	Ceramic Capacitor
9	C_{OUT}	1320 μF / 35 V	Electrolytic Capacitor
10	C_{CC}, C_{CP}	0.1 μF / 50 V	Ceramic Capacitor
11	M_{UH}, M_{UL}, M_{VH}, M_{VL}, M_{WH}, M_{WL}	-	Nch MOSFET
12	C_{UHH}, C_{VHH}, C_{WHH}, C_{ULH}, C_{VLH}, C_{WLH}	100 pF / 50 V	Ceramic Capacitor
13	CUHL, CVHL, CWHL, CULL, CVLL, CWLL	100 pF / 50 V	Ceramic Capacitor

Recommended Circuit Component – continued

No.	Component Name	Component Value	Description
14	C_{UH}, C_{VH}, C_{WH}, C_{UL}, C_{VL}, C_{WL}	1000 pF / 50 V	Ceramic Capacitor
15	R_{VUH}, R_{VUL}, R_{VVH}, R_{VVL}, R_{VWH}, R_{VWL}	51 Ω	Resistor
16	R_{UH}, R_{VH}, R_{WH}	47 kΩ	Resistor
17	R_{UL}, R_{VL}, R_{WL}	10 kΩ	Resistor
18	R_{DUH}, R_{DUL}, R_{DVH}, R_{DVL}, R_{DWH}, R_{DWL}	75 Ω	Resistor
19	D_{DUH}, D_{DUL}, D_{DVH}, D_{DVL}, D_{DWH}, D_{DWL}	-	Diode
20	R_{RNF}	1 mΩ / 5 W	Shunt Resistor
21	R_{RNF1}, R_{RNF2}	2.2 kΩ	Resistor
22	R_{RNF11}	47 kΩ	Resistor
23	R_{AMPO}	47 kΩ	Resistor
24	C_{RNF1}, C_{RNF11}, C_{RNF21}	0.1 µF / 50 V	Ceramic Capacitor
25	C_{RNF2}, C_{RNF12}, C_{RNF22}	100 pF / 50 V	Ceramic Capacitor
26	R_{OCPH}	39 kΩ	Resistor
27	R_{OCPM}	4.7 kΩ	Resistor
28	R_{OCPL}	5.6 kΩ	Resistor
29	R_{EXTSDH}	1.4 kΩ	Resistor
30	R_{EXTSDL}	100 kΩ	NTC Thermistor
31	R_{XOUT}	150 Ω	Resistor
32	R_{XIO}	1 MΩ	Resistor
33	CK1	10.000 MHz	Ceramic Resonator
34	C_{VREG1}, C_{VREG2}	2.2 µF / 5 V	Ceramic Capacitor
35	C_{SREG1}, C_{SREG2}	0.22 µF / 5 V	Ceramic Capacitor
36	R_{HH}	150 Ω	Resistor
37	H_U, H_V, H_W	-	Hall Element
38	C_{HU}, C_{HV}, C_{HW}	0.1 µF / 5 V	Ceramic Capacitor
39	R_{HL}	150 Ω	Resistor
40	R_{SREG}	10 kΩ	Resistor
41	R_{TDEADL}, R_{FRL}, $R_{MODESELL}$	0 Ω	Resistor
42	R_{TDEADH}, R_{FRH}, $R_{MODESELH}$	N.A	Resistor
43	R_{PWM}	47 kΩ	Resistor
44	C_{PWM}	100 pF / 5 V	Ceramic Capacitor
45	R_{DCIN}	47 kΩ	Resistor
46	C_{DCIN}	100 pF / 5 V	Ceramic Capacitor
47	R_{LCTH}, R_{INTGH}, R_{PRPH}, R_{RREFH}, R_{SSDH}, R_{SSUH}, R_{PCGH}, R_{PCIH}	to 500 kΩ	Resistor
48	R_{LCTL}, R_{INTGL}, R_{PRPL}, R_{RREFL}, R_{SSDL}, R_{SSUL}, R_{PCGL}, R_{PCIL}	to 500 kΩ	Resistor
49	R_{FG}	1 kΩ	Resistor
50	Q_{FG}	-	NPN Transistor

Application Designing Notes

1. Absolute Maximum Ratings

An excess in the absolute maximum ratings such as supply voltage and voltage range of operating conditions may damage the IC, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. In cases where the IC is expected to be used in a special mode in which it exceeds the absolute maximum ratings, consider taking physical safety measures such as using a fuse.

2. GND Potential

Depending on the conditions including heat generation condition, power supply voltage and the motor in use, it may cause failures such as malfunction when the potential of the output pin swings to substantially below GND. In that case, take measures to prevent such failures by adding a schottky diodes between the output and GND. Make sure to keep the potential of the GND pin at the minimum potential in any operating conditions.

3. Back Electromotive Force

The back electromotive force may be changed due to the operating condition, environment and characteristic of each motor. Make sure to thoroughly check that the IC operation is not affected by the back electromotive force.
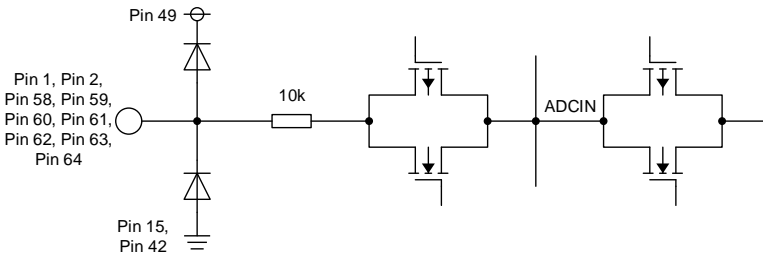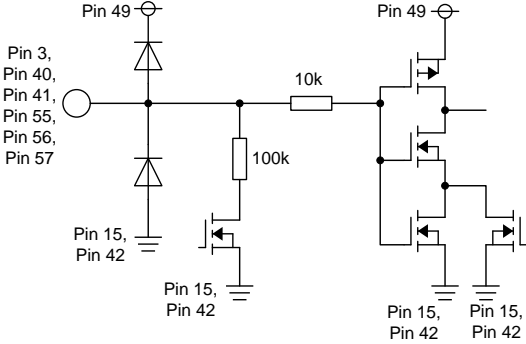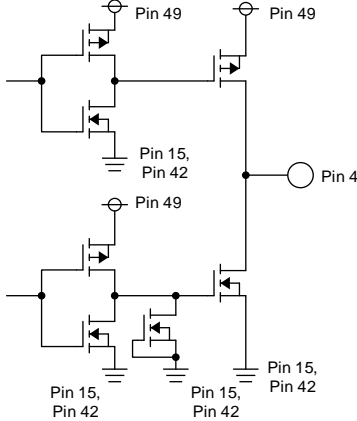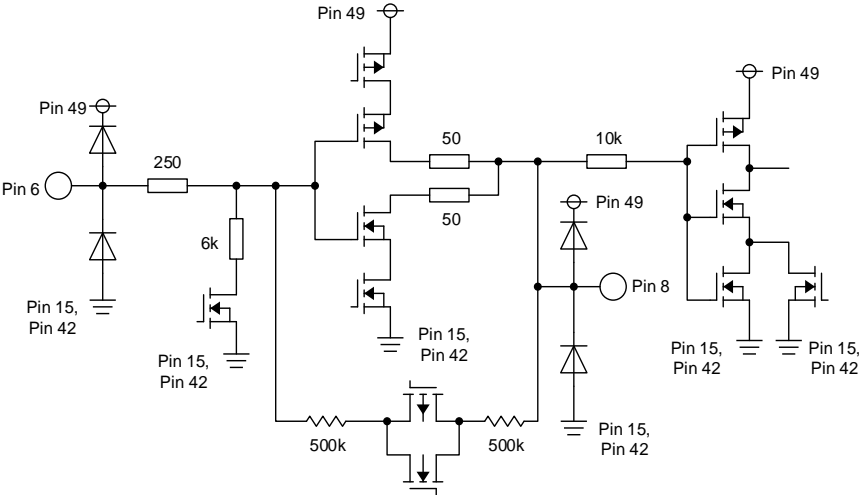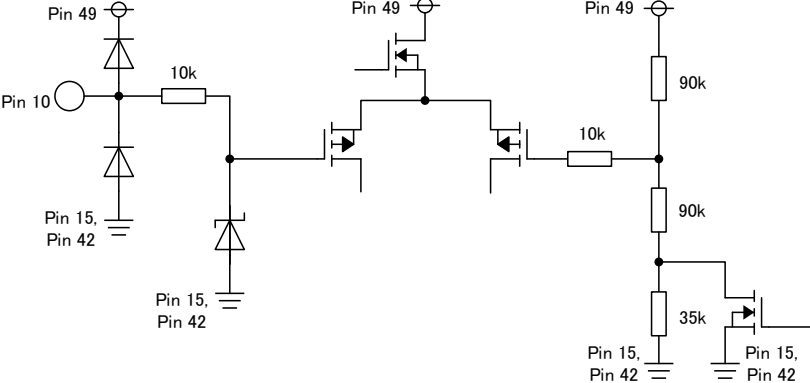
4. GND Wiring

Connection destinations of PGND and GND of each component are shown as recommended connection destinations in Figure 51. Pay sufficient attention when wiring as high current flows into PGND.

5. TDEAD, FR, MODESEL

The TDEAD, FR and MODESEL pins are respectively connected to GND at 0Ω when the recommended circuit components are installed in the circuit shown in Figure 51. When connecting them to the VREG pin, set the resistance value to at least 130 Ω to 10 kΩ.

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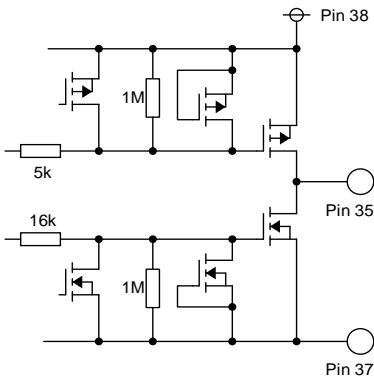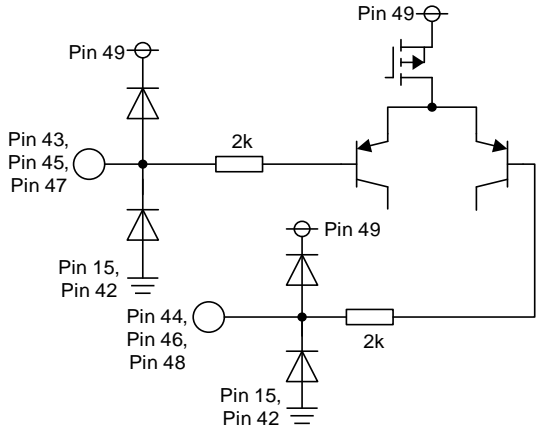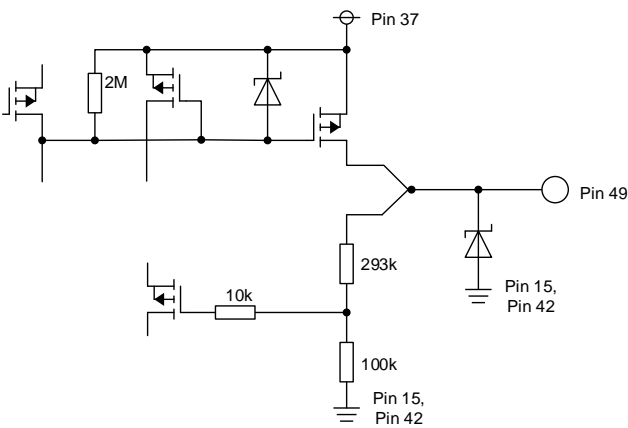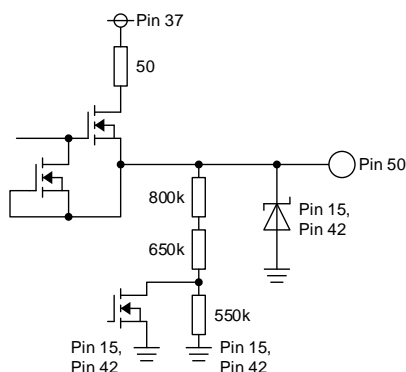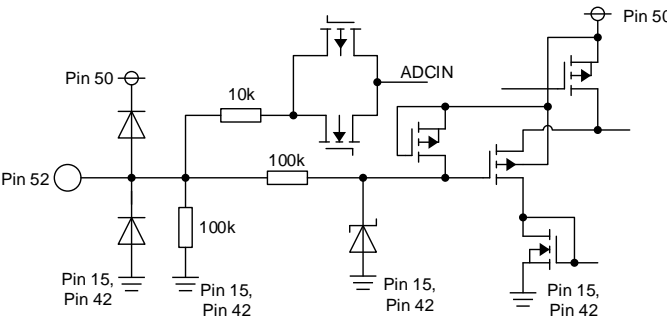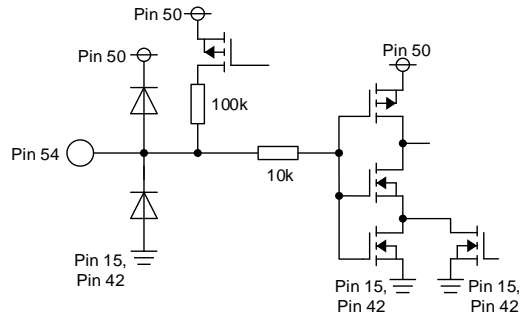
I/O Equivalence Circuit (Typ values for resistance and capacitance)

1.PCI, 2.TEST4, 15.GND, 42.GND, 58.LCSET, 59.SSU, 60.SSD, 61.PROP, 62.INTG, 63.RREF, 64.PCG

3.TEST3, 40.TEST1, 41.TEST2, 55.TDEAD, 56.MODESEL, 57.FR	4.FG

6.XIN, 8.XOUT

10.EXTSD

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I/O Equivalence Circuit – continued

11.OCL,12.OCP	13.AMPO

14.RNF1, 16.RNF2	17.DWL, 22.DVL, 27.DUL, 32.PGND, 37.VCC

19.VS_W, 20.DWH, 24.VS_V, 25.DVH, 29.VS_U, 30.DUH	33.C_M

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I/O Equivalence Circuit – continued

35.C_P, 38.VG	43.HU+, 44.HU-, 45.HV+, 46.HV-, 47.HW+, 48.HW-

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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.
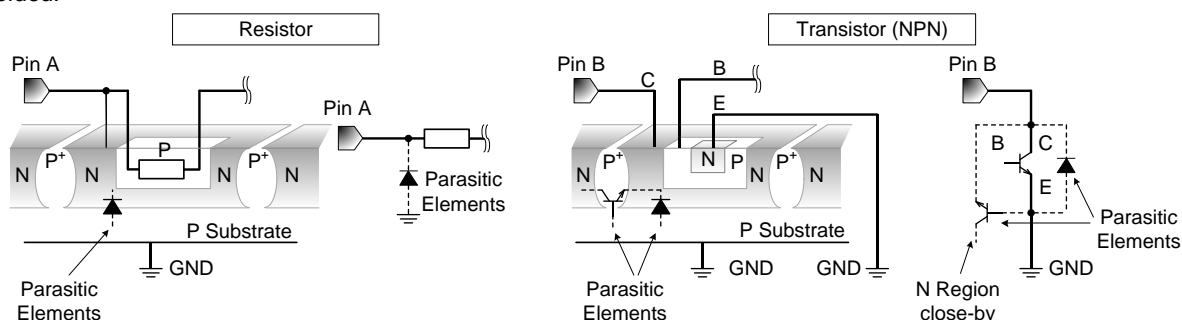

Figure 52. Example of monolithic IC structure

12. **Ceramic Capacitor**
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. **Area of Safe Operation (ASO)**
Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).
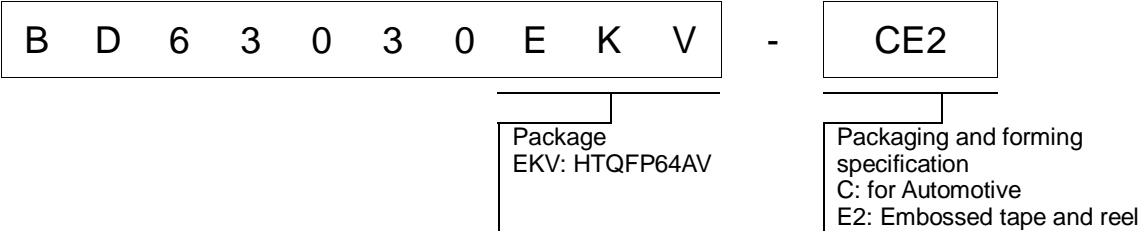
14. **Thermal Shutdown Circuit (TSD)**
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. **Over Current Protection Circuit (OCP)**
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information

| B | D | 6 | 3 | 0 | 3 | 0 | E | K | V | - | | CE2 |

Package
EKV: HTQFP64AV

Packaging and forming
specification
C: for Automotive
E2: Embossed tape and reel

Marking Diagram

HTQFP64AV (TOP VIEW)

BD63030EKV ← Part Number Marking

← LOT Number

Pin 1 Mark
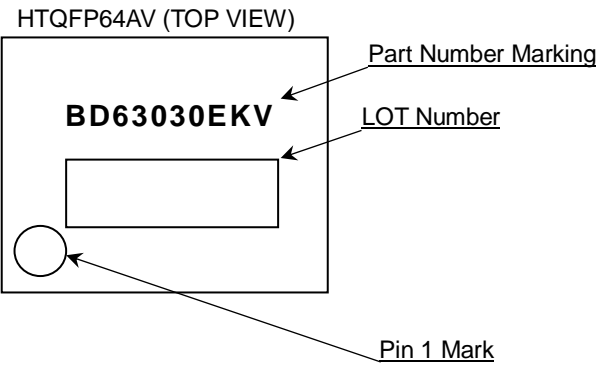
Physical Dimension and Packing Information

Package Name	HTQFP64AV

1 PIN MARK

(UNIT : mm)
PKG : HTQFP64AV
Drawing No. EX285-5001

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand

E2	TR	E2	TR	E2	TR	E2	TR	E2	TR	E2	TR
TL	E1	TL	E1	TL	E1	TL	E1	TL	E1	TL	E1

Reel

Pocket Quadrants

Direction of feed

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Revision History

Date	Revision	Changes
04.Jul.2018	002	New release.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment [Note 1], aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
    - [a] Installation of protection circuits or other protective devices to improve system safety
    - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
    - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
    - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
    - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
    - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
    - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
    - [f] Sealing or coating our Products with resin or other coating materials
    - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
    - [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document.   ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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