Precision, Funneling Instrumentation Amplifier with Level Shift and Output Clamping

FEATURES

- **Single Gain Set Resistor: G = 0.2 to >200**
- **Excellent DC Precision**
  - **Input Offset Voltage: 60µV Max**
  - **Input Offset Voltage Drift: 0.6µV/°C Max**
  - **Low Gain Error: 0.012% Max (G = 0.2)**
  - **Low Gain Drift: 35ppm/°C Max (G > 0.2)**
  - **High DC CMRR: 80dB Min (G = 0.2)**
- **Integrated Output Clamps**
- **Integrated Output Level Shift**
- Input Bias Current: 800pA Max
- 4MHz –3dB Bandwidth (G = 0.2)
- Low Noise:
  - 0.1Hz to 10Hz Noise: 0.2µV_{P-P}
  - 1kHz Voltage Noise: 7nV/√Hz
- Integrated Input RFI Filter
- Wide Supply Range 4.75V to 35V
- Temperature Ranges: –40°C to 85°C and –40°C to 125°C
- MS16E and 20-Lead 3mm × 4mm QFN Packages

APPLICATIONS

- Bridge Amplifier
- Data Acquisition
- Thermocouple Amplifier
- Strain Gauge Amplifier
- Medical Instrumentation
- Transducer Interfaces
- Differential to Single-Ended Conversion

DESCRIPTION

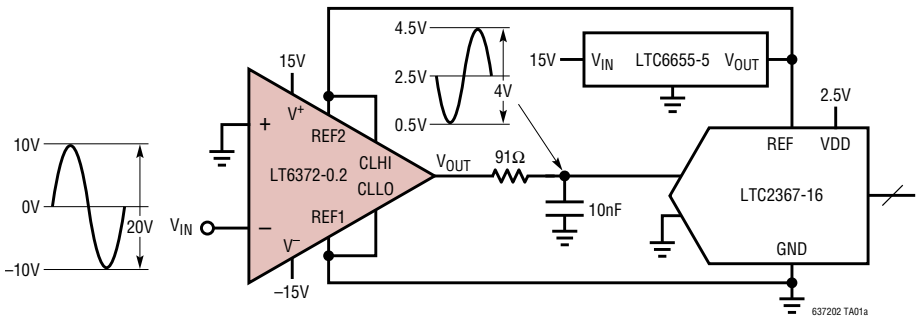
The LT®6372-0.2 is a gain programmable, high precision funneling instrumentation amplifier that delivers industry leading DC precision. This high precision enables smaller signals to be sensed and eases calibration requirements, particularly over temperature. The LT6372-0.2 incorporates features into the LT6370 which further improve accuracy and simplify interfacing to an ADC.

The LT6372-0.2 uses a proprietary high performance bipolar process which enables industry leading accuracy coupled with exceptional long-term stability. The LT6372-0.2 is laser trimmed for very low input offset voltage (60µV) and high CMRR (80dB, G = 0.2). Proprietary on-chip test capability allows the gain drift (35ppm/°C) to be guaranteed with automated testing.

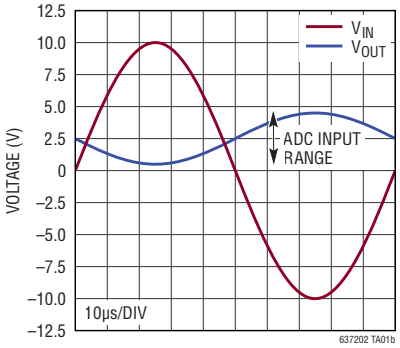
The LT6372-0.2's difference amplifier uses a split reference configuration which simplifies level shifting the amplifier's output to the center of the ADC's input range. Output clamp pins are also provided to limit the voltage which can be applied to an ADC's input. EMI filtering is integrated on the LT6372-0.2's inputs to maintain accuracy in the presence of harsh RF interference.

The LT6372-0.2 is available in a compact MS16E or a 20-pin 3mm x 4mm QFN. The LT6372-0.2 is fully specified over the –40°C to 85°C and –40°C to 125°C temperature ranges.

TYPICAL APPLICATION



LT6372-0.2 Funnels and Level Shifts ±10V Inputs to 5V ADC Input Range



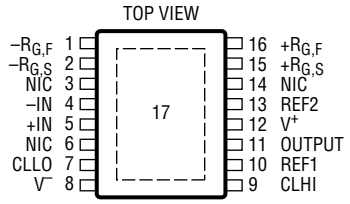
Rev. 0

ABSOLUTE MAXIMUM RATINGS

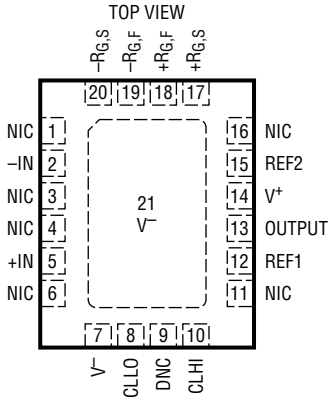
(Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Input Voltage (+IN, –IN, $+R_{G,S}$, $+R_{G,F}$, $-R_{G,S}$, $-R_{G,F}$, REF1, REF2, CLHI, CLLO) ... (V^- – 0.3V) to (V^+ + 0.3V)
Differential Input Voltage
(+IN to –IN) ..... ±36V
(REF1 to REF2) ..... ±8V
Input Current
($+R_{GS}$, $+R_{GF}$, $-R_{GS}$, $-R_{GF}$) ..... ±2mA
(+IN, –IN, CLLO) ..... ±10mA
(REF1, REF2, CLHI) ..... –10mA
Output Short-Circuit Duration ..... Thermally Limited
Output Current 80mA
Operating and Specified Temperature Range
I-Grade ..... –40°C to 85°C
H-Grade ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP
θ_{JA} = 35°C/W
EXPOSED PAD (PIN 17) MUST FLOAT OR
BE CONNECTED TO V^+ IN ADDITION TO PIN 12



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN
θ_{JA} = 52°C/W
EXPOSED PAD (PIN 21) IS CONNECTED
TO V^- (PIN 7) (PCB CONNECTION OPTIONAL)

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6372IMSE-0.2#PBF	LT6372IMSE-0.2#TRPBF	637202	16-Lead Plastic MSOP	–40°C to 85°C
LT6372HMSE-0.2#PBF	LT6372HMSE-0.2#TRPBF	637202	16-Lead Plastic MSOP	–40°C to 125°C
LT6372IUDC-0.2#PBF	LT6372IUDC-0.2#TRPBF	LHHQ	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 85°C
LT6372HUDC-0.2#PBF	LT6372HUDC-0.2#TRPBF	LHHQ	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4kΩ.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G	Gain Range	G = 0.2 • (1 + 24.2k/R_G) (Note 2)		0.2		200	V/V
	Gain Error (Notes 3, 4)	G = 0.2			0.002	0.012	%
		G = 0.2	●			0.015	%
		G = 1			0.01	0.15	%
		G = 1	●			0.45	%
		G = 10			0.02	0.15	%
		G = 10	●			0.45	%
		G = 100			0.02	0.15	%
		G = 100	●			0.45	%
		G = 200			0.03	0.15	%
		G = 200	●			0.53	%
	Gain vs Temperature (Notes 3, 4)	G = 0.2 (Note 5)	●		0.2	0.5	ppm/°C
		G > 0.2 (Note 6)	●		20	35	ppm/°C
	Gain Nonlinearity (Notes 3, 7)	V_{OUT} = 0V to 4.096V, G = 0.2			3	5	ppm
		V_{OUT} = 0V to 4.096V, G = 1			4	60	ppm
		V_{OUT} = 0V to 4.096V, G = 10			5	80	ppm
		V_{OUT} = 0V to 4.096V, G = 100			6		ppm
		V_{OUT} = 0V to 4.096V, G = 200			12		ppm
V_{OST}, Total Input Referred Offset Voltage, V_{OST} = V_{OSI} + V_{OSO}/G							
V_{OSI}	Input Offset Voltage (Note 8)				±15	±60	µV
			●			±175	µV
V_{OSO}	Output Offset Voltage (Note 8)				±30	±175	µV
			●			±300	µV
V_{OSI}/T	Input Offset Voltage Drift (Notes 5, 8)		●			±0.6	µV/°C
	Input Offset Voltage Hysteresis (Note 9)	T_A = –40°C to 125°C	●		±3		µV
V_{OSO}/T	Output Offset Voltage Drift (Notes 5, 8)		●			±2	µV/°C
	Output Offset Voltage Hysteresis (Note 9)	T_A = –40°C to 125°C	●		±10		µV
I_B	Input Bias Current				±0.1	±0.8	nA
		T_A = –40°C to 85°C	●			±1.5	nA
		T_A = –40°C to 125°C	●			±3	nA
I_{OS}	Input Offset Current				±0.2	±1.4	nA
			●			±4	nA
	Input Noise Voltage (Note 10)	0.1Hz to 10Hz, G = 0.2			4		$µV_{P-P}$
		0.1Hz to 10Hz, G = 200			0.2		$µV_{P-P}$
Total RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$ (Note 10)							
e_{ni}	Input Noise Voltage Density	f = 1kHz			7		nV/√Hz
e_{no}	Output Noise Voltage Density	f = 1kHz			32		nV/√Hz
	Input Noise Current	0.1Hz to 10Hz			10		pA_{P-P}
i_n	Input Noise Current Density	f = 1kHz			200		fA/√Hz
R_{IN}	Input Resistance	V_{IN} = –12.6V to 13V			225		GΩ
C_{IN}	Differential	f = 100kHz			0.9		pF
	Common Mode	f = 100kHz			15.9		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR		V^- + 1.8/V^+ – 1.4			V
			●	V^- + 2.4		V^+ – 2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4kΩ.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	DC to 60Hz, 1k Source Imbalance, V_{CM} = –12.6V to 13V					
		G = 0.2		80	96		dB
		G = 0.2	●	74			dB
		G = 1		95	110		dB
		G = 1	●	89			dB
		G = 10		114	130		dB
		G = 10	●	108			dB
		G = 100			146		dB
		G = 200		125	146		dB
		G = 200	●	119			dB
	AC Common Mode Rejection Ratio	f = 20kHz, QFN20 Package					
		G = 0.2			62		dB
		G = 2			82		dB
		G = 20			104		dB
		G = 200			104		dB
		f = 20kHz, MS16E Package					
		G = 0.2			80		dB
		G = 2			100		dB
		G = 20			104		dB
		G = 200			104		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±17.5V					
		G = 0.2		106	121		dB
		G = 0.2	●	104			dB
		G = 1		120	135		dB
		G = 1	●	117			dB
		G = 10		128	140		dB
		G = 10	●	122			dB
		G = 100		128	142		dB
		G = 100	●	122			dB
		G = 200			146		dB
V_S	Supply Voltage	Guaranteed by PSRR	●	4.75		35	V
I_S	Supply Current	V_S = ±15V			2.75	2.85	mA
		T_A = –40°C to 85°C	●			3	mA
		T_A = –40°C to 125°C	●			3.1	mA
		V_S = ±2.375V			2.65	2.7	mA
		T_A = –40°C to 85°C	●			2.85	mA
		T_A = –40°C to 125°C	●			2.95	mA
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 10kΩ		–14.4	–14.7/14	13.6	V
			●	–14.2		13.5	V
		V_S = ±2.375V, R_L = 10kΩ		–0.7	–1/1.6	1.4	V
			●	–0.5		1.2	V
I_{OUT}	Output Short Circuit Current			35	55		mA
			●	30			mA
BW	–3dB Bandwidth	G = 0.2			4		MHz
		G = 1			2		MHz
		G = 10			1		MHz
		G = 100			140		kHz
		G = 200			15		kHz
SR	Slew Rate	G = 1, V_{OUT} = ±2.5V			3.5		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4kΩ.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_S	Settling Time	4.096V Output Step to 0.0015% G = 0.2 G = 1 G = 10 G = 100 G = 200			 1.8 2.5 12.4 68 135		 µs µs µs µs µs
R_{REFIN}	REF Input Resistance	REF1 or REF2, Untested REF pin floating			14		kΩ
I_{REFIN}	REF Input Current	V_{+IN} = $V_{–IN}$ = V_{REF1} = V_{REF2}= 0V, REF1 or REF2	 ●	–36 –50	–24	–12 0	µA µA
V_{REF}	REF Voltage Range	REF1 or REF2	●	V^-		V^+	V
A_{VREF}	REF Gain to Output	V_{REF1} = 0V to 5V, V_{REF2} = 0V			0.5		V/V
	REF Gain Error	V_{REF1} = 0V to 5V, V_{REF2} = 0V	 ●	–250 –300	±75	250 300	ppm ppm
	CLLO Input Current	V_{CLLO} = 0V	●			1	µA
	CLHI Input Current	V_{CLHI} = 5V	●			1	µA
	CLLO Input Operating Voltage Range	Outside this Range CLLO is Disabled	●	V^- + 3		V^+ – 2	V
	CLHI Input Operating Voltage Range	Outside this Range CLHI is Disabled	●	V^- + 2		V^+ – 2.5	V
	CLLO Clamp Voltage (V_{OUT} – V_{CLLO})		 ●	–0.57 –0.74	–0.45		V V
	CLHI Clamp Voltage (V_{OUT} – V_{CLHI})		 ●		0.45	0.55 0.755	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Gains higher than 200 are possible but the resulting low R_G values can make PCB and package lead resistance a significant error source.

Note 3: For gains greater than 0.2V/V, gain tests are performed with –IN at mid-supply and +IN driven. The gain of 0.2V/V testing is performed with –IN and +IN driven differentially.

Note 4: When the gain is greater than 0.2 the gain error and gain drift specifications do not include the effect of external gain set resistor R_G.

Note 5: This specification is guaranteed by design.

Note 6: This specification is guaranteed with high-speed automated testing.

Note 7: This parameter is measured in a high speed automatic tester that does not measure the thermal effects with longer time constants. The magnitude of these thermal effects are dependent on the package used, PCB layout, heat sinking and air flow conditions.

Note 8: For more information on how offsets relate to the amplifiers, see section “Input and Output Offset Voltage” in the Applications section.

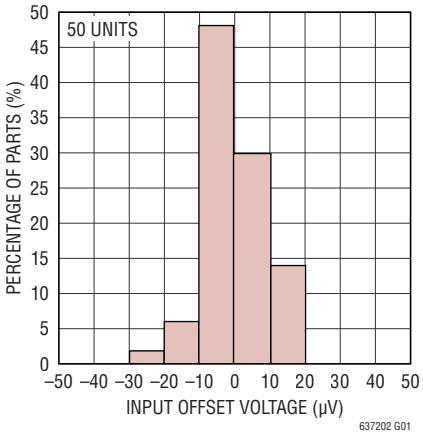
Note 9: Hysteresis in output voltage is created by mechanical stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis is roughly proportional to the square of the temperature change. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature), hysteresis is usually not a significant error source. Typical hysteresis is the worst case of 25°C to cold to 25°C or 25°C to hot to 25°C, preconditioned by one thermal cycle.

Note 10: Referred to the input.

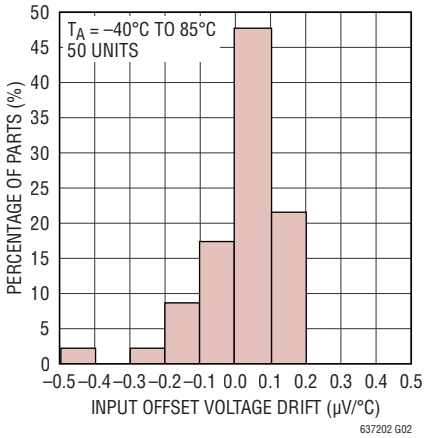
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4k, unless otherwise noted.

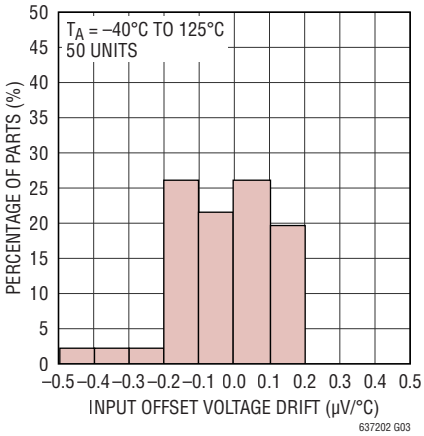
Distribution of Input Offset Voltage, MS16E Package



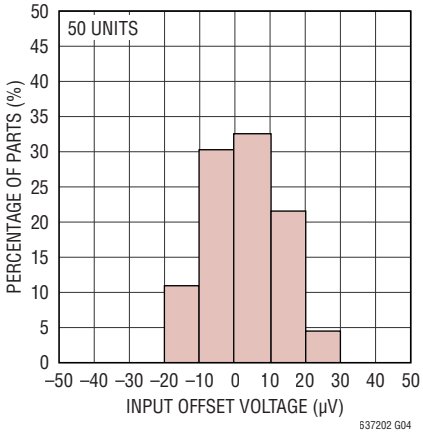
Distribution of Input Offset Voltage Drift, MS16E Package



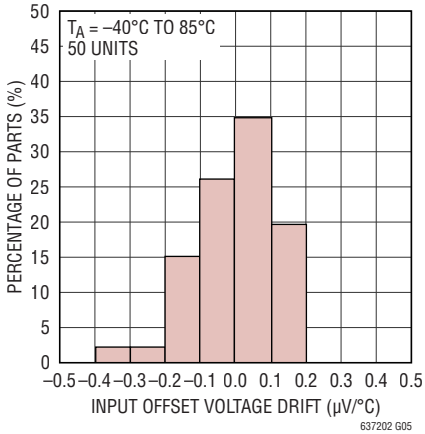
Distribution of Input Offset Voltage Drift, MS16E Package



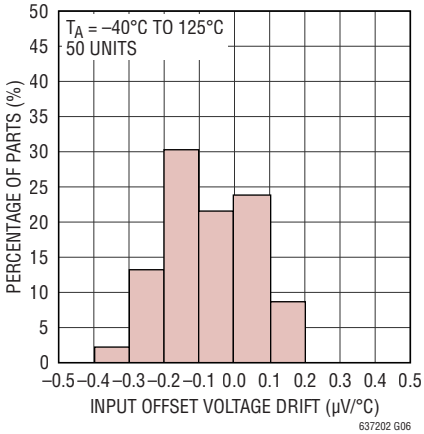
Distribution of Input Offset Voltage, QFN Package



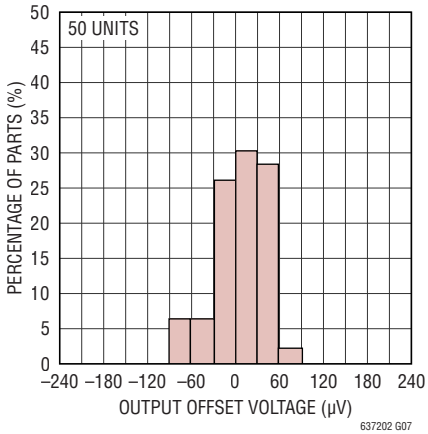
Distribution of Input Offset Voltage Drift, QFN Package



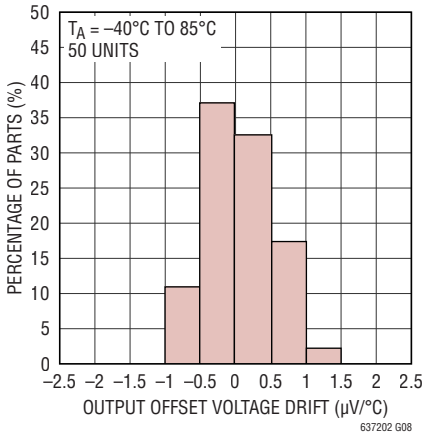
Distribution of Input Offset Voltage Drift, QFN Package



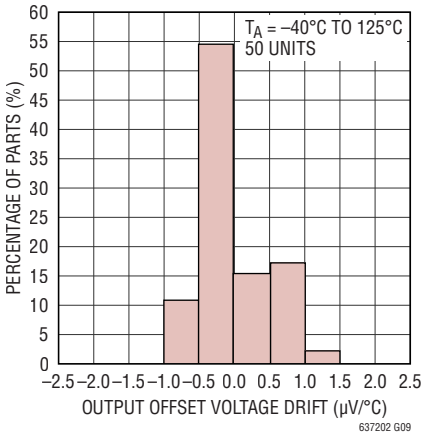
Distribution of Output Offset Voltage, MS16E Package



Distribution of Output Offset Voltage Drift, MS16E Package



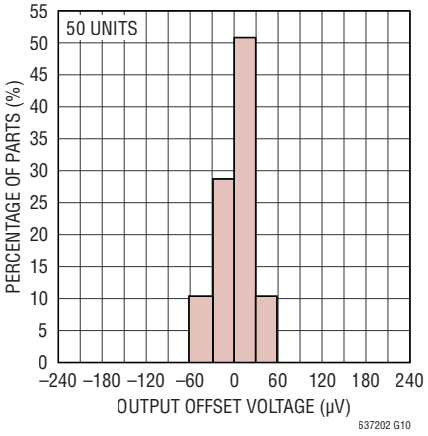
Distribution Output Offset Voltage Drift, MS16E Package



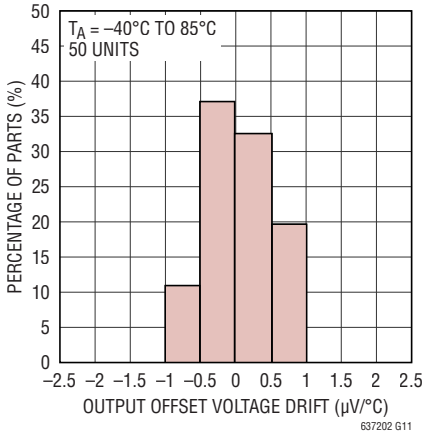
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4k, unless otherwise noted.

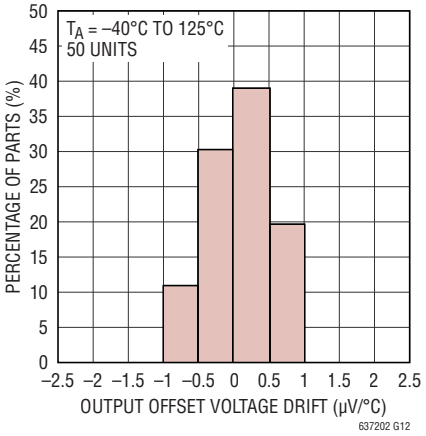
Distribution of Output Offset Voltage, QFN Package



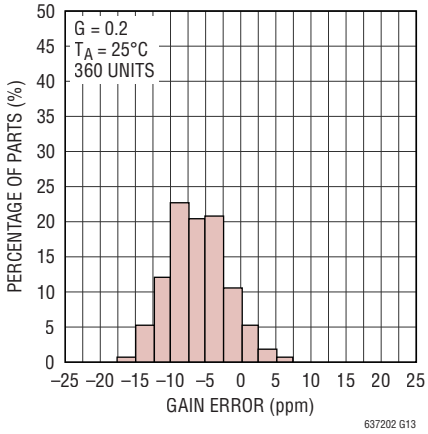
Distribution of Output Offset Voltage Drift, QFN Package



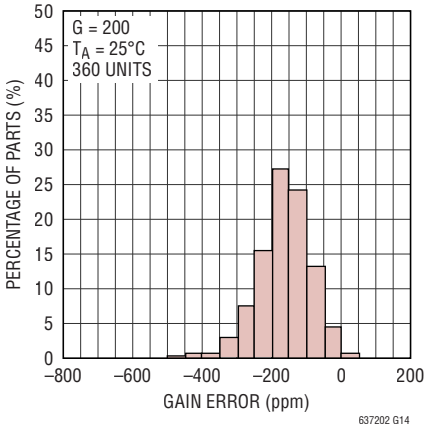
Distribution of Output Offset Voltage Drift, QFN Package



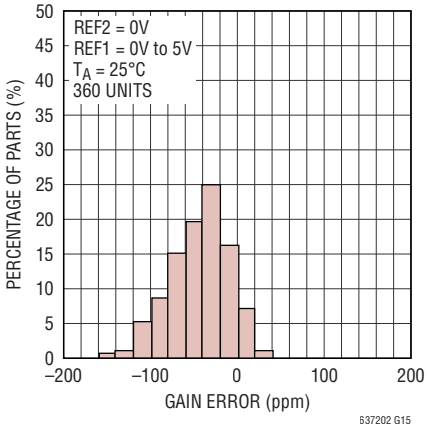
Distribution of Gain Error



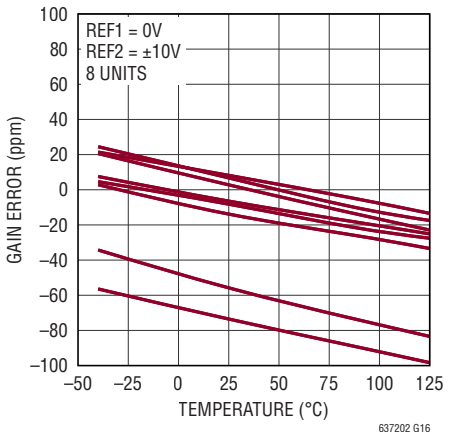
Distribution of Gain Error



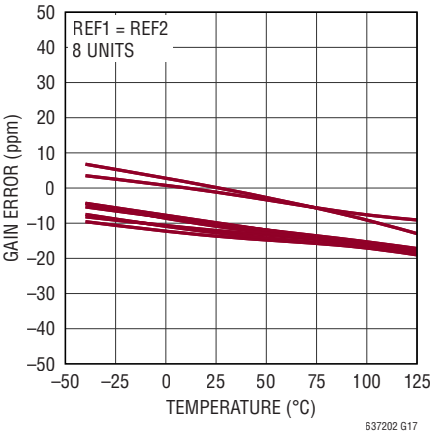
Distribution of REF Divide Gain Error



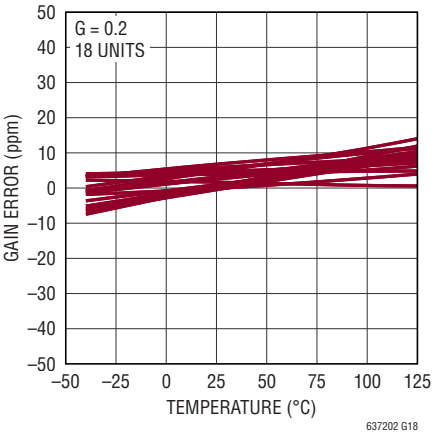
REF Divider Gain Drift



REF Gain Drift



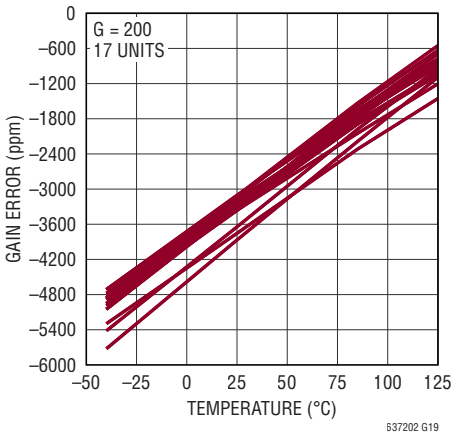
Gain Drift (G = 0.2)



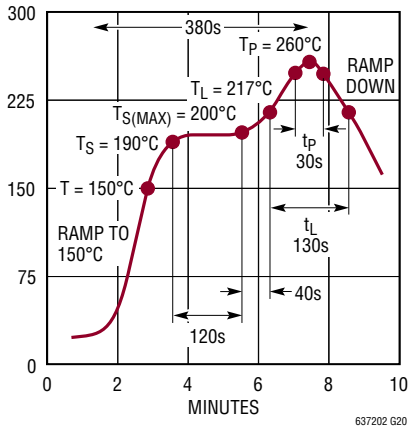
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4k, unless otherwise noted.

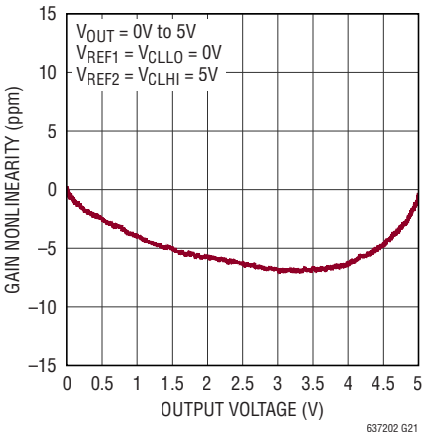
Gain Drift (G = 200)



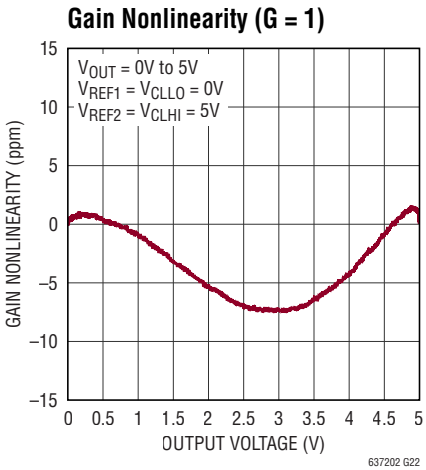
Lead Free Reflow Profile Due to IR Reflow



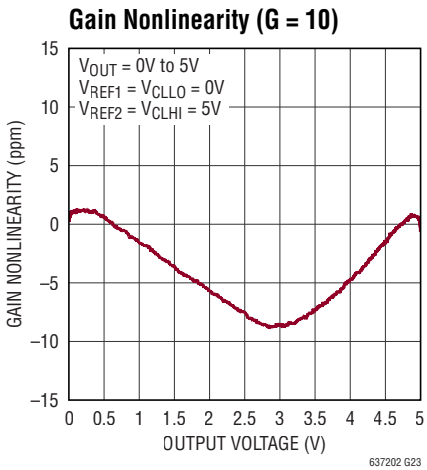
Gain Nonlinearity (G = 0.2)



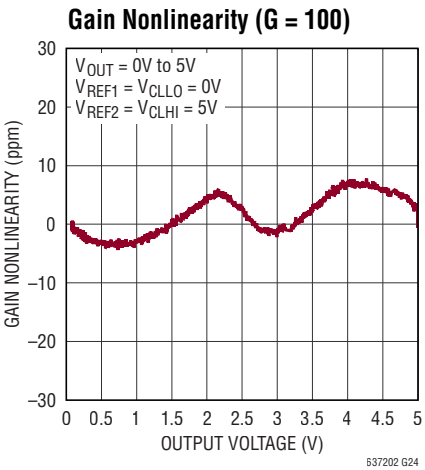
Gain Nonlinearity (G = 1)



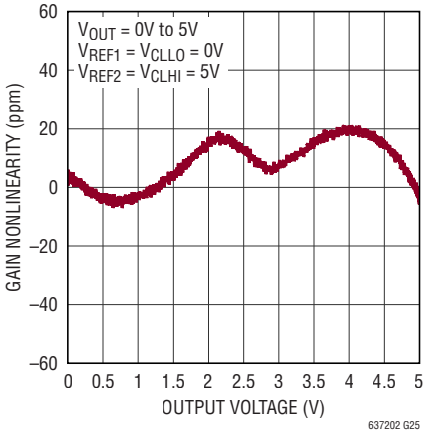
Gain Nonlinearity (G = 10)



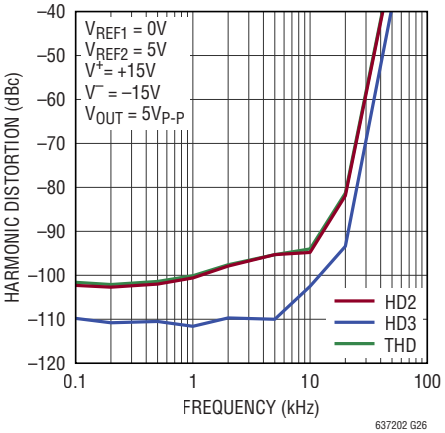
Gain Nonlinearity (G = 100)



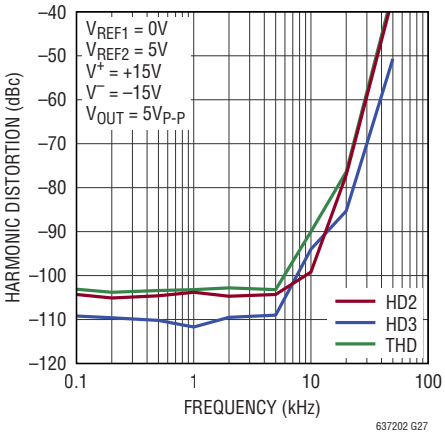
Gain Nonlinearity (G = 200)



Harmonic Distortion vs Frequency, G = 0.25, R_L = 2k



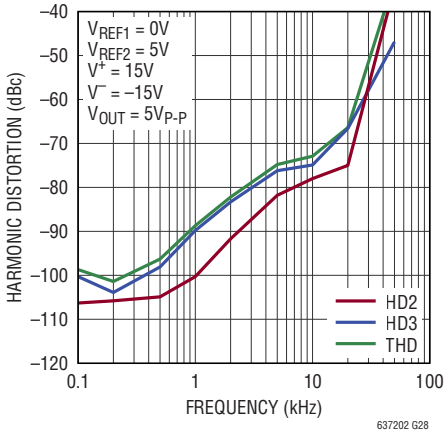
Harmonic Distortion vs Frequency, G = 1, R_L = 2k



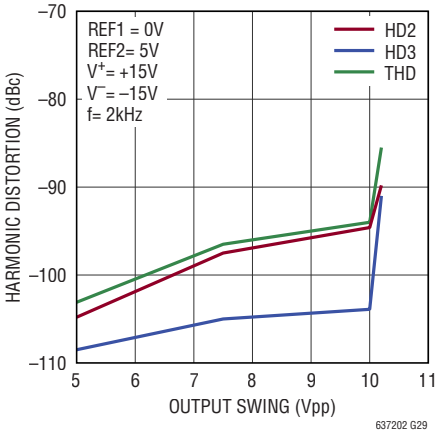
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4k, unless otherwise noted.

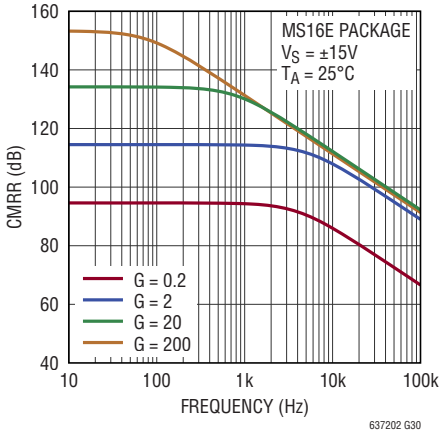
Harmonic Distortion vs Frequency, G = 10, R_L = 2k



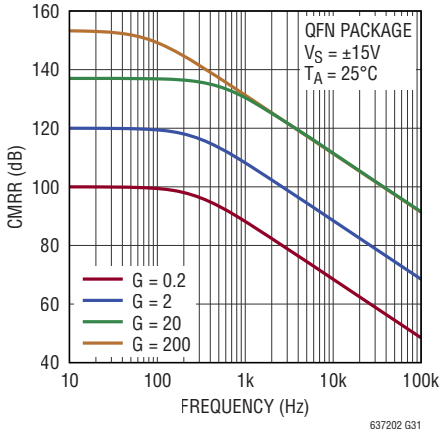
Harmonic Distortion vs Output Swing, G = 10, R_L = 2k



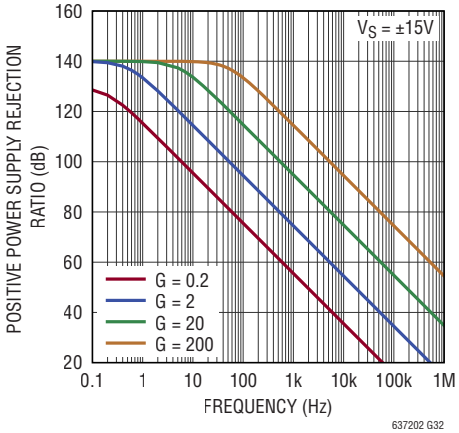
CMRR vs Frequency, RTI MS16E Package



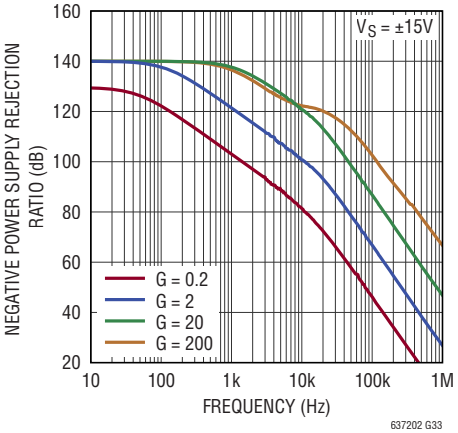
CMRR vs Frequency, RTI QFN Package



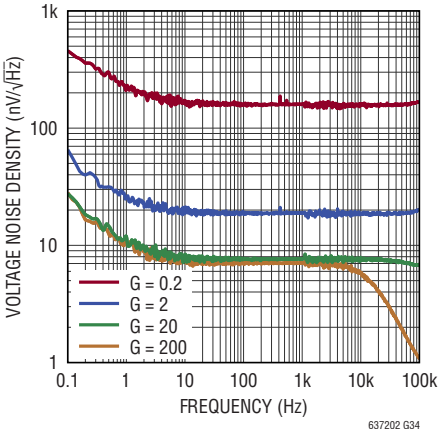
Positive Power Supply Rejection Ratio vs Frequency



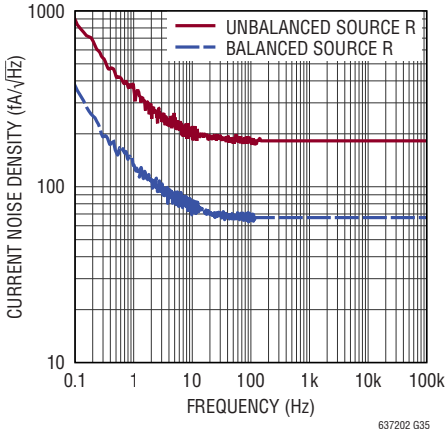
Negative Power Supply Rejection Ratio vs Frequency



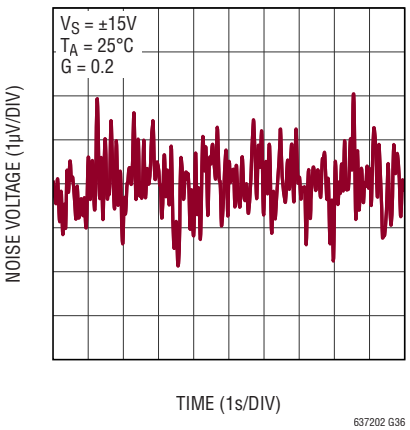
Input-Referred Voltage Noise Density vs Frequency



Current Noise Density vs Frequency



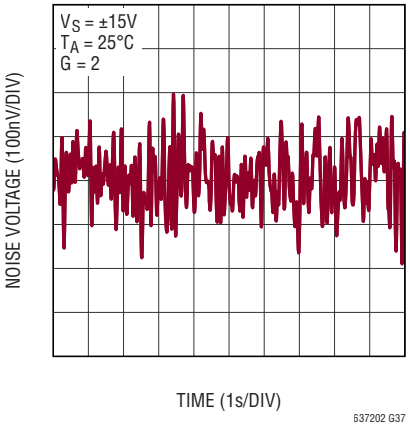
0.1Hz to 10Hz Noise Voltage, G = 0.2, RTI



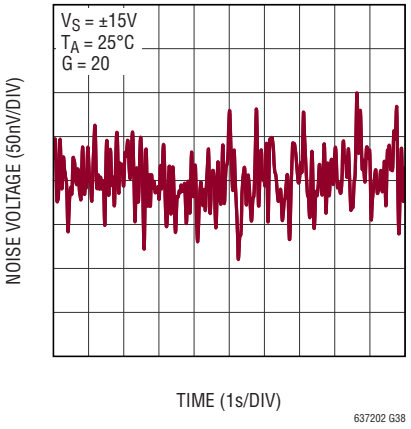
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4k, unless otherwise noted.

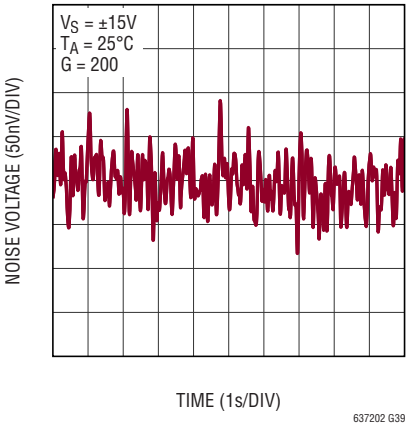
0.1Hz to 10Hz Noise Voltage, G = 2, RTI



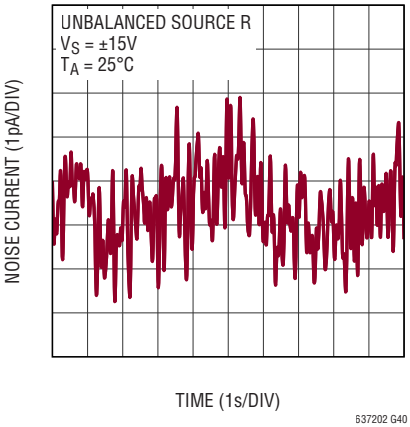
0.1Hz to 10Hz Noise Voltage, G = 20, RTI



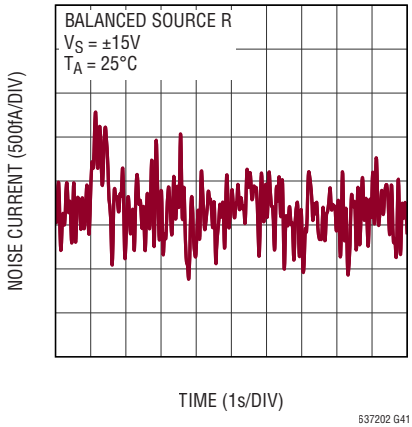
0.1Hz to 10Hz Noise Voltage, G = 200, RTI



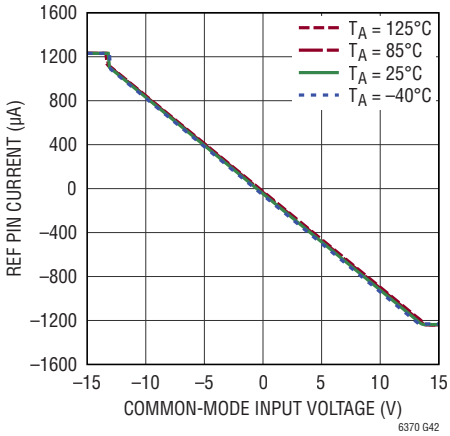
0.1Hz to 10Hz Noise Current, Unbalanced Source R



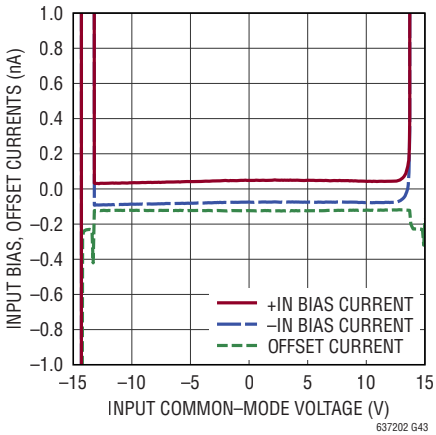
0.1Hz to 10Hz Noise Current, Balanced Source R



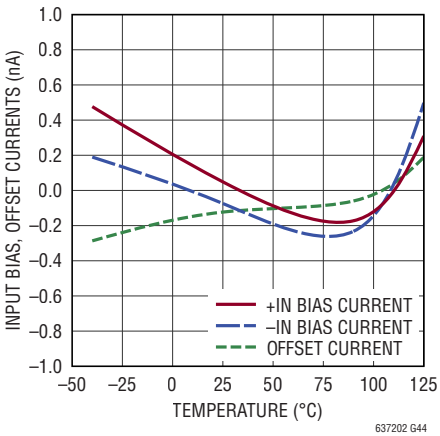
REF Pin Current vs Input Common Mode Voltage



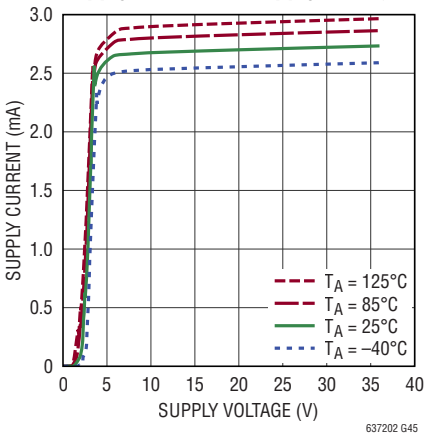
Input Bias Current vs Common Mode Voltage



Input Bias and Offset Current vs Temperature



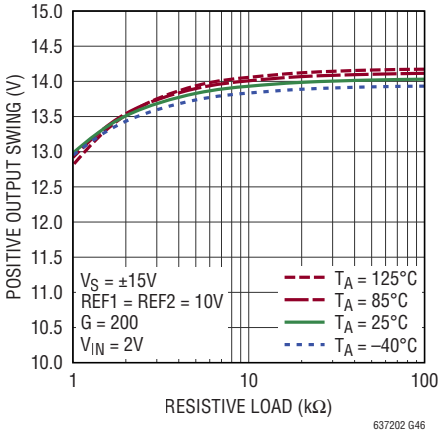
Supply Current vs Supply Voltage



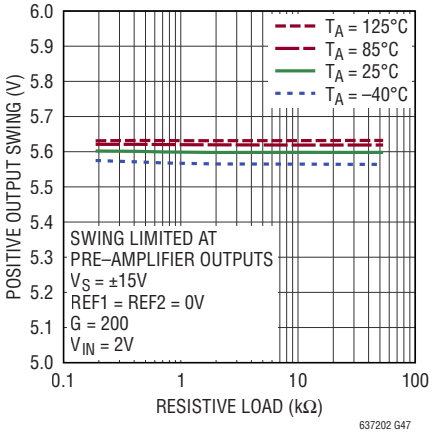
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4k, unless otherwise noted.

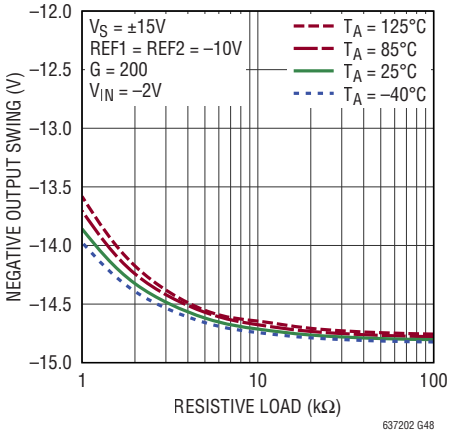
Positive Output Swing vs Resistive Load



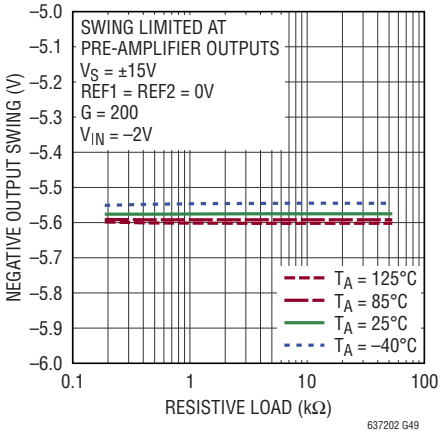
Positive Output Swing vs Resistive Load



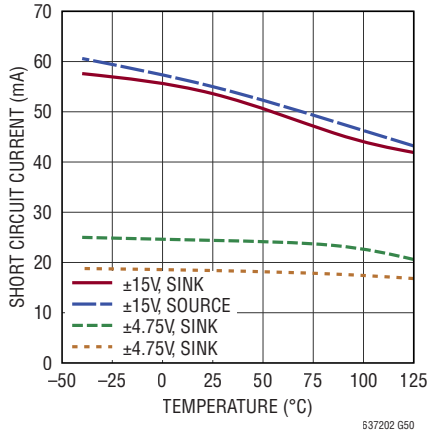
Negative Output Swing vs Resistive Load



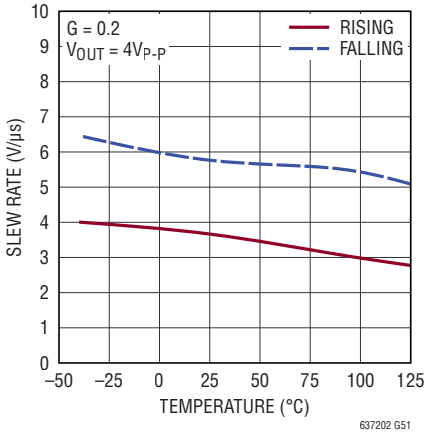
Negative Output Swing vs Resistive Load



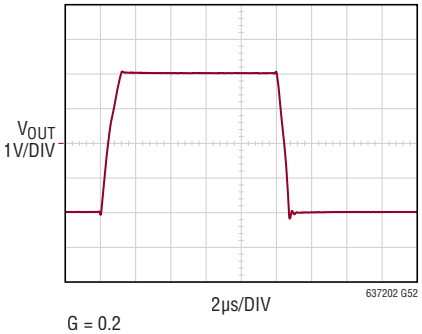
Short-Circuit Current vs Temperature



Slew Rate vs Temperature

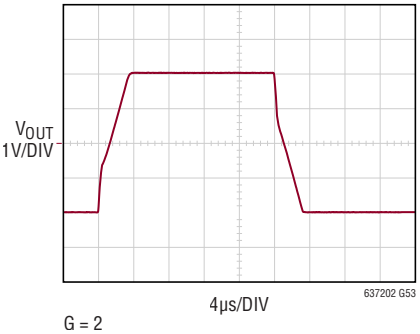


Large Signal Transient Response



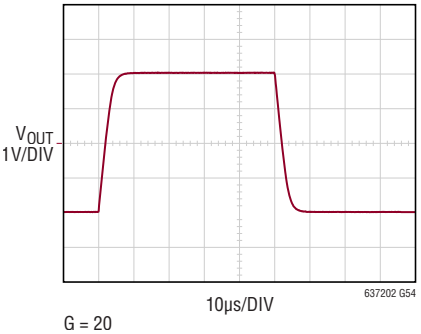
G = 0.2
V_S = ±15V
T_A = 25°C
C_L = 100pF

Large Signal Transient Response



G = 2
V_S = ±15V
T_A = 25°C
C_L = 100pF

Large Signal Transient Response

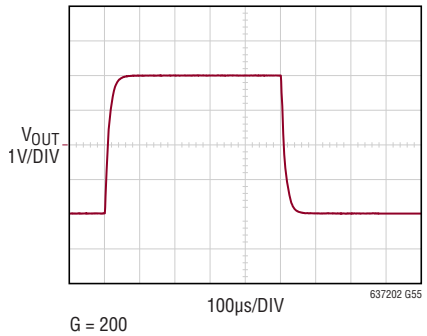


G = 20
V_S = ±15V
T_A = 25°C
C_L = 100pF

TYPICAL PERFORMANCE CHARACTERISTICS

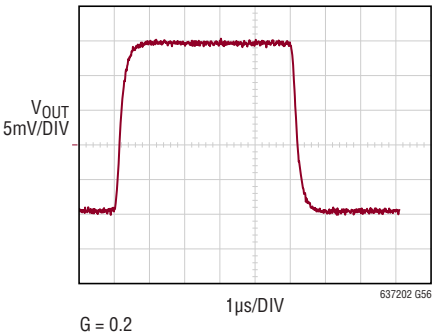
T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 4k, unless otherwise noted.

Large Signal Transient Response



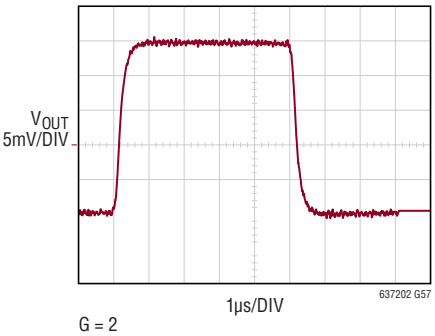
G = 200
V_S = ±15V
T_A = 25°C
C_L = 100pF

Small Signal Transient Response



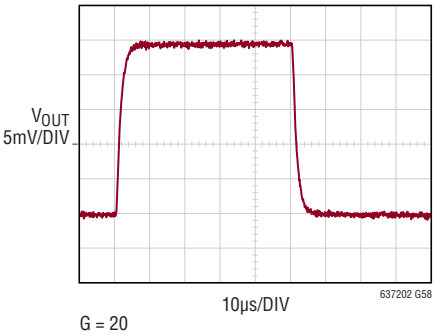
G = 0.2
V_S = ±15V
T_A = 25°C
C_L = 100pF

Small Signal Transient Response



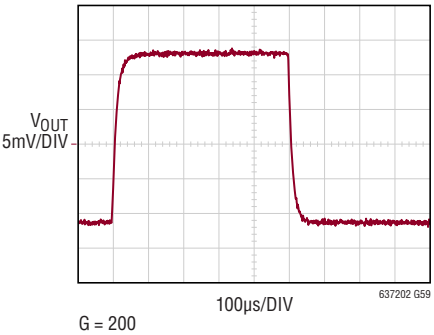
G = 2
V_S = ±15V
T_A = 25°C
C_L = 100pF

Small Signal Transient Response



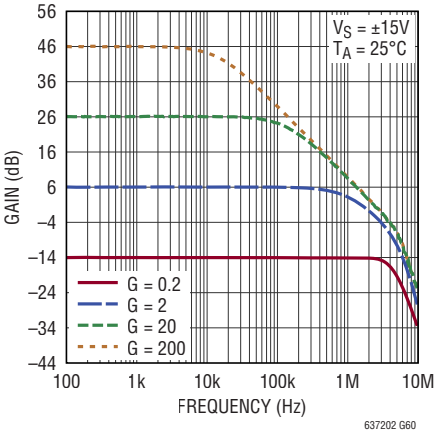
G = 20
V_S = ±15V
T_A = 25°C
C_L = 100pF

Small Signal Transient Response

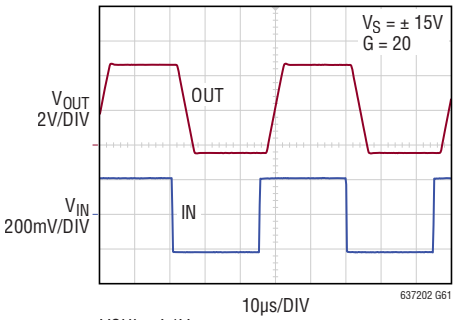


G = 200
V_S = ±15V
T_A = 25°C
C_L = 100pF

Gain vs Frequency

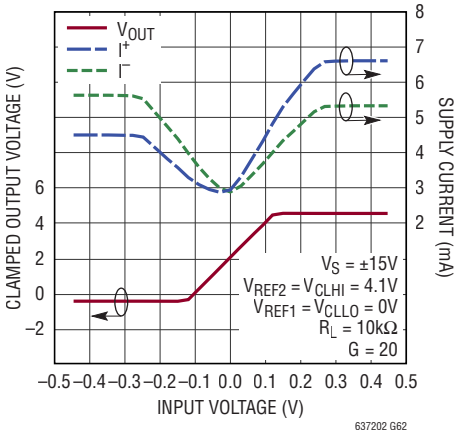


Clamp Transient Response

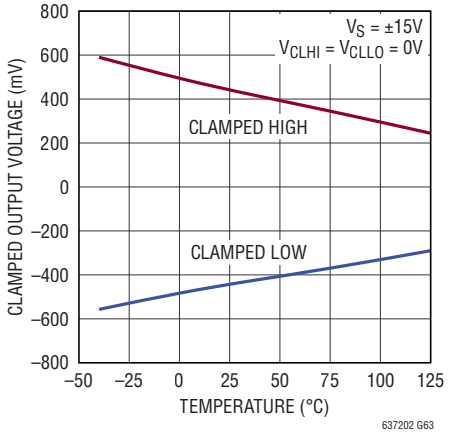


VCHI = 4.1V
VCLO = 0V
V_{REF1} = 0V
V_{REF2} = 4.1V

Supply Current While Clamping



Clamp Voltage vs Temperature



PIN FUNCTIONS (MS16E/QFN20)

$-R_{G,F}$ (Pin 1/Pin 19): For use with an external gain setting resistor. This connection should be routed to the gain setting resistor separately from $-R_{G,S}$ in order to minimize gain errors.

$-R_{G,S}$ (Pin 2/Pin 20): For use with an external gain setting resistor. This connection should be routed to the gain setting resistor separately from $-R_{G,F}$ in order to minimize gain errors.

–IN (Pin 4/Pin 2): Negative Input Terminal. This input is high impedance.

+IN (Pin 5/Pin 5): Positive Input Terminal. This input is high impedance.

CLLO (Pin 7/Pin 8): Low Side Clamp Input. The voltage applied to the CLLO pin defines the lower voltage limit of the output. Typically, the output clamps 500mV below the voltage applied to the CLLO pin. Do not float CLLO.

V^- (Pin 8/Pin 7): Negative Power Supply. A bypass capacitor should be used between supply pins and ground.

CLHI (Pin 9/Pin 10): High Side Clamp Input. The voltage applied to the CLHI pin defines the upper voltage limit of the output. Typically, the output clamps 500mV above the voltage applied to the CLHI pin. Do not float CLHI.

REF1 (Pin 10/Pin 12): Reference for the output voltage. REF1 can be tied to REF2 and used as a reference for the output. REF1 can also be used with REF2 to form a voltage divider and level shift the output.

OUTPUT (Pin 11/Pin 13): Output voltage referenced to the REF pins.

V^+ (Pin 12/Pin 14): Positive Power Supply. A bypass capacitor should be used between supply pins and ground.

REF2 (Pin 13/Pin 15): Reference for the output voltage. REF2 can be tied to REF1 and used as a reference for the output. REF2 can also be used with REF1 to form a voltage divider and level shift the output.

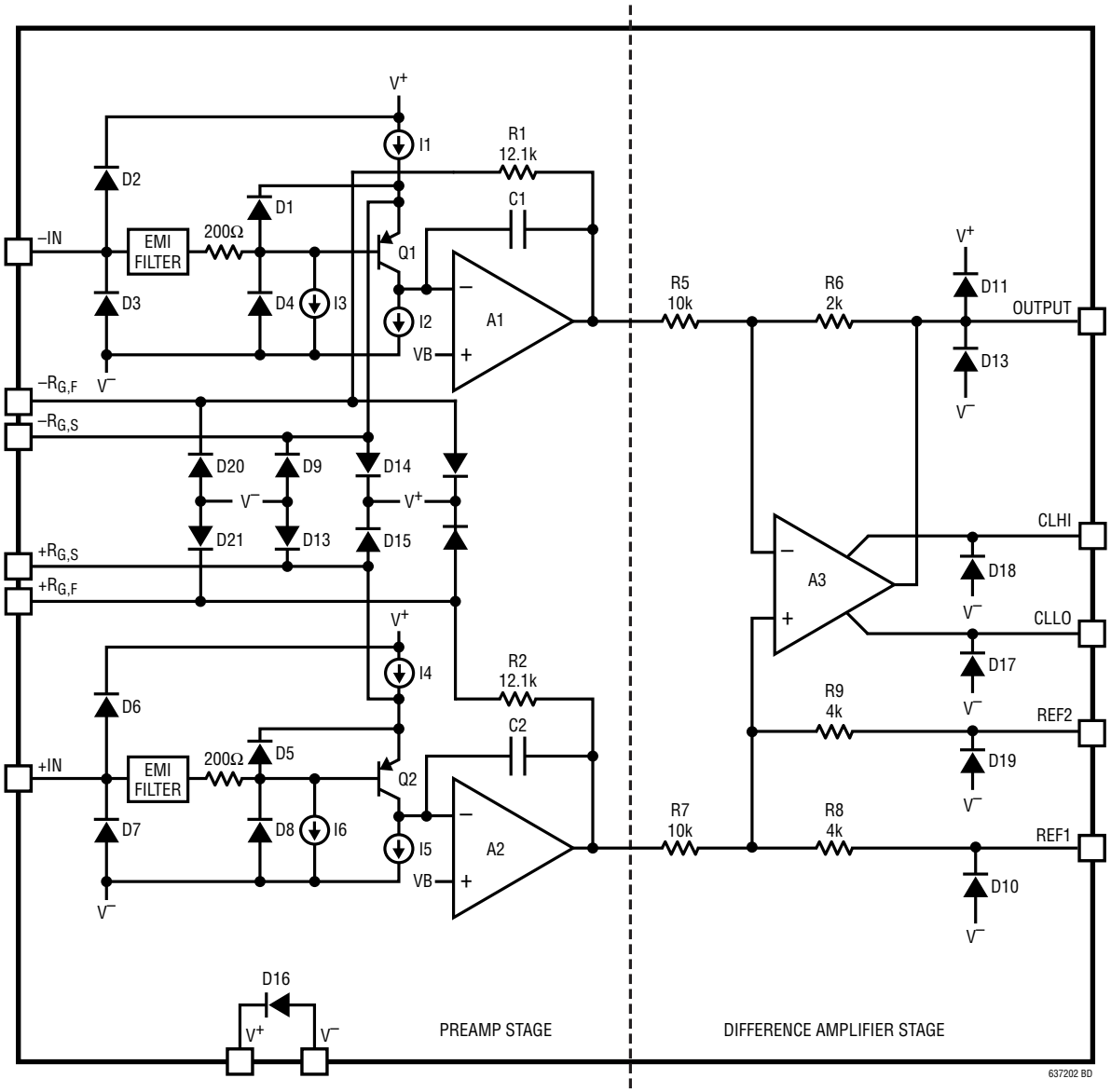
$+R_{G,S}$ (Pin 15/Pin 17): For use with an external gain setting resistor. This connection should be routed to the gain setting resistor separately from $+R_{G,F}$ in order to minimize gain errors.

$+R_{G,F}$ (Pin 16/Pin 18): For use with an external gain setting resistor. This connection should be routed to the gain setting resistor separately from $+R_{G,S}$ in order to minimize gain errors.

NIC (Pins 3, 6, 14/Pins 1, 3, 4, 6, 11, 16): No Internal Connection.

DNC (QFN Pin 9): Do Not Connect. This pin should float.

SIMPLIFIED BLOCK DIAGRAM



THEORY OF OPERATION

The LT6372-0.2 is an improved version of the classic three op amp instrumentation amplifier topology that incorporates features to improve accuracy and simplify interfacing to ADCs. Laser trimming and proprietary monolithic construction allow for tight matching and extremely low drift of circuit parameters over the specified temperature range. Refer to the Simplified Block Diagram to aid in understanding the following circuit description. The collector currents in Q1 and Q2 as well as I1 and I4 are trimmed to minimize input offset voltage drift, thus assuring a high level of performance. R1 and R2 are trimmed to an absolute value of 12.1k to assure that the gain can be set accurately (0.15% at G = 100) with only one external resistor, R_G. The value of R_G determines the transconductance of the preamp stage. As R_G is reduced to increase the programmed gain, the transconductance of the input preamp stage also increases to that of the input transistors Q1 and Q2. This causes the open-loop gain to increase when the programmed gain is increased, reducing the input related errors and noise. The input voltage noise at high gains is determined only by Q1 and Q2. At lower gains, noise of the difference amplifier and preamp gain setting resistors may increase the noise. The gain bandwidth product is determined by C1, C2 and the preamp transconductance, which increases with programmed gain. Therefore, the bandwidth is self-adjusting and does not drop directly proportional to gain.

The input transistors Q1 and Q2 offer excellent matching, drift and noise performance, which is due to using a proprietary high performance process, as well as low input bias current due to the high beta of these input devices. The input bias current is further reduced by trimming I3 and I6. The collector currents in Q1 and Q2 are held constant due to the feedback through the Q1-A1-R1 loop and Q2-A2-R2 loop. The action of the amplifier loops impresses the differential input voltage across the external gain set resistor R_G. Since the current that flows through R_G also flows through R1 and R2, the ratios provide a gained-up differential voltage,

$$G = 1 + \frac{R1 + R2}{R_G}$$

to the difference amplifier A3. The difference amplifier removes the common mode voltage and provides a single-ended output voltage referenced to the average of the voltages on REF1 and REF2. This split reference resistor configuration allows the output voltage to be easily level shifted to the center of an ADCs input range without external components. The offset voltage of the difference amplifier is trimmed to minimize output offset voltage drift, thus assuring a high level of performance, even in low gains. Resistors R5 to R9 are trimmed to maximize CMRR and minimize gain error. The resulting gain equation is:

$$G = 0.2\left(1 + \frac{24.2k}{R_G}\right)$$

Solving for the gain set resistor gives:

$$R_G = \frac{24.2k}{5G - 1}$$

Table 1 shows appropriate 1% resistor values for a variety of gains.

Table 1. LT6372-0.2 Gain and R_G Lookup.

Resulting Gains for Various 1% Standard Resistor Values	
Gain	**Standard 1% Resistor Value (Ω)**
0.2	–
0.399	24.3k
0.499	16.2k
0.8	8.06k
1.001	6.04k
2.013	2.67k
5.04	1k
9.9	499
20.12	243
49.79	97.6
99.58	48.7
199.4	24.3
496.1	9.76
994	4.87

Additionally, The LT6372-0.2 has two integrated output voltage clamps which can be used to limit the voltage

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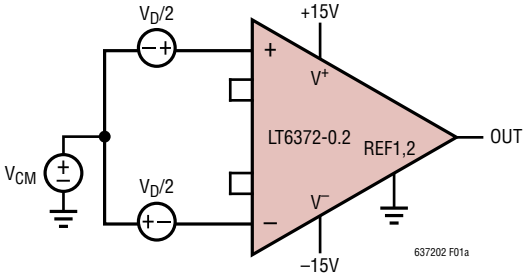
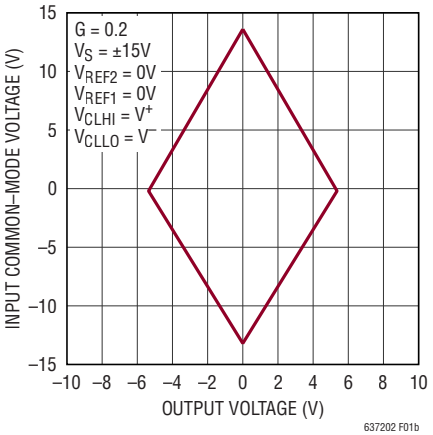
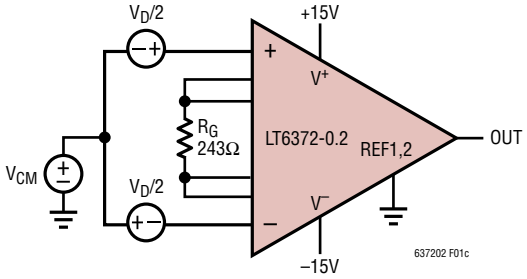
applied to an ADCs input. Typically, CLHI is tied to the ADC's reference and CLLO is tied to the ADC's ground connection.

Valid Input and Output Range

Instrumentation amplifiers traditionally specify a valid input common mode range and an output swing range. This however often fails to identify limitations associated with internal swing limits. Referring to the Simplified Block Diagram, the output swing of pre-amplifiers A1 and A2 as well as the common-mode input range of the difference amplifier A3 impose limitations on the valid operating range. Figure 1 shows the operating region where a valid output is produced for various configurations. Further valid input and output range plots can be generated using the Diamond Plot Tool.







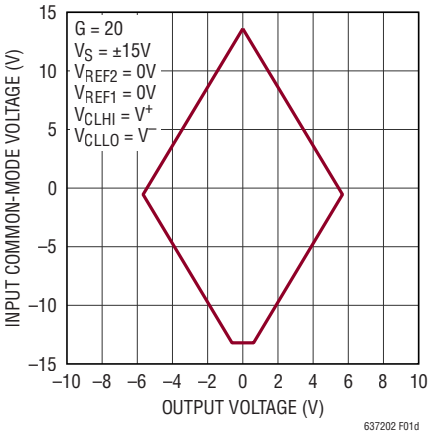
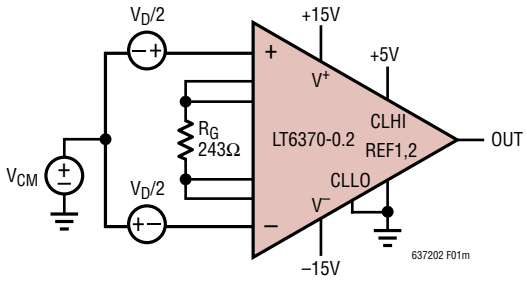
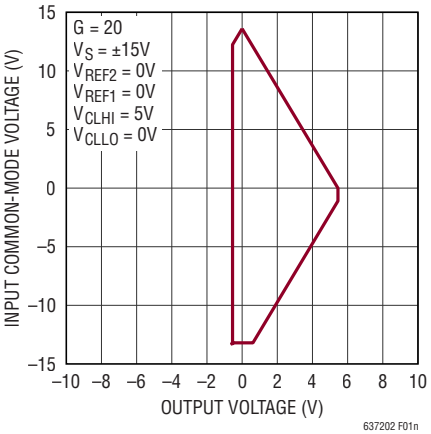
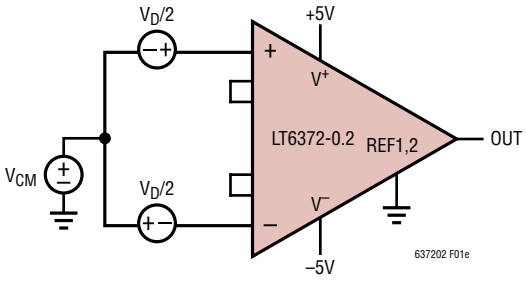


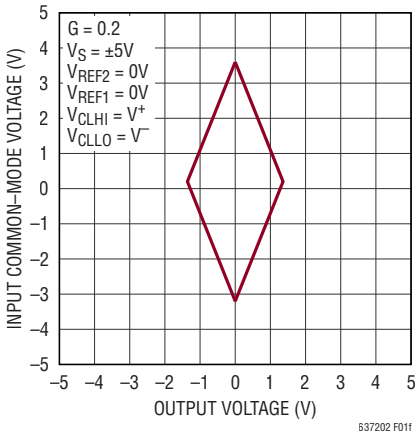
Figure 1. Input Common Mode Range vs Output Voltage

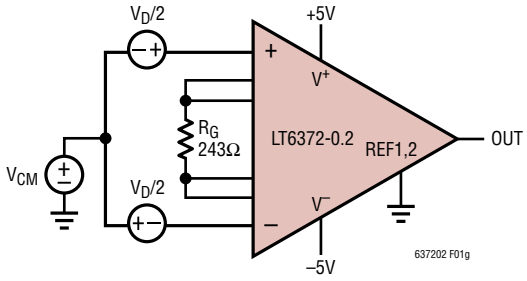
APPLICATIONS INFORMATION











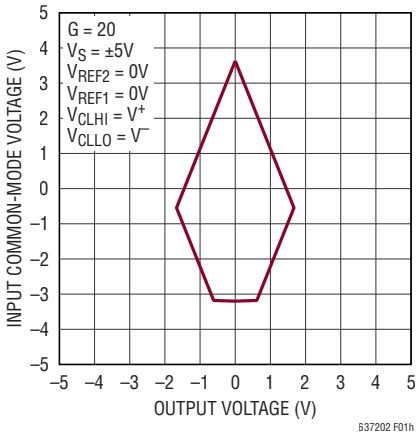
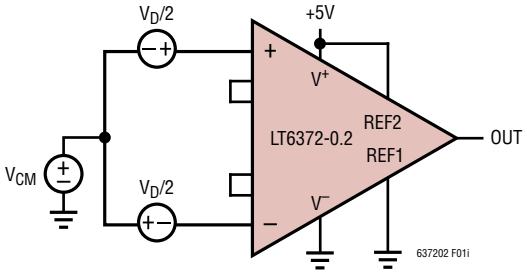
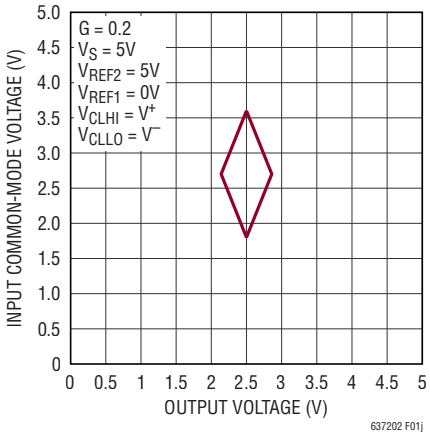
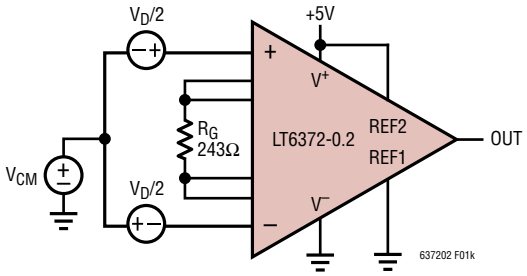


Figure 1 (Continued). Input Common Mode Range vs Output Voltage

APPLICATIONS INFORMATION







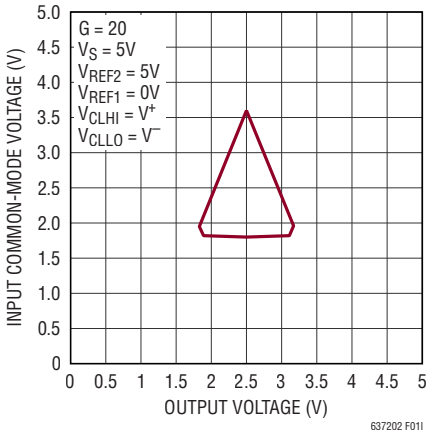


Figure 1 (Continued). Input Common Mode Range vs Output Voltage

APPLICATIONS INFORMATION

Output Level Shifting with Split Reference Pins

The LT6372-0.2's difference amplifier features split reference pins, REF1 and REF2, which allow the output to be easily and accurately level shifted without the use of external circuitry. REF1 and REF2 are typically tied to an ADC ground and reference respectively. In this configuration the amplifier's output is conveniently level shifted to the center of the ADC input range.

If REF1 and REF2 are shorted to each other, they can function as the reference for the output voltage like a traditional instrumentation amplifier.

Parasitic resistance in series with REF1 and REF2 should be minimized to preserve CMRR and gain performance. It is also important to note that the drift in any circuitry used to drive REF1 or REF2 can result in an additional output drift term. Therefore, it may be important to consider the temperature accuracy of the circuitry used to drive the REF pin.

Gain Setting Resistor Connections

Each pre-amplifier gives a set of RG connection terminals which should be routed separately to the gain setting resistor. Doing this minimizes the impact which parasitic trace and lead resistance has on gain accuracy. When routing to the gain setting resistors, large loops should be avoided as they can couple noise into the amplifier.

Output Clamps

The CLHI and CLLO clamp pins limit the output voltage swing of the LT6372-0.2. CLHI and CLLO are typically tied to the ADC supply/reference and ADC ground respectively. In this case the ADC input is protected from being overdriven by the LT6372-0.2 which is likely running off a higher supply voltage.

When the CLLO is tied to 0V, attempts to drive the output below 0V will be clamped at –0.45V typically. When CLHI is tied to 5V, attempts to drive the output above 5V will be clamped at 5.45V typically.

CLHI and CLLO are high impedance inputs and do not conduct significant current during clamping. Rather, internal amplifier nodes are controlled by CLHI and CLLO to limit the output voltage.

In applications where clamping is not desired, CLLO should be tied to V^- and CLHI to V^+ to disable clamping.

Input and Output Offset Voltage

The offset voltage of the LT6372-0.2 has two main components: the input offset voltage due to the input amplifiers and the output offset due to the output amplifier. The total offset voltage referred to the input (RTI) is found by dividing the output offset by the programmed gain and adding it to the input offset voltage. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is:

Total input offset voltage (RTI) = $V_{OSI} + V_{OSO}/G$

Total output offset voltage (RTO) = $V_{OSI} \bullet G + V_{OSO}$

The preceding equations can also be used to calculate offset drift in a similar manner.

Output Offset Trimming

The LT6372-0.2 is laser trimmed for low offset voltage so that no external offset trimming is required for most applications. In the event that the offset voltage needs to be adjusted, the circuit in Figure 2 is an example of an optional offset adjustment circuit. The op amp buffer provides a low impedance signal to the REF pin in order to achieve the best CMRR and lowest gain error.

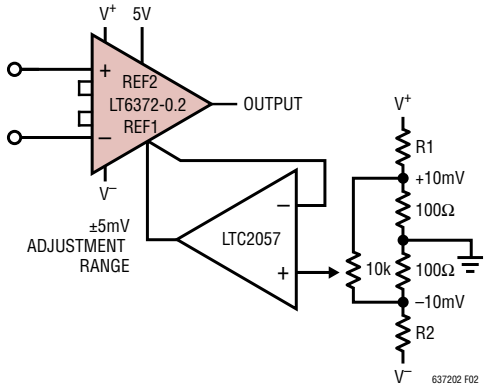


Figure 2. Optional Trimming of Output Offset Voltage

Thermocouple Effects

In order to achieve accuracy on the microvolt level, thermocouple effects must be considered. Any connection of dissimilar metals forms a thermoelectric junction and

APPLICATIONS INFORMATION

generates a small temperature-dependent voltage. Also known as the Seebeck Effect, these thermal EMFs can be the dominant error source in low-drift circuits.

Connectors, switches, relay contacts, sockets, resistors, and solder are all candidates for significant thermal EMF generation. Even junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C, which is comparable to the maximum input offset voltage drift specification of the LT6372-0.2. Figure 3 and Figure 4 illustrate the potential magnitude of these voltages and their sensitivity to temperature.

In order to minimize thermocouple-induced errors, attention must be given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input and R_G signal paths and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

Air currents can also lead to thermal gradients and cause significant noise in measurement systems. It is important to prevent airflow across sensitive circuits. Doing so will often reduce thermocouple noise substantially. Placing PCB input traces close together, and on an internal PCB layer, can help minimize temperature differentials resulting from air currents reacting with the input trace thermal surface area.

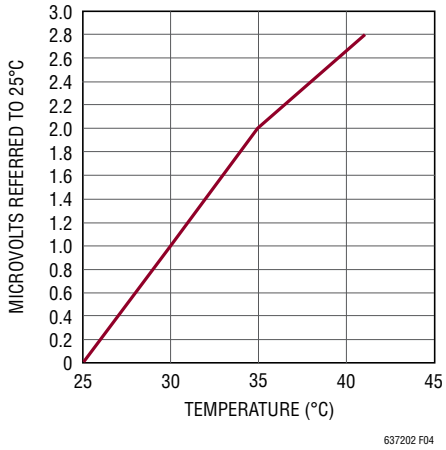


Figure 3. Thermal EMF Generated by Two Copper Wires From Different Manufacturers

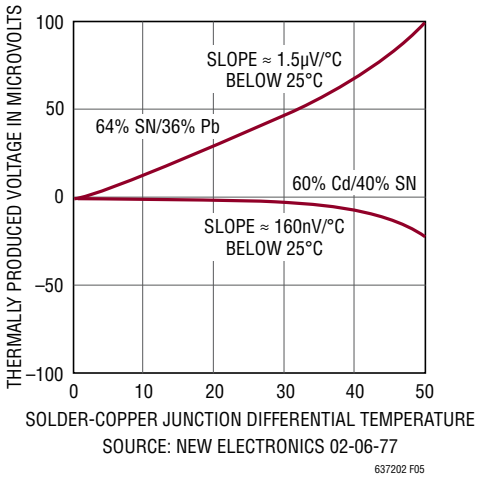


Figure 4. Solder-Copper Thermal EMFs

Reducing Board-Related Leakage Effects

Leakage currents can have a significant impact on system accuracy, particularly in high temperature and high voltage applications. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.

Leakage into the R_G pin conducts through the on-chip feedback resistor, creating an error at the output of the preamplifiers. This error is independent of gain and degrades accuracy the most at low gains. This leakage can be minimized by encircling the R_G connections with a guard-ring operated at a potential very close to that of the R_G pins. NIC pins adjacent to each R_G pin can be used to simplify the implementation of this guard-ring. These NIC pins do not provide any bias and have no internal connections. In some cases, the guard-ring can be connected to the input voltage which biases one diode drop below R_G.

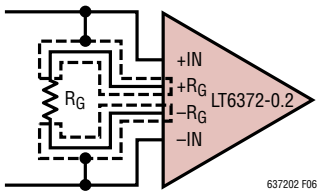


Figure 5. Guard-Rings Can Be Used to Minimize Leakage into the R_G Pins

Leakage into the input pins reacts with the source resistance, creating an error directly at the input. This leakage can be minimized by encircling the input connections with a guard-rings operated at a potential very close to that of the input pins. In some cases, the guard-ring can be connected to R_G which biases one diode above the input.

Figure 5 and Figure 6 show the force and sense R_G connections as a single R_G connection for simplicity.

For the lowest leakage, amplifiers can be used to drive the guard ring. These buffers must have very low input bias current since that will now be a leakage.

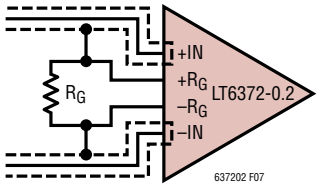


Figure 6. Guard-Rings Can Be Used to Minimize Leakage into the Input Pins

Input Bias Current Return Path

The low input bias current of the LT6372-0.2 (800pA max) and high input impedance (225GΩ) allow the use of high impedance sources without introducing additional offset voltage errors, even when the full common mode range is required. However, a path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path, the inputs will float to either rail and exceed the input common mode range of the LT6372-0.2, resulting in a saturated input amplifier. Figure 7 shows three examples of an input bias current path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both AC and DC common mode rejection and DC offset. The need for input resistors is eliminated if a center tap is present as shown in the third example.

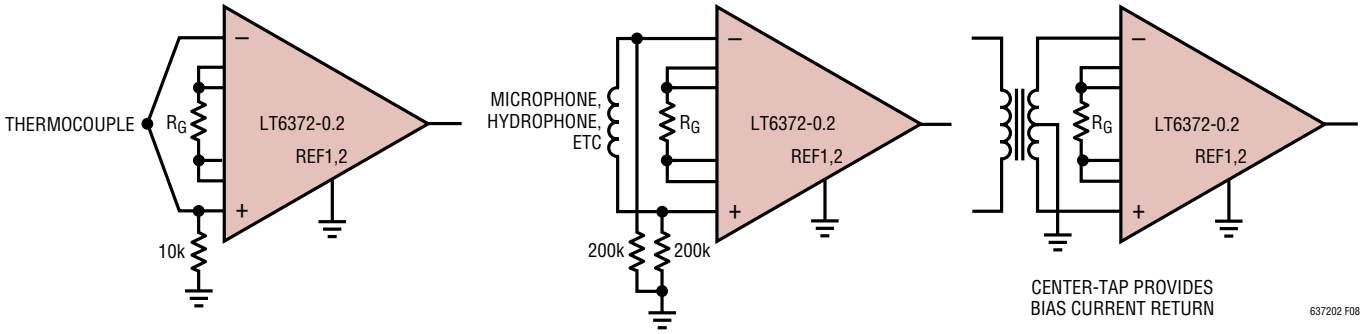


Figure 7. Providing an Input Common Mode Current Path

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Input Protection

Additional input protection can be achieved by adding external resistors in series with each input. If low value resistors are needed, a clamp diode from the positive supply to each input will help improve robustness. A 2N4394 drain/source to gate is a good low leakage diode which can be used as shown in Figure 8. Robust input resistors should be chosen, such as carbon composite or bulk metal foil. Metal film and carbon film should not be used because of their poor performance.

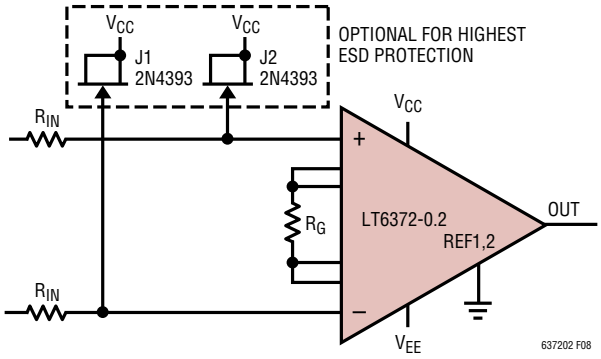

Figure 8. Input Protection

Maintaining AC CMRR

To achieve optimum AC CMRR, it is important to balance the capacitance on the R_G gain setting pins. Furthermore, if the source resistance on each input is not equal, adding an additional resistance to one input to improve input source resistance matching will improve AC CMRR.

RFI Reduction/Internal RFI Filter

In many industrial and data acquisition applications, the LT6372-0.2 will be used to amplify small signals accurately in the presence of large common mode voltages or high levels of noise. Typically, the sources of these very small signals (on the order of microvolts or millivolts) are sensors that can be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry using shielded or unshielded twisted-pair cabling, the cabling may act as an antenna, conveying very high frequency interference directly into the input stage of the LT6372-0.2.

The amplitude and frequency of the interference can have an adverse effect on an instrumentation amplifier's input stage by causing any unwanted DC shift in the amplifier's input offset voltage. This well known effect is called RFI rectification and is produced when out-of-band interference is coupled (inductively, capacitively or via radiation) and rectified by the instrumentation amplifier's input transistors. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled into the circuit, an out-of-band error signal appears in series with the instrumentation amplifier's inputs.

To help minimize this effect, the LT6372-0.2 has 50MHz on-chip RFI filters to help attenuate high frequencies before they can interact with its input transistors. These on-chip filters are well matched due to their monolithic construction, which helps minimize any degradation in AC CMRR. To reduce the effect of these out-of-band signals on the input offset voltage of the LT6372-0.2 further, an additional external low-pass filter can be used at the inputs. The filter should be located very close to the input pins of the circuit. An effective filter configuration is illustrated in Figure 9, where three capacitors have been added to the inputs of the LT6372-0.2.

The filter limits the input signal according to the following relationship:

$$\text{FilterFreq}_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$\text{FilterFreq}_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in $R \times C_C$ degrades the LT6372-0.2 CMRR. To avoid inadvertently reducing CMRR-bandwidth performance, make sure that C_C is at least one magnitude smaller than C_D.The effect of mismatched C_Cs is reduced with a larger C_D:C_C ratio.

APPLICATIONS INFORMATION

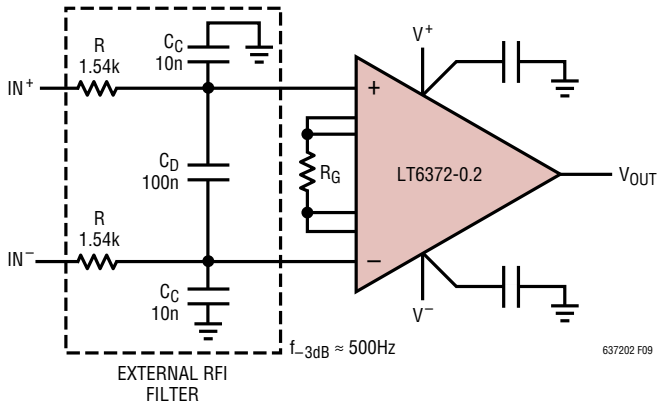

Figure 9. Adding a Simple External RC Filter at the Inputs to an Instrumentation Amplifier Is Effective in Further Reducing Rectification of High Frequency Out-Of-Band Signals

To avoid any possibility of common mode to differential mode signal conversion, match the common mode low-pass filter on each input to 1% or better. Here are the steps to help determine appropriate values for the filter:

1. Pick R and C_D to have a low pass pole at least 10x higher than the highest signal of interest (e.g. 500Hz for a 50Hz signal) using:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$= \frac{1}{2\pi R(2C_D + 0.1C_D)}$$

$$= \frac{1}{4.2\pi RC_D}$$

2. Select $C_C = C_D/10$.

If implemented this way, the common-mode pole frequency is placed about 20x higher than the differential pole frequency. Here are the differential and common-mode low pass pole frequencies for the values shown in Figure 9:

$FilterFreq_{DIFF}$ = 500Hz

$FilterFreq_{CM}$ = 10kHz

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Benefits when using LT6372-0.2 as an ADC Driver

The LT6372-0.2 incorporates several features which enable better interface to ADCs compared to traditional instrumentation amplifiers. Often, larger signals need to be attenuated to match the input range of an ADC. Additionally, a level shift is often required to center the amplifier's output to the ADC's input range. Figure 10 shows the LT6372-0.2 performing both these functions while maintaining high input impedance and providing protective clamping to the ADC's input.

Consider the alternative circuit in Figure 11, which shows a traditional instrumentation amplifier with a handful of additional components to perform the attenuation and level shifting functions. The added resistive dividers to attenuate the output and the ADC reference must have excellent initial tolerance and temperature coefficient. The operational amplifiers use to buffer the divided down reference and amplifier output must also have precision specifications over temperature. In order to protect the ADC in this configuration, U1 should run off the same supplies as the ADC. This requires that the input and output of U1 be rail-to-rail, limiting choices and likely giving up some input range on the ADC. These additional components take up space, draw power, add noise, increase cost and add complexity when compared to the LT6372-0.2 solution.

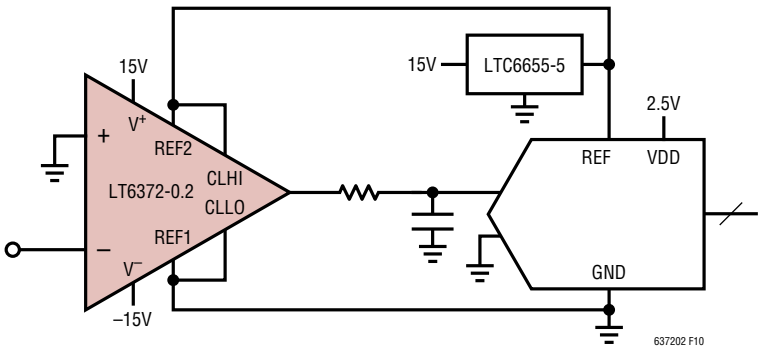


Figure 10. LT6372-0.2 Integrated ADC Driving Solution

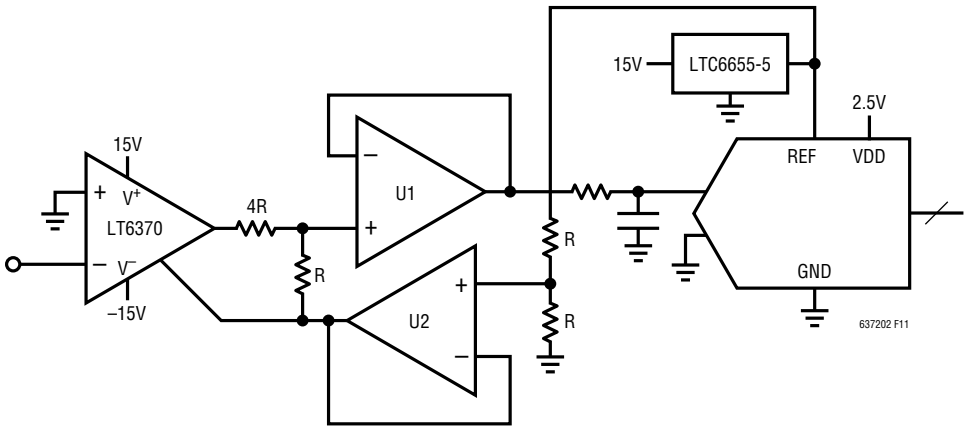
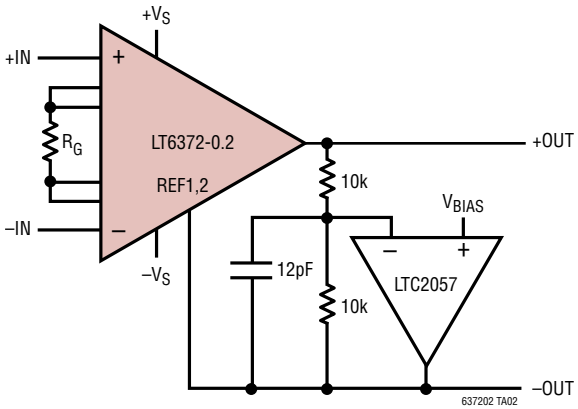


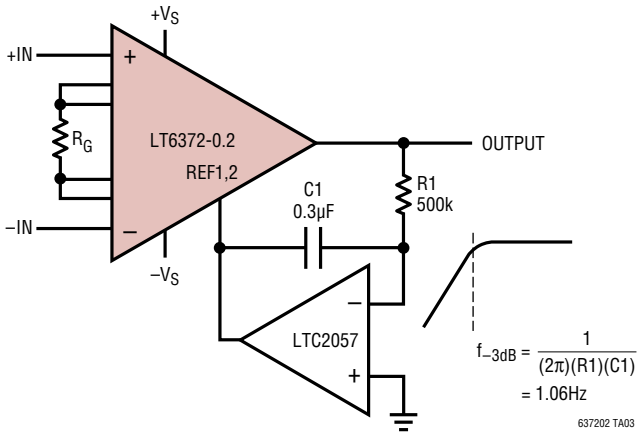
Figure 11. Alternative IA-ADC Interfacing Circuit

TYPICAL APPLICATIONS

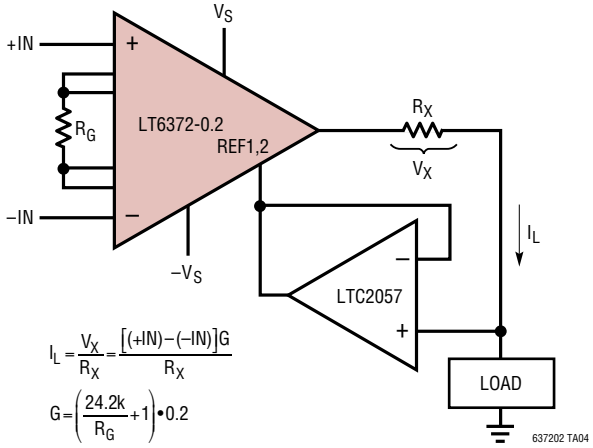
Differential Output Instrumentation Amplifier



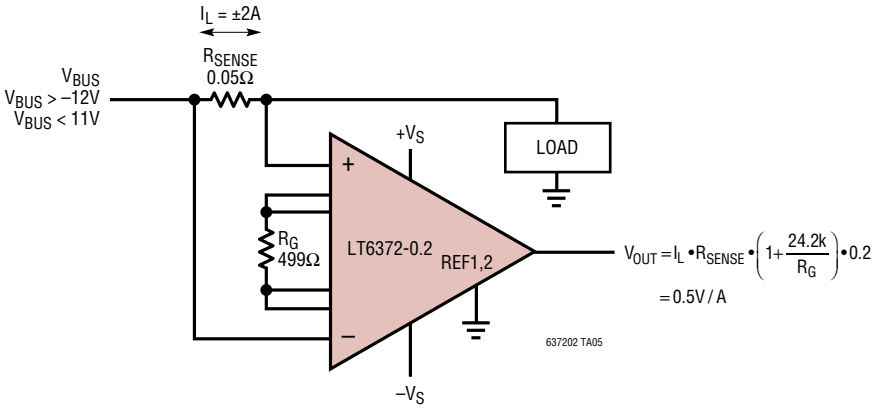
AC Coupled Instrumentation Amplifier



Precision Voltage-to-Current Converter

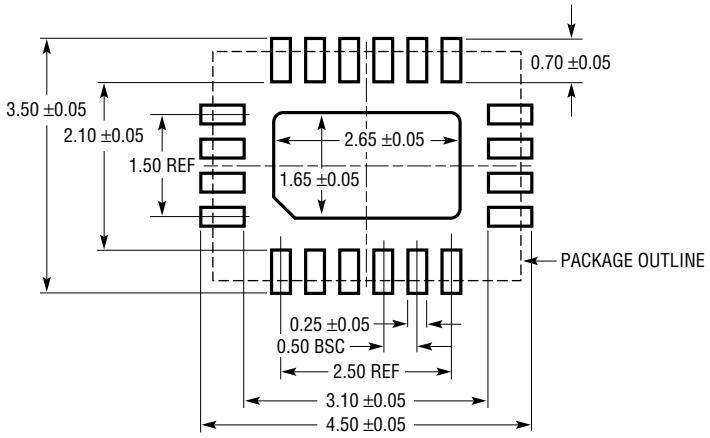


High Side, Bidirectional Current Sense

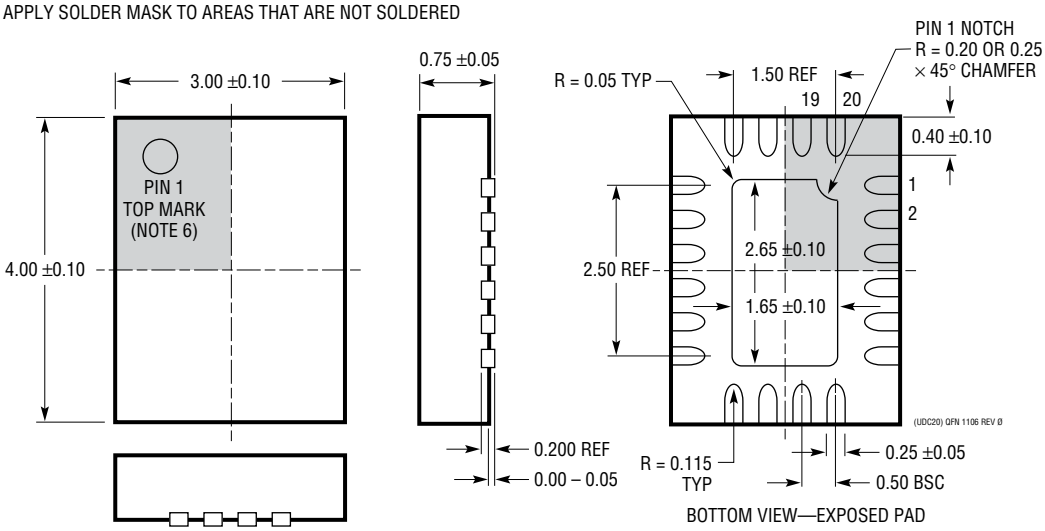


PACKAGE DESCRIPTION

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

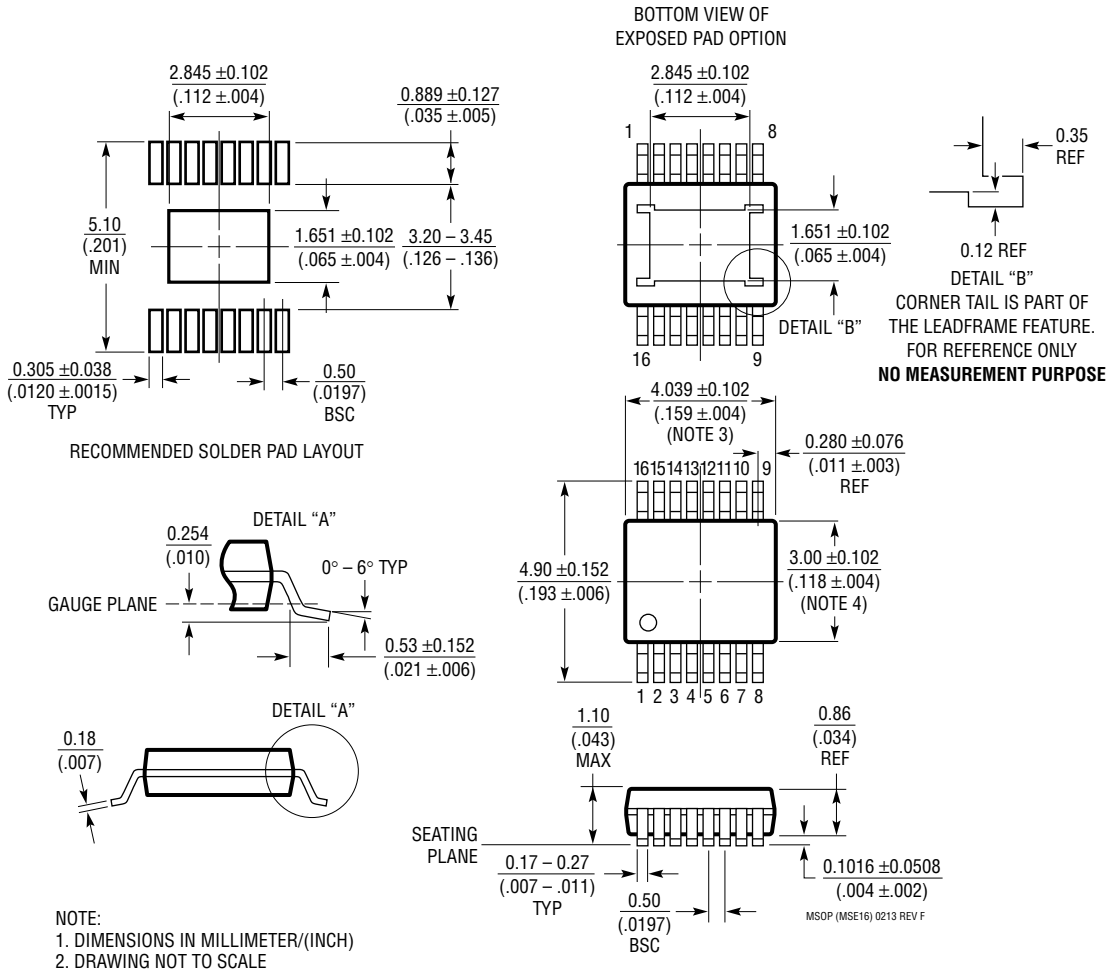


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

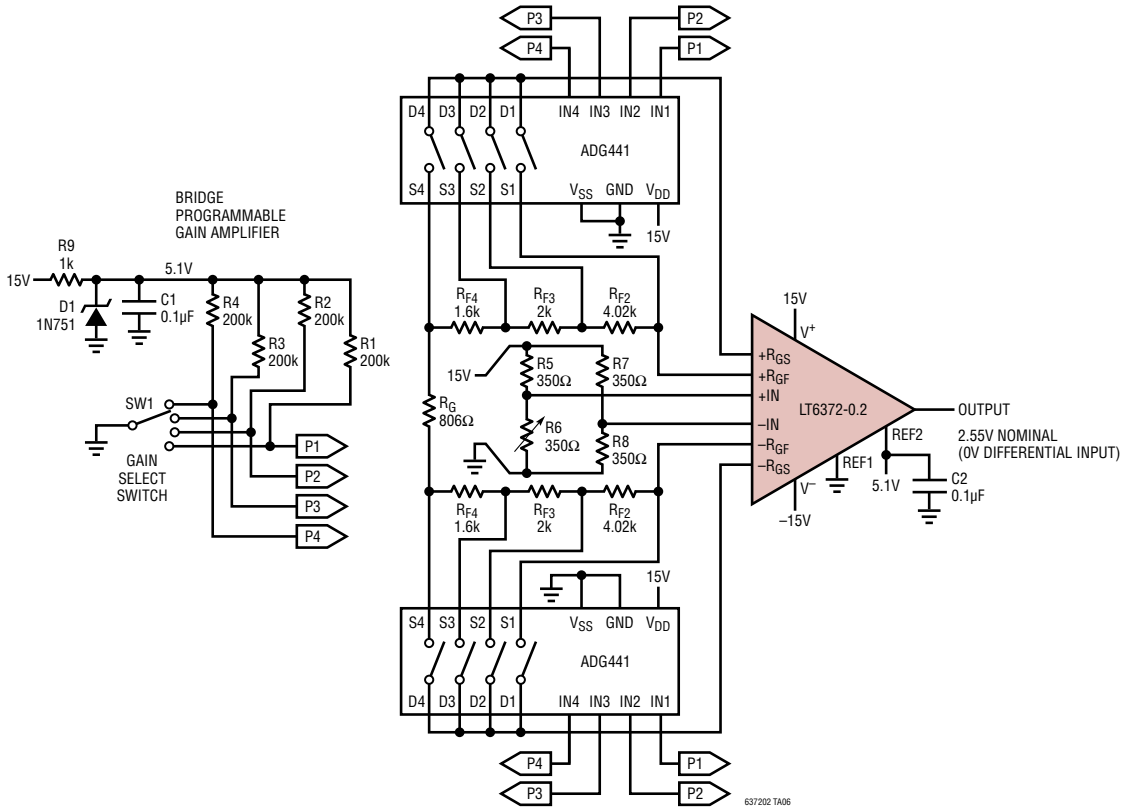
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

Programmable Gain Amplifier with Gains of 0.5V/V, 1V/V, 2V/V and 10V/V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Instrumentation Amplifiers		
AD8429	Low Noise Instrumentation Amplifier	V_S = 36V, I_S = 6.7mA, V_{OS} = 50µV, BW = 15MHz, e_{ni} = 1nV/√Hz, e_{no} = 45nV/√Hz
LT6372-1	Low Drift Instrumentation Amplifier	LT6372-0.2 with Min Gain = 1V/V
LT6370	Low Drift Instrumentation Amplifier	V_S = 30V, I_S = 2.65mA, V_{OS} = 25µV, BW = 3.1MHz, e_{ni} = 7nV/√Hz, e_{no} = 65nV/√Hz
LTC1100	Zero-Drift Instrumentation Amplifier	V_S = 18V, I_S = 2.4mA, V_{OS} = 10µV, BW = 19kHz, 1.9µV_{P-P} DC to 10Hz
AD8421	Low Noise Instrumentation Amplifier	V_S = 36V, I_S = 2mA, V_{OS} = 25µV, BW = 10MHz, e_{ni} = 3nV/√Hz, e_{no} = 60nV/√Hz
AD8221	Low Power Instrumentation Amplifier	V_S = 36V, I_S = 900µA, V_{OS} = 25µV, BW = 825kHz, e_{ni} = 8nV/√Hz, e_{no} = 75nV/√Hz
LT1167	Instrumentation Amplifier	V_S = 36V, I_S = 900µA, V_{OS} = 40µV, BW = 1MHz, e_{ni} = 7.5nV/√Hz, e_{no} = 67nV/√Hz
AD620	Low Power Instrumentation Amplifier	V_S = 36V, I_S = 900µA, V_{OS} = 50µV, BW = 1MHz, e_{ni} = 9nV/√Hz, e_{no} = 72nV/√Hz
LTC6800	RRIO Instrumentation Amplifier	V_S = 5.5V, I_S = 800µA, V_{OS} = 100µV, BW = 200kHz, 2.5µV_{P-P} DC to 10Hz
LTC2053	Zero-Drift Instrumentation Amplifier	V_S = 11V, I_S = 750µA, V_{OS} = 10µV, BW = 200kHz, 2.5µV_{P-P} DC to 10Hz
LT1168	Low Power Instrumentation Amplifier	V_S = 36V, I_S = 350µA, V_{OS} = 40µV, BW = 400kHz, e_{ni} = 10nV/√Hz, e_{no} = 165nV/√Hz
Operational Amplifiers		
LTC2057	40V Zero Drift Op Amp	V_{OS} = 4µV, Drift = 15nV/°C, I_B = 200pA, I_S = 900µA
Analog to Digital Converters		
LTC2389-16	16-Bit SAR ADC	2.5Msps, 96dB SNR, 162.5mW
LTC2367-16	16-Bit SAR ADC	500ksps, 94.7dB SNR, 6.8mW