

EFM32 Gecko Family

EFM32JG12 Family Data Sheet



The EFM32 Gecko MCUs are the world's most energy-friendly microcontrollers.

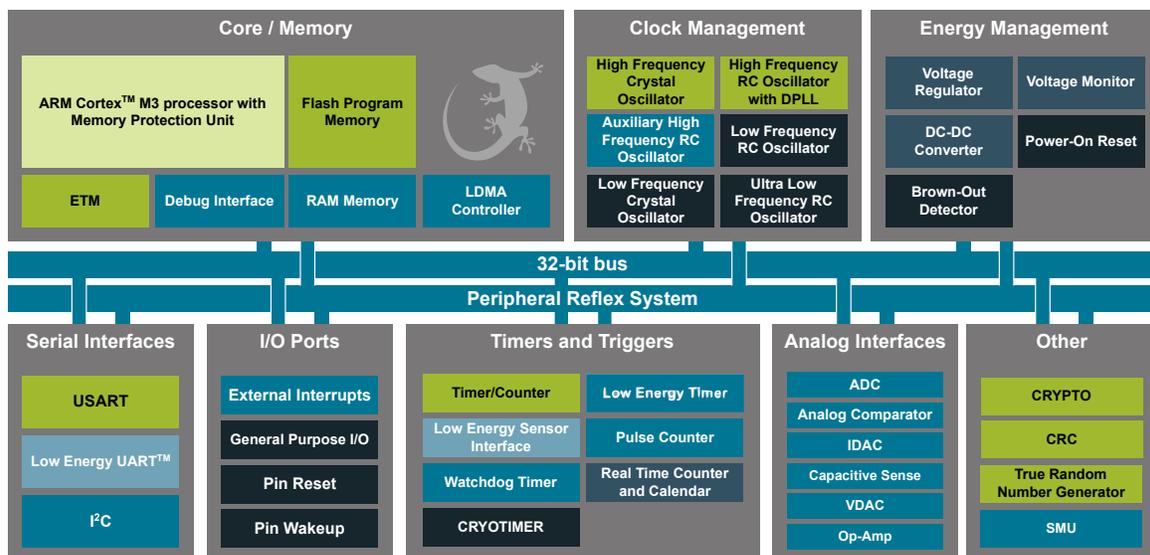
EFM32JG12 features a powerful 32-bit ARM[®] Cortex[®]-M3 and a wide selection of peripherals, including a unique cryptographic hardware engine and Security Management Unit, True Random Number Generator, and robust capacitive touch sense unit. These features, combined with ultra-low current active and sleep modes, make EFM32JG12 microcontrollers well suited for any battery-powered application, as well as other systems requiring high performance and low energy consumption.

Example applications:

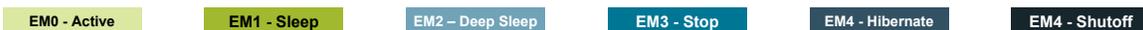
- IoT devices and sensors
- Health and fitness
- Smart accessories
- Home automation and security
- Industrial and factory automation

ENERGY FRIENDLY FEATURES

- ARM Cortex-M3 at 40 MHz
- Ultra low energy operation:
 - 0.39 μ A EM4H Hibernate current
 - 1.5 μ A EM2 Deep Sleep current (RTCC running with state and RAM retention)
 - 64 μ A/MHz EM0 Active current
- Hardware cryptographic engine (AES, ECC, and SHA) and TRNG
- Security Management Unit (SMU)
- Autonomous low energy sensor interface (LESENSE)
- Rich analog features including ADC, VDAC, OPAMPs, and capacitive sense
- Integrated DC-DC converter
- 5 V tolerant I/O



Lowest power mode with peripheral operational:



1. Feature List

The EFM32JG12 highlighted features are listed below.

- **ARM Cortex-M3 CPU platform**
 - High performance 32-bit processor @ up to 40 MHz
 - Memory Protection Unit
 - Wake-up Interrupt Controller
- **Flexible Energy Management System**
 - 64 μ A/MHz in Active Mode (EM0)
 - 2.1 μ A EM2 Deep Sleep current (256 kB RAM retention and RTCC running from LFXO)
 - 1.5 μ A EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
 - 1.81 μ A EM3 Stop current (State and 256 kB RAM retention, CRYOTIMER running from ULFRCO)
 - 0.39 μ A EM4H Hibernate Mode (128 byte RAM retention)
- **Up to 1024 kB flash program memory**
 - Dual-bank with read-while-write support
- **Up to 256 kB RAM data memory**
- **Up to 65 General Purpose I/O Pins**
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - Asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- **Hardware Cryptography**
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
 - True random number generator (TRNG)
- **Security Management Unit (SMU)**
 - Fine-grained access control for on-chip peripherals
- **Timers/Counters**
 - 2 \times 16-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels
 - 2 \times 32-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels
 - 1 \times 32-bit Real Time Counter and Calendar
 - 1 \times 32-bit Ultra Low Energy CRYOTIMER for periodic wake-up from any Energy Mode
 - 16-bit Low Energy Timer for waveform generation
 - 3 \times 16-bit Pulse Counter with asynchronous operation
 - 2 \times Watchdog Timer with dedicated RC oscillator
- **8 Channel DMA Controller**
- **12 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Communication Interfaces**
 - 4 \times Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - Triple buffered full/half-duplex operation with flow control
 - Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - 2 \times I²C Interface with SMBus support
 - Address recognition in EM3 Stop Mode
- **Ultra Low-Power Precision Analog Peripherals**
 - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
 - 2 \times Analog Comparator (ACMP)
 - 2 \times 12-bit 500 ksps Digital to Analog Converter (VDAC)
 - 3 \times Operational Amplifier (OPAMP)
 - Digital to Analog Current Converter (IDAC)
 - Multi-channel Capacitive Sense Interface (CSEN)
 - Up to 54 pins connected to analog channels (APORT) shared between analog peripherals
- **Low-Energy Sensor Interface (LESENSE)**
 - Autonomous sensor monitoring in deep sleep mode
 - Wide range of supported sensors, including LC sensors and capacitive touch switches
 - Up to 16 channels
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
 - 2-pin Serial Wire Debug interface
 - 1-pin Serial Wire Viewer
 - JTAG (programming only)
 - Embedded Trace Macrocell (ETM)
- **Wide Operating Range**
 - 1.8 V to 3.8 V single power supply
 - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
 - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
 - 7 mm \times 7 mm QFN48
 - 7 mm \times 7 mm BGA125
- **Pre-Programmed UART Bootloader**
- **Full Software Support**
 - CMSIS register definitions
 - Low-power Hardware Abstraction Layer (HAL)
 - Portable software components
 - Third-party middleware
 - Free and available example code

2. Ordering Information

Table 2.1. Ordering Information

| Ordering Code | Flash (kB) | RAM (kB) | DC-DC Converter | GPIO | Package | Temp Range |
|---------------------------|------------|----------|-----------------|------|---------|---------------|
| EFM32JG12B500F1024GL125-C | 1024 | 256 | Yes | 65 | BGA125 | -40 to +85°C |
| EFM32JG12B500F1024IL125-C | 1024 | 256 | Yes | 65 | BGA125 | -40 to +125°C |
| EFM32JG12B500F1024GM48-C | 1024 | 256 | Yes | 33 | QFN48 | -40 to +85°C |
| EFM32JG12B500F1024IM48-C | 1024 | 256 | Yes | 33 | QFN48 | -40 to +125°C |

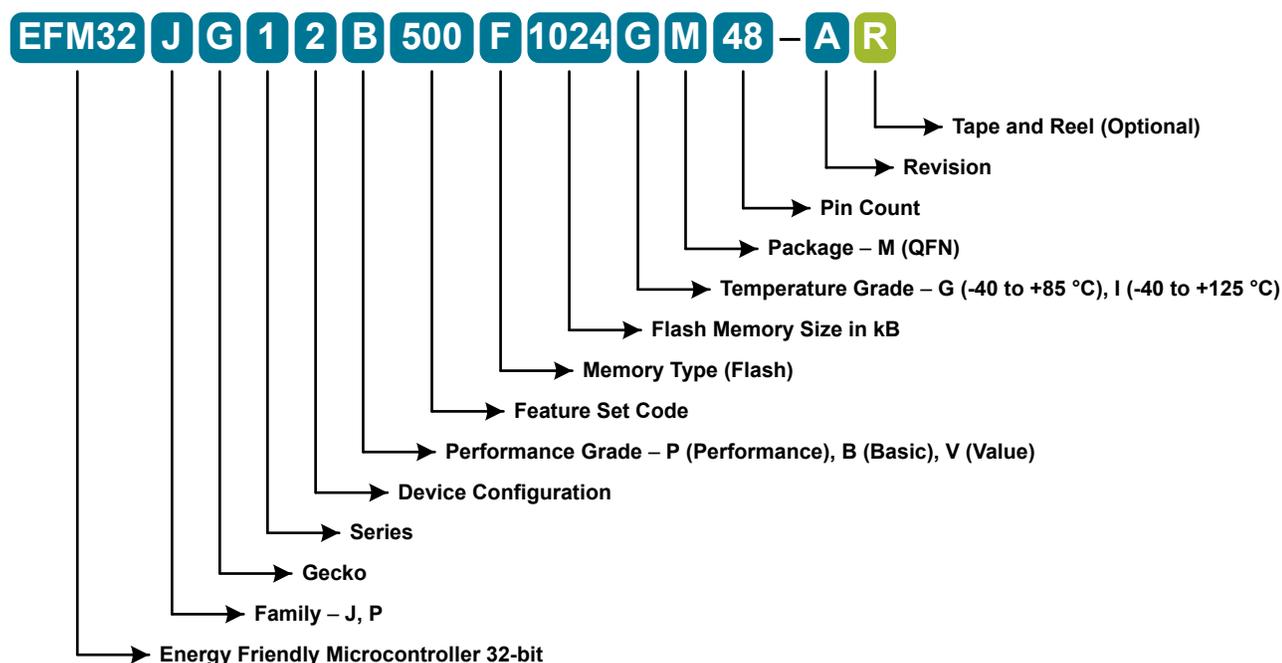


Figure 2.1. Ordering Code Key

Table of Contents

| | |
|---|----------|
| 1. Feature List | 2 |
| 2. Ordering Information | 3 |
| 3. System Overview | 7 |
| 3.1 Introduction | 7 |
| 3.2 Power | 8 |
| 3.2.1 Energy Management Unit (EMU) | 8 |
| 3.2.2 DC-DC Converter | 8 |
| 3.2.3 Power Domains | 8 |
| 3.3 General Purpose Input/Output (GPIO) | 9 |
| 3.4 Clocking | 9 |
| 3.4.1 Clock Management Unit (CMU) | 9 |
| 3.4.2 Internal and External Oscillators | 9 |
| 3.5 Counters/Timers and PWM | 9 |
| 3.5.1 Timer/Counter (TIMER) | 9 |
| 3.5.2 Wide Timer/Counter (WTIMER) | 9 |
| 3.5.3 Real Time Counter and Calendar (RTCC) | 9 |
| 3.5.4 Low Energy Timer (LETIMER) | 10 |
| 3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER) | 10 |
| 3.5.6 Pulse Counter (PCNT) | 10 |
| 3.5.7 Watchdog Timer (WDOG) | 10 |
| 3.6 Communications and Other Digital Peripherals | 10 |
| 3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) | 10 |
| 3.6.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART) | 10 |
| 3.6.3 Inter-Integrated Circuit Interface (I ² C) | 10 |
| 3.6.4 Peripheral Reflex System (PRS) | 10 |
| 3.6.5 Low Energy Sensor Interface (LESENSE) | 11 |
| 3.7 Security Features | 11 |
| 3.7.1 General Purpose Cyclic Redundancy Check (GPCRC) | 11 |
| 3.7.2 Crypto Accelerator (CRYPTO) | 11 |
| 3.7.3 True Random Number Generator (TRNG) | 11 |
| 3.7.4 Security Management Unit (SMU) | 11 |
| 3.8 Analog | 11 |
| 3.8.1 Analog Port (APORT) | 11 |
| 3.8.2 Analog Comparator (ACMP) | 11 |
| 3.8.3 Analog to Digital Converter (ADC) | 12 |
| 3.8.4 Capacitive Sense (CSEN) | 12 |
| 3.8.5 Digital to Analog Current Converter (IDAC) | 12 |
| 3.8.6 Digital to Analog Converter (VDAC) | 12 |
| 3.8.7 Operational Amplifiers | 12 |
| 3.9 Reset Management Unit (RMU) | 12 |
| 3.10 Core and Memory | 12 |
| 3.10.1 Processor Core | 12 |

| | | |
|-----------|---|-------------|
| 3.10.2 | Memory System Controller (MSC) | .13 |
| 3.10.3 | Linked Direct Memory Access Controller (LDMA) | .13 |
| 3.10.4 | Bootloader | .13 |
| 3.11 | Memory Map | .14 |
| 3.12 | Configuration Summary | .16 |
| 4. | Electrical Specifications | .17 |
| 4.1 | Electrical Characteristics | .17 |
| 4.1.1 | Absolute Maximum Ratings | .17 |
| 4.1.2 | Operating Conditions | .18 |
| 4.1.3 | Thermal Characteristics | .20 |
| 4.1.4 | DC-DC Converter | .21 |
| 4.1.5 | Current Consumption | .23 |
| 4.1.6 | Wake Up Times | .28 |
| 4.1.7 | Brown Out Detector (BOD) | .29 |
| 4.1.8 | Oscillators | .30 |
| 4.1.9 | Flash Memory Characteristics | .34 |
| 4.1.10 | General-Purpose I/O (GPIO) | .35 |
| 4.1.11 | Voltage Monitor (VMON) | .37 |
| 4.1.12 | Analog to Digital Converter (ADC) | .38 |
| 4.1.13 | Analog Comparator (ACMP) | .40 |
| 4.1.14 | Digital to Analog Converter (VDAC) | .42 |
| 4.1.15 | Current Digital to Analog Converter (IDAC) | .45 |
| 4.1.16 | Capacitive Sense (CSEN) | .47 |
| 4.1.17 | Operational Amplifier (OPAMP) | .49 |
| 4.1.18 | Pulse Counter (PCNT) | .52 |
| 4.1.19 | Analog Port (APORT) | .52 |
| 4.1.20 | I2C | .53 |
| 4.1.21 | USART SPI | .56 |
| 4.2 | Typical Performance Curves | .58 |
| 4.2.1 | Supply Current | .59 |
| 4.2.2 | DC-DC Converter | .64 |
| 5. | Typical Connection Diagrams | .66 |
| 5.1 | Power | .66 |
| 5.2 | Other Connections | .66 |
| 6. | Pin Definitions | .67 |
| 6.1 | EFM32JG12B5xx in BGA125 Device Pinout | .67 |
| 6.2 | EFM32JG12B5xx in QFN48 Device Pinout | .71 |
| 6.3 | GPIO Functionality Table | .73 |
| 6.4 | Alternate Functionality Overview | .92 |
| 6.5 | Analog Port (APORT) Client Maps | .104 |
| 7. | BGA125 Package Specifications | .113 |
| 7.1 | BGA125 Package Dimensions | .113 |

7.2 BGA125 PCB Land Pattern 115

7.3 BGA125 Package Marking 117

8. QFN48 Package Specifications. 118

8.1 QFN48 Package Dimensions 118

8.2 QFN48 PCB Land Pattern 120

8.3 QFN48 Package Marking 122

9. Revision History 123

3. System Overview

3.1 Introduction

The EFM32JG12 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the EFM32JG12 Reference Manual.

A block diagram of the EFM32JG12 family is shown in [Figure 3.1 Detailed EFM32JG12 Block Diagram on page 7](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

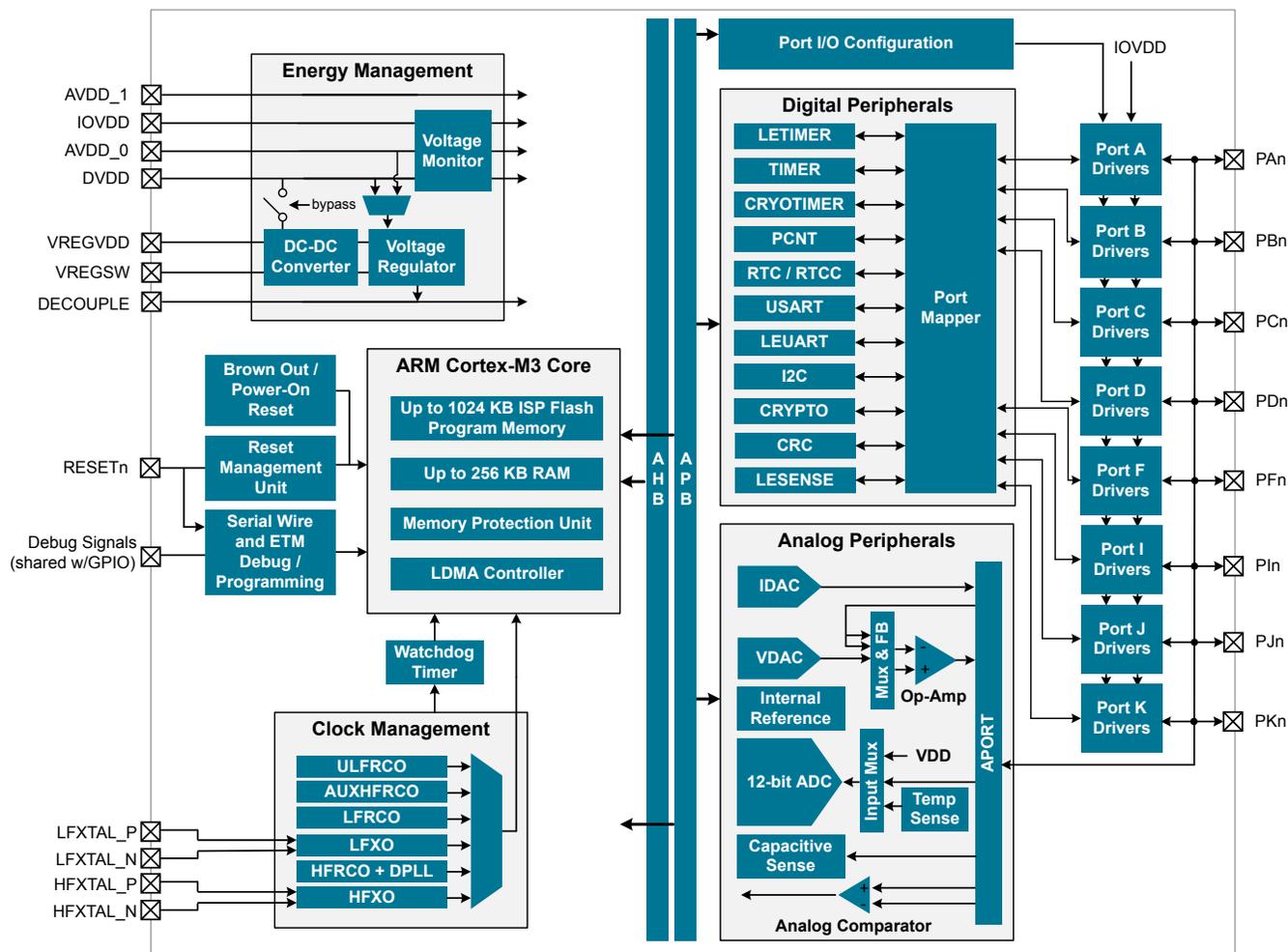


Figure 3.1. Detailed EFM32JG12 Block Diagram

3.2 Power

The EFM32JG12 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32JG12 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 Power Domains

The EFM32JG12 has two peripheral power domains for operation in EM2 and lower. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

Table 3.1. Peripheral Power Subdomains

| Peripheral Power Domain 1 | Peripheral Power Domain 2 |
|---------------------------|---------------------------|
| ACMP0 | ACMP1 |
| PCNT0 | PCNT1 |
| ADC0 | PCNT2 |
| LETIMER0 | CSEN |
| LESENSE | DAC0 |
| APOINT | LEUART0 |
| - | I2C0 |
| - | I2C1 |
| - | IDAC |

3.3 General Purpose Input/Output (GPIO)

EFM32JG12 has up to 65 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32JG12. Individual enabling and disabling of clocks to all peripherals is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32JG12 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit `TIMER_0` only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit `WTIMER_0` only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The peripheral may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O interface. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.6.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.3 Inter-Integrated Circuit Interface (I²C)

The I²C interface enables communication between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C peripheral allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripherals without software involvement. Peripherals producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals, which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.6.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.7 Security Features

3.7.1 General Purpose Cyclic Redundancy Check (GPCRC)

The GPCRC block implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFM32JG12 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO peripheral allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

Note: TRNG operation is only supported at VSCALE2. TRNG cannot be used at VSCALE0.

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog peripherals on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN peripheral is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN peripheral uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The peripheral can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Current Converter (IDAC)

The IDAC can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 kbps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC peripheral or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32JG12. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M3 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 1024 kB flash program memory
 - Dual-bank memory with read-while-write support
- Up to 256 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire or 4-pin JTAG debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the **[Documentation]** area.

3.11 Memory Map

The EFM32JG12 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

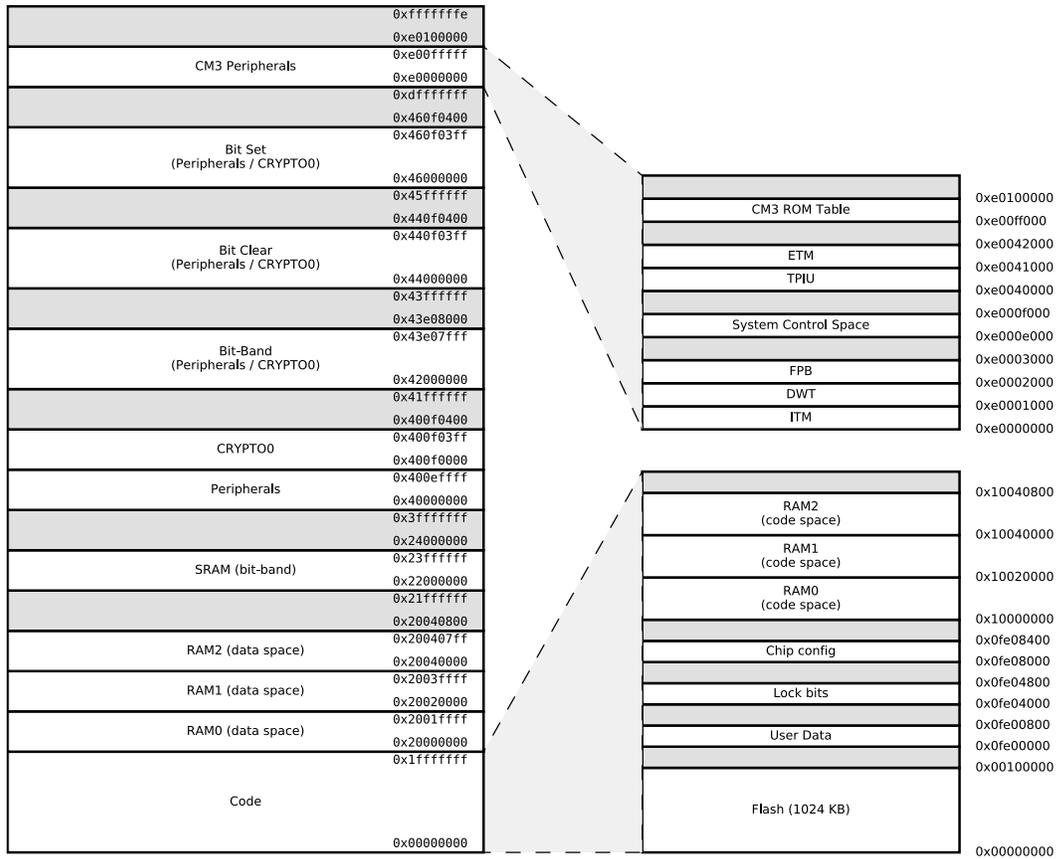


Figure 3.2. EFM32JG12 Memory Map — Core Peripherals and Code Space

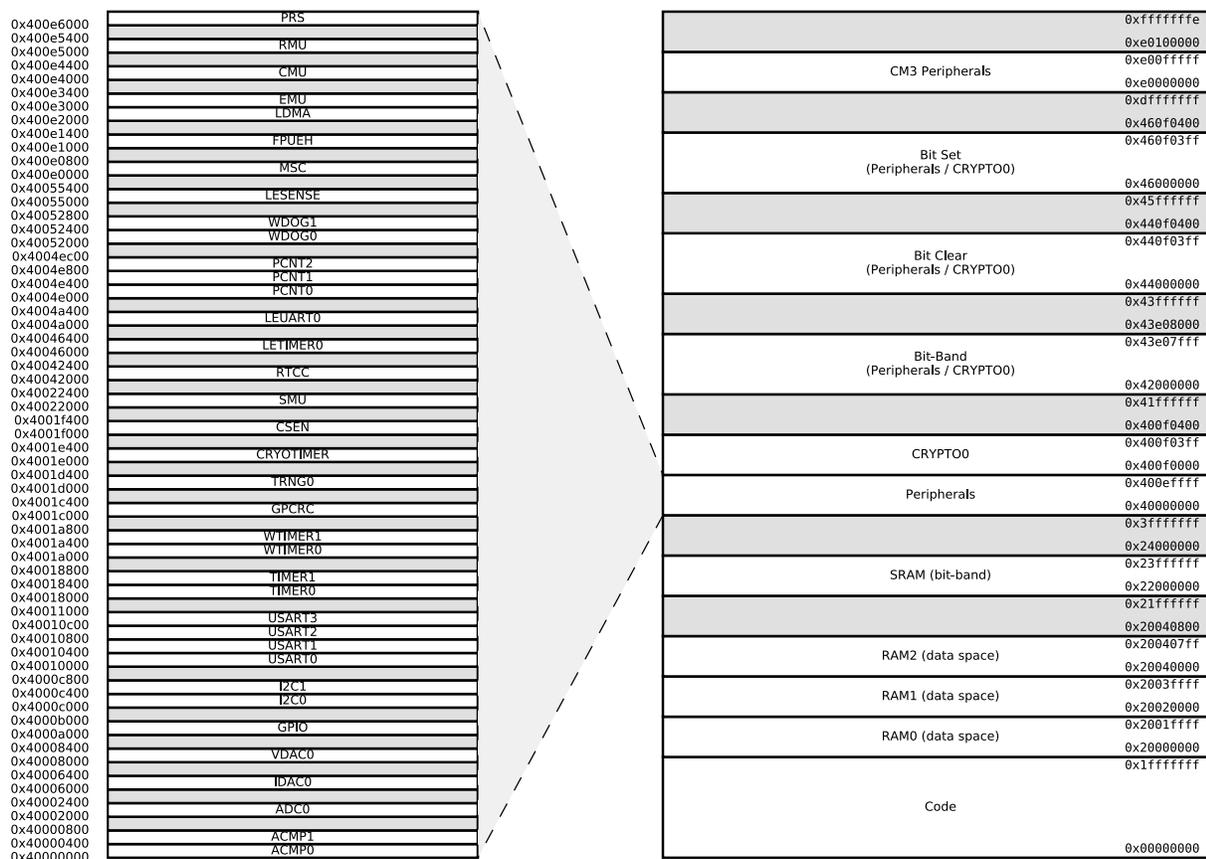


Figure 3.3. EFM32JG12 Memory Map — Peripherals

3.12 Configuration Summary

The features of the EFM32JG12 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

| Module | Configuration | Pin Connections |
|---------|-------------------------------|---------------------------------|
| USART0 | IrDA SmartCard | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | I ² S SmartCard | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | IrDA SmartCard | US2_TX, US2_RX, US2_CLK, US2_CS |
| USART3 | I ² S SmartCard | US3_TX, US3_RX, US3_CLK, US3_CS |
| TIMER0 | with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | - | TIM1_CC[3:0] |
| WTIMER0 | with DTI | WTIM0_CC[2:0], WTIM0_CDTI[2:0] |
| WTIMER1 | - | WTIM1_CC[3:0] |

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}=25\text{ }^{\circ}\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to [4.1.2.1 General Operating Conditions](#) for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.1. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|-----------------|--|------|-----|--------------------------|--------------------|
| Storage temperature range | T_{STG} | | -50 | — | 150 | $^{\circ}\text{C}$ |
| Voltage on any supply pin | V_{DDMAX} | | -0.3 | — | 3.8 | V |
| Voltage ramp rate on any supply pin | $V_{DDRAMPMAX}$ | | — | — | 1 | V / μs |
| DC voltage on any GPIO pin | V_{DIGPIN} | 5V tolerant GPIO pins ^{1 2 3} | -0.3 | — | Min of 5.25 and IOVDD +2 | V |
| | | Standard GPIO pins | -0.3 | — | IOVDD+0.3 | V |
| Voltage on HFXO pins | $V_{HFXOPIN}$ | | -0.3 | — | 1.4 | V |
| Total current into VDD power lines | I_{VDDMAX} | Source | — | — | 200 | mA |
| Total current into VSS ground lines | I_{VSSMAX} | Sink | — | — | 200 | mA |
| Current per I/O pin | I_{IOMAX} | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | $I_{IOALLMAX}$ | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |
| Junction temperature | T_J | -G grade devices | -40 | — | 105 | $^{\circ}\text{C}$ |
| | | -I grade devices | -40 | — | 125 | $^{\circ}\text{C}$ |

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD \leq AVDD
- IOVDD \leq AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------------------|---|------|-----|----------------------|------|
| Operating ambient temperature range ⁶ | T _A | -G temperature grade | -40 | 25 | 85 | °C |
| | | -I temperature grade | -40 | 25 | 125 | °C |
| AVDD supply voltage ² | V _{AVDD} | | 1.8 | 3.3 | 3.8 | V |
| VREGVDD operating supply voltage ^{2 1} | V _{VREGVDD} | DCDC in regulation | 2.4 | 3.3 | 3.8 | V |
| | | DCDC in bypass, 50mA load | 1.8 | 3.3 | 3.8 | V |
| | | DCDC not in use. DVDD externally shorted to VREGVDD | 1.8 | 3.3 | 3.8 | V |
| VREGVDD current | I _{VREGVDD} | DCDC in bypass, T ≤ 85 °C | — | — | 200 | mA |
| | | DCDC in bypass, T > 85 °C | — | — | 100 | mA |
| DVDD operating supply voltage | V _{DVDD} | | 1.62 | — | V _{VREGVDD} | V |
| IOVDD operating supply voltage | V _{IOVDD} | All IOVDD pins ⁵ | 1.62 | — | V _{VREGVDD} | V |
| DECOUPLE output capacitor ^{3 4} | C _{DECOUPLE} | | 0.75 | 1.0 | 2.75 | μF |
| Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD) ² | dV _{DD} | | — | — | 0.1 | V |
| HFCORECLK frequency | f _{CORE} | VSCALE2, MODE = WS1 | — | — | 40 | MHz |
| | | VSCALE0, MODE = WS0 | — | — | 20 | MHz |
| HFCLK frequency | f _{HFCLK} | VSCALE2 | — | — | 40 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |
| HFSRCCLK frequency | f _{HFSRCCLK} | VSCALE2 | — | — | 40 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as V_{DVDD_min} + I_{LOAD} * R_{BYP_max}.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - (THETA_{JA} x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and THETA_{JA}.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------|---------------------|--|-----|------|-----|------|
| Thermal Resistance | THETA _{JA} | QFN48 Package, 2-Layer PCB, Air velocity = 0 m/s | — | 75.7 | — | °C/W |
| | | QFN48 Package, 2-Layer PCB, Air velocity = 1 m/s | — | 61.5 | — | °C/W |
| | | QFN48 Package, 2-Layer PCB, Air velocity = 2 m/s | — | 55.4 | — | °C/W |
| | | QFN48 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 30.2 | — | °C/W |
| | | QFN48 Package, 4-Layer PCB, Air velocity = 1 m/s | — | 26.3 | — | °C/W |
| | | QFN48 Package, 4-Layer PCB, Air velocity = 2 m/s | — | 24.9 | — | °C/W |
| | | BGA125 Package, 2-Layer PCB, Air velocity = 0 m/s | — | 90.7 | — | °C/W |
| | | BGA125 Package, 2-Layer PCB, Air velocity = 1 m/s | — | 73.7 | — | °C/W |
| | | BGA125 Package, 2-Layer PCB, Air velocity = 2 m/s | — | 66.4 | — | °C/W |
| | | BGA125 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 45 | — | °C/W |
| | | BGA125 Package, 4-Layer PCB, Air velocity = 1 m/s | — | 39.6 | — | °C/W |
| | | BGA125 Package, 4-Layer PCB, Air velocity = 2 m/s | — | 37.6 | — | °C/W |

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 μ H (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 μ F (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|--|------|-----|--------------------------|------------------|
| Input voltage range | V _{DCDC_I} | Bypass mode, I _{DCDC_LOAD} = 50 mA | 1.8 | — | V _{VREGVDD_MAX} | V |
| | | Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I _{DCDC_LOAD} = 10 mA | 2.4 | — | V _{VREGVDD_MAX} | V |
| | | Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 200 mA | 2.6 | — | V _{VREGVDD_MAX} | V |
| Output voltage programmable range ¹ | V _{DCDC_O} | | 1.8 | — | V _{VREGVDD} | V |
| Regulation DC accuracy | ACC _{DC} | Low Noise (LN) mode, 1.8 V target output | 1.7 | — | 1.9 | V |
| Regulation window ⁴ | WIN _{REG} | Low Power (LP) mode, LPCMPBIASEM _{xx} ³ = 0, 1.8 V target output, I _{DCDC_LOAD} \leq 75 μ A | 1.63 | — | 2.2 | V |
| | | Low Power (LP) mode, LPCMPBIASEM _{xx} ³ = 3, 1.8 V target output, I _{DCDC_LOAD} \leq 10 mA | 1.63 | — | 2.1 | V |
| Steady-state output ripple | V _R | | — | 3 | — | mV _{pp} |
| Output voltage under/overshoot | V _{OV} | CCM Mode (LNFORCECCM ³ = 1), Load changes between 0 mA and 100 mA | — | 25 | 60 | mV |
| | | DCM Mode (LNFORCECCM ³ = 0), Load changes between 0 mA and 10 mA | — | 45 | 90 | mV |
| | | Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode | — | 200 | — | mV |
| | | Undershoot during BYP/LP to LN CCM (LNFORCECCM ³ = 1) mode transitions compared to DC level in LN mode | — | 40 | — | mV |
| | | Undershoot during BYP/LP to LN DCM (LNFORCECCM ³ = 0) mode transitions compared to DC level in LN mode | — | 100 | — | mV |
| DC line regulation | V _{REG} | Input changes between V _{VREGVDD_MAX} and 2.4 V | — | 0.1 | — | % |
| DC load regulation | I _{REG} | Load changes between 0 mA and 100 mA in CCM mode | — | 0.1 | — | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------|---|-----|-----|-----|------|
| Max load current | I _{LOAD_MAX} | Low noise (LN) mode, Heavy Drive ² , T ≤ 85 °C | — | — | 200 | mA |
| | | Low noise (LN) mode, Heavy Drive ² , T > 85 °C | — | — | 100 | mA |
| | | Low noise (LN) mode, Medium Drive ² | — | — | 100 | mA |
| | | Low noise (LN) mode, Light Drive ² | — | — | 50 | mA |
| | | Low power (LP) mode, LPCMPBIASEMxx ³ = 0 | — | — | 75 | μA |
| | | Low power (LP) mode, LPCMPBIASEMxx ³ = 3 | — | — | 10 | mA |
| DCDC nominal output capacitor ⁵ | C _{DCDC} | 25% tolerance | 1 | 4.7 | 4.7 | μF |
| DCDC nominal output inductor | L _{DCDC} | 20% tolerance | 4.7 | 4.7 | 4.7 | μH |
| Resistance in Bypass mode | R _{BYP} | | — | 1.2 | 2.5 | Ω |

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VREGVDD}.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF. See Application Note AN0948 for details.

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.5. Current Consumption 3.3 V without DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|---|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled | I _{ACTIVE} | 38.4 MHz crystal, CPU running while loop from flash ¹ | — | 126 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 99 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 99 | 105 | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 124 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 102 | 108 | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 280 | 435 | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled | I _{ACTIVE_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 88 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 234 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | I _{EM1} | 38.4 MHz crystal ¹ | — | 76 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 50 | 54 | µA/MHz |
| | | 26 MHz HFRCO | — | 52 | 58 | µA/MHz |
| | | 1 MHz HFRCO | — | 230 | 400 | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled | I _{EM1_VS} | 19 MHz HFRCO | — | 47 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 193 | — | µA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled | I _{EM2_VS} | Full 256 kB RAM retention and RTCC running from LFXO | — | 2.9 | — | µA |
| | | Full 256 kB RAM retention and RTCC running from LFRCO | — | 3.2 | — | µA |
| | | 16 kB (1 bank) RAM retention and RTCC running from LFRCO ² | — | 2.1 | 3.5 | µA |
| Current consumption in EM3 mode, with voltage scaling enabled | I _{EM3_VS} | Full 256 kB RAM retention and CRYOTIMER running from ULFRCO | — | 2.56 | 4.8 | µA |
| Current consumption in EM4H mode, with voltage scaling enabled | I _{EM4H_VS} | 128 byte RAM retention, RTCC running from LFXO | — | 1.0 | — | µA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.45 | — | µA |
| | | 128 byte RAM retention, no RTCC | — | 0.43 | 0.9 | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|------------|---------------------------|-----|------|-----|---------------|
| Current consumption in EM4S mode | I_{EM4S} | No RAM retention, no RTCC | — | 0.04 | 0.1 | μA |

Note:

1. CMU_HFXOCTRL_LOWPOWER=1.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V using DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|--|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode ² | I _{ACTIVE_DCM} | 38.4 MHz crystal, CPU running while loop from flash ⁴ | — | 86 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 70 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 70 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 85 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 77 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 636 | — | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode ¹ | I _{ACTIVE_CCM} | 38.4 MHz crystal, CPU running while loop from flash ⁴ | — | 96 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 81 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 82 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 95 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 95 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1155 | — | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode ³ | I _{ACTIVE_LPM} | 38.4 MHz crystal, CPU running while loop from flash ⁴ | — | 80 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 64 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 64 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 79 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 66 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 224 | — | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode ¹ | I _{ACTIVE_CCM_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 101 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1128 | — | μA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode ³ | I _{ACTIVE_LPM_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 58 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 196 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode ² | I _{EM1_DCM} | 38.4 MHz crystal ⁴ | — | 56 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 41 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 48 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 610 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode ³ | I _{EM1_LPM} | 38.4 MHz crystal ⁴ | — | 49 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 33 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 35 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 194 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode ² | I _{EM1_DCM_VS} | 19 MHz HFRCO | — | 52 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 587 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode ³ | I _{EM1_LPM_VS} | 19 MHz HFRCO | — | 32 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 170 | — | μA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode ³ | I _{EM2_VS} | Full 256 kB RAM retention and RTCC running from LFXO | — | 2.1 | — | μA |
| | | Full 256 kB RAM retention and RTCC running from LFRCO | — | 2.2 | — | μA |
| | | 16 kB (1 bank) RAM retention and RTCC running from LFRCO ⁵ | — | 1.5 | — | μA |
| Current consumption in EM3 mode, with voltage scaling enabled | I _{EM3_VS} | Full 256 kB RAM retention and CRYOTIMER running from ULFRCO | — | 1.81 | — | μA |
| Current consumption in EM4H mode, with voltage scaling enabled | I _{EM4H_VS} | 128 byte RAM retention, RTCC running from LFXO | — | 0.69 | — | μA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.39 | — | μA |
| | | 128 byte RAM retention, no RTCC | — | 0.39 | — | μA |
| Current consumption in EM4S mode | I _{EM4S} | No RAM retention, no RTCC | — | 0.06 | — | μA |

Note:

- DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
- DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
- DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMLIMSEL=1, ANASW=DVDD.
- CMU_HFXOCTRL_LOWPOWER=1.
- CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.5.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.7. Current Consumption 1.8 V without DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|---|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled | I _{ACTIVE} | 38.4 MHz crystal, CPU running while loop from flash ¹ | — | 126 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 99 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 99 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 124 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 102 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 277 | — | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled | I _{ACTIVE_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 87 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 231 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | I _{EM1} | 38.4 MHz crystal ¹ | — | 76 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 50 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 52 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 227 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled | I _{EM1_VS} | 19 MHz HFRCO | — | 47 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 190 | — | μA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled | I _{EM2_VS} | Full 256 kB RAM retention and RTCC running from LFXO | — | 2.8 | — | μA |
| | | Full 256 kB RAM retention and RTCC running from LFRCO | — | 3.0 | — | μA |
| | | 16 kB (1 bank) RAM retention and RTCC running from LFRCO ² | — | 1.9 | — | μA |
| Current consumption in EM3 mode, with voltage scaling enabled | I _{EM3_VS} | Full 256 kB RAM retention and CRYOTIMER running from ULFR-CO | — | 2.47 | — | μA |
| Current consumption in EM4H mode, with voltage scaling enabled | I _{EM4H_VS} | 128 byte RAM retention, RTCC running from LFXO | — | 0.91 | — | μA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.35 | — | μA |
| | | 128 byte RAM retention, no RTCC | — | 0.35 | — | μA |
| Current consumption in EM4S mode | I _{EM4S} | No RAM retention, no RTCC | — | 0.04 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. CMU_HFXOCTRL_LOWPOWER=1. | | | | | | |
| 2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1 | | | | | | |

4.1.6 Wake Up Times

Table 4.8. Wake Up Times

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---|-----|------|-----|---------------|
| Wakeup time from EM1 | t_{EM1_WU} | | — | 3 | — | AHB Clocks |
| Wake up from EM2 | t_{EM2_WU} | Code execution from flash | — | 10.1 | — | μs |
| | | Code execution from RAM | — | 3.2 | — | μs |
| Wake up from EM3 | t_{EM3_WU} | Code execution from flash | — | 10.1 | — | μs |
| | | Code execution from RAM | — | 3.2 | — | μs |
| Wake up from EM4H ¹ | t_{EM4H_WU} | Executing from flash | — | 80 | — | μs |
| Wake up from EM4S ¹ | t_{EM4S_WU} | Executing from flash | — | 291 | — | μs |
| Time from release of reset source to first instruction execution | t_{RESET} | Soft Pin Reset released | — | 43 | — | μs |
| | | Any other reset released | — | 350 | — | μs |
| Power mode scaling time | t_{SCALE} | VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{4 2} | — | 31.8 | — | μs |
| | | VSCALE2 to VSCALE0, HFCLK = 19 MHz ³ | — | 4.3 | — | μs |

Note:

1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/ μs for approximately 20 μs . During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.

4.1.7 Brown Out Detector (BOD)

Table 4.9. Brown Out Detector (BOD)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------------|----------------------------|------------------------------|------|-----|------|------|
| DVDD BOD threshold | V _{DVddbod} | DVDD rising | — | — | 1.62 | V |
| | | DVDD falling (EM0/EM1) | 1.35 | — | — | V |
| | | DVDD falling (EM2/EM3) | 1.3 | — | — | V |
| DVDD BOD hysteresis | V _{DVddbod_hyst} | | — | 18 | — | mV |
| DVDD BOD response time | t _{DVddbod_delay} | Supply drops at 0.1V/μs rate | — | 2.4 | — | μs |
| AVDD BOD threshold | V _{AVddbod} | AVDD rising | — | — | 1.8 | V |
| | | AVDD falling (EM0/EM1) | 1.62 | — | — | V |
| | | AVDD falling (EM2/EM3) | 1.53 | — | — | V |
| AVDD BOD hysteresis | V _{AVddbod_hyst} | | — | 20 | — | mV |
| AVDD BOD response time | t _{AVddbod_delay} | Supply drops at 0.1V/μs rate | — | 2.4 | — | μs |
| EM4 BOD threshold | V _{EM4bod} | AVDD rising | — | — | 1.7 | V |
| | | AVDD falling | 1.45 | — | — | V |
| EM4 BOD hysteresis | V _{EM4bod_hyst} | | — | 25 | — | mV |
| EM4 BOD response time | t _{EM4bod_delay} | Supply drops at 0.1V/μs rate | — | 300 | — | μs |

4.1.8 Oscillators

4.1.8.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.10. Low-Frequency Crystal Oscillator (LFXO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---|-----|--------|-----|------------|
| Crystal frequency | f_{LFXO} | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{LFXO} | | — | — | 70 | k Ω |
| Supported range of crystal load capacitance ¹ | C_{LFXO_CL} | | 6 | — | 18 | pF |
| On-chip tuning cap range ² | C_{LFXO_T} | On each of LFX TAL_N and LFX TAL_P pins | 8 | — | 40 | pF |
| On-chip tuning cap step size | SS_{LFXO} | | — | 0.25 | — | pF |
| Current consumption after startup ³ | I_{LFXO} | ESR = 70 k Ω , C_L = 7 pF, GAIN ⁴ = 2, AGC ⁴ = 1 | — | 273 | — | nA |
| Start-up time | t_{LFXO} | ESR = 70 k Ω , C_L = 7 pF, GAIN ⁴ = 2 | — | 308 | — | ms |

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be $C_{LFXO_T} / 2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.8.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.11. High-Frequency Crystal Oscillator (HFXO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--|---------------------------------------|-----|------|-----|---------------|
| Crystal frequency | f_{HFXO} | | 38 | 38.4 | 40 | MHz |
| Supported crystal equivalent series resistance (ESR) | $\text{ESR}_{\text{HFXO}_38\text{M4}}$ | Crystal frequency 38.4 MHz | — | — | 60 | Ω |
| Supported range of crystal load capacitance ¹ | $C_{\text{HFXO_CL}}$ | | 6 | — | 12 | pF |
| On-chip tuning cap range ² | $C_{\text{HFXO_T}}$ | On each of HFXTAL_N and HFXTAL_P pins | 9 | 20 | 25 | pF |
| On-chip tuning capacitance step | SS_{HFXO} | | — | 0.04 | — | pF |
| Startup time | t_{HFXO} | 38.4 MHz, ESR = 50 Ohm, $C_L = 10$ pF | — | 300 | — | μs |
| Frequency tolerance for the crystal | FT_{HFXO} | 38.4 MHz, ESR = 50 Ohm, $C_L = 10$ pF | -40 | — | 40 | ppm |

Note:

- Total load capacitance as seen by the crystal.
- The effective load capacitance seen by the crystal will be $C_{\text{HFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.8.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.12. Low-Frequency RC Oscillator (LFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------------|---|------|--------|------|---------------|
| Oscillation frequency | f_{LFRCO} | $\text{ENVREF}^2 = 1$ | 31.3 | 32.768 | 33.6 | kHz |
| | | $\text{ENVREF}^2 = 1, T > 85^\circ\text{C}$ | 31.6 | 32.768 | 36.8 | kHz |
| | | $\text{ENVREF}^2 = 0$ | 31.3 | 32.768 | 33.4 | kHz |
| | | $\text{ENVREF}^2 = 0, T > 85^\circ\text{C}$ | 30.0 | 32.768 | 33.4 | kHz |
| Startup time | t_{LFRCO} | | — | 500 | — | μs |
| Current consumption ¹ | I_{LFRCO} | ENVREF = 1 in CMU_LFRCOCTRL | — | 370 | — | nA |
| | | ENVREF = 0 in CMU_LFRCOCTRL | — | 520 | — | nA |

Note:

- Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
- In CMU_LFRCOCTRL register.

4.1.8.4 High-Frequency RC Oscillator (HFRCO)

Table 4.13. High-Frequency RC Oscillator (HFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------------|---|------|---------------|-----|---------------|
| Frequency accuracy | $f_{\text{HFRCO_ACC}}$ | At production calibrated frequencies, across supply voltage and temperature | -2.5 | — | 2.5 | % |
| Start-up time | t_{HFRCO} | $f_{\text{HFRCO}} \geq 19 \text{ MHz}$ | — | 300 | — | ns |
| | | $4 < f_{\text{HFRCO}} < 19 \text{ MHz}$ | — | 1 | — | μs |
| | | $f_{\text{HFRCO}} \leq 4 \text{ MHz}$ | — | 2.5 | — | μs |
| Maximum DPLL lock time ¹ | $t_{\text{DPLL_LOCK}}$ | $f_{\text{REF}} = 32.768 \text{ kHz}$, $f_{\text{HFRCO}} = 39.98 \text{ MHz}$, $N = 1219$, $M = 0$ | — | 183 | — | μs |
| Current consumption on all supplies | I_{HFRCO} | $f_{\text{HFRCO}} = 38 \text{ MHz}$ | — | 244 | 265 | μA |
| | | $f_{\text{HFRCO}} = 32 \text{ MHz}$ | — | 204 | 222 | μA |
| | | $f_{\text{HFRCO}} = 26 \text{ MHz}$ | — | 173 | 188 | μA |
| | | $f_{\text{HFRCO}} = 19 \text{ MHz}$ | — | 143 | 156 | μA |
| | | $f_{\text{HFRCO}} = 16 \text{ MHz}$ | — | 123 | 136 | μA |
| | | $f_{\text{HFRCO}} = 13 \text{ MHz}$ | — | 110 | 124 | μA |
| | | $f_{\text{HFRCO}} = 7 \text{ MHz}$ | — | 85 | 94 | μA |
| | | $f_{\text{HFRCO}} = 4 \text{ MHz}$ | — | 32 | 37 | μA |
| | | $f_{\text{HFRCO}} = 2 \text{ MHz}$ | — | 28 | 34 | μA |
| | | $f_{\text{HFRCO}} = 1 \text{ MHz}$ | — | 26 | 31 | μA |
| | | $f_{\text{HFRCO}} = 40 \text{ MHz}$, DPLL enabled | — | 423 | 470 | μA |
| | | $f_{\text{HFRCO}} = 32 \text{ MHz}$, DPLL enabled | — | 338 | 375 | μA |
| | | $f_{\text{HFRCO}} = 16 \text{ MHz}$, DPLL enabled | — | 192 | 220 | μA |
| | | $f_{\text{HFRCO}} = 4 \text{ MHz}$, DPLL enabled | — | 51 | 75 | μA |
| $f_{\text{HFRCO}} = 1 \text{ MHz}$, DPLL enabled | — | 36 | 50 | μA | | |
| Coarse trim step size (% of period) | $SS_{\text{HFRCO_COARSE}}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{\text{HFRCO_FINE}}$ | | — | 0.1 | — | % |
| Period jitter | PJ_{HFRCO} | | — | 0.2 | — | % RMS |
| Note: | | | | | | |
| 1. Maximum DPLL lock time $\approx 6 \times (M+1) \times t_{\text{REF}}$, where t_{REF} is the reference clock period. | | | | | | |

4.1.8.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Table 4.14. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|--------------------------------|---|-----|-----|-----|---------------|
| Frequency accuracy | $f_{\text{AUXHFRCO_ACC}}$ | At production calibrated frequencies, across supply voltage and temperature | -3 | — | 3 | % |
| Start-up time | t_{AUXHFRCO} | $f_{\text{AUXHFRCO}} \geq 19 \text{ MHz}$ | — | 400 | — | ns |
| | | $4 < f_{\text{AUXHFRCO}} < 19 \text{ MHz}$ | — | 1.4 | — | μs |
| | | $f_{\text{AUXHFRCO}} \leq 4 \text{ MHz}$ | — | 2.5 | — | μs |
| Current consumption on all supplies | I_{AUXHFRCO} | $f_{\text{AUXHFRCO}} = 38 \text{ MHz}$ | — | 193 | 213 | μA |
| | | $f_{\text{AUXHFRCO}} = 32 \text{ MHz}$ | — | 157 | 175 | μA |
| | | $f_{\text{AUXHFRCO}} = 26 \text{ MHz}$ | — | 135 | 151 | μA |
| | | $f_{\text{AUXHFRCO}} = 19 \text{ MHz}$ | — | 108 | 122 | μA |
| | | $f_{\text{AUXHFRCO}} = 16 \text{ MHz}$ | — | 100 | 113 | μA |
| | | $f_{\text{AUXHFRCO}} = 13 \text{ MHz}$ | — | 77 | 88 | μA |
| | | $f_{\text{AUXHFRCO}} = 7 \text{ MHz}$ | — | 53 | 63 | μA |
| | | $f_{\text{AUXHFRCO}} = 4 \text{ MHz}$ | — | 29 | 36 | μA |
| | | $f_{\text{AUXHFRCO}} = 2 \text{ MHz}$ | — | 28 | 34 | μA |
| | | $f_{\text{AUXHFRCO}} = 1 \text{ MHz}$ | — | 27 | 31 | μA |
| Coarse trim step size (% of period) | $SS_{\text{AUXHFRCO_COARSE}}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{\text{AUXHFRCO_FINE}}$ | | — | 0.1 | — | % |
| Period jitter | PJ_{AUXHFRCO} | | — | 0.2 | — | % RMS |

4.1.8.6 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.15. Ultra-low Frequency RC Oscillator (ULFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------|---------------------|----------------|------|-----|------|------|
| Oscillation frequency | f_{ULFRCO} | | 0.95 | 1 | 1.07 | kHz |

4.1.9 Flash Memory Characteristics⁵

Table 4.16. Flash Memory Characteristics⁵

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------|---|-------|------|-----|--------|
| Flash erase cycles before failure | EC _{FLASH} | | 10000 | — | — | cycles |
| Flash data retention | RET _{FLASH} | T ≤ 85 °C | 10 | — | — | years |
| | | T ≤ 125 °C | 10 | — | — | years |
| Word (32-bit) programming time | t _{W_PROG} | Burst write, 128 words, average time per word | 20 | 24.4 | 30 | µs |
| | | Single word | 60 | 68.4 | 80 | µs |
| Page erase time ⁴ | t _{PERASE} | | 20 | 26.4 | 35 | ms |
| Mass erase time ¹ | t _{MERASE} | | 20 | 26.5 | 35 | ms |
| Device erase time ^{2 3} | t _{DERASE} | T ≤ 85 °C | — | 82 | 100 | ms |
| | | T ≤ 125 °C | — | 82 | 110 | ms |
| Erase current ⁶ | I _{ERASE} | Page Erase | — | — | 1.6 | mA |
| Write current ⁶ | I _{WRITE} | | — | — | 3.8 | mA |
| Supply voltage during flash erase and write | V _{FLASH} | | 1.62 | — | 3.6 | V |

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

4.1.10 General-Purpose I/O (GPIO)

Table 4.17. General-Purpose I/O (GPIO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------|---|-----------|-----|-----------|------|
| Input low voltage | V _{IL} | GPIO pins | — | — | IOVDD*0.3 | V |
| | | RESETn | — | — | AVDD*0.3 | v |
| Input high voltage | V _{IH} | GPIO pins | IOVDD*0.7 | — | — | V |
| | | RESETn | AVDD*0.7 | — | — | v |
| Output high voltage relative to IOVDD | V _{OH} | Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ¹ = WEAK | IOVDD*0.8 | — | — | V |
| | | Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ¹ = WEAK | IOVDD*0.6 | — | — | V |
| | | Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ¹ = STRONG | IOVDD*0.8 | — | — | V |
| | | Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ¹ = STRONG | IOVDD*0.6 | — | — | V |
| Output low voltage relative to IOVDD | V _{OL} | Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ¹ = WEAK | — | — | IOVDD*0.2 | V |
| | | Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ¹ = WEAK | — | — | IOVDD*0.4 | V |
| | | Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ¹ = STRONG | — | — | IOVDD*0.2 | V |
| | | Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ¹ = STRONG | — | — | IOVDD*0.4 | V |
| Input leakage current | I _{IOLEAK} | All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C | — | 0.1 | 30 | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C | — | 0.1 | 50 | nA |
| | | All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C | — | — | 110 | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T > 85 °C | — | — | 250 | nA |
| Input leakage current on 5VTOL pads above IOVDD | I _{5VTOLLEAK} | IOVDD < GPIO ≤ IOVDD + 2 V | — | 3.3 | 15 | μA |
| I/O pin pull-up/pull-down resistor | R _{PUD} | | 30 | 40 | 65 | kΩ |
| Pulse width of pulses removed by the glitch suppression filter | t _{IOGLITCH} | | 15 | 25 | 45 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------|---|-----|-----|-----|------|
| Output fall time, From 70% to 30% of V_{IO} | t_{IOF} | $C_L = 50$ pF, DRIVESTRENGTH ¹ = STRONG, SLEWRATE ¹ = 0x6 | — | 1.8 | — | ns |
| | | $C_L = 50$ pF, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6 | — | 4.5 | — | ns |
| Output rise time, From 30% to 70% of V_{IO} | t_{IOR} | $C_L = 50$ pF, DRIVESTRENGTH ¹ = STRONG, SLEWRATE = 0x6 ¹ | — | 2.2 | — | ns |
| | | $C_L = 50$ pF, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6 | — | 7.4 | — | ns |
| RESETn low time to ensure pin reset | T_{RESET} | | 100 | — | — | ns |

Note:

1. In GPIO_Pn_CTRL register.

4.1.11 Voltage Monitor (VMON)

Table 4.18. Voltage Monitor (VMON)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|--|------|------|-----|------|
| Supply current (including I _{SENSE}) | I _{VMON} | In EM0 or EM1, 1 supply monitored, T ≤ 85 °C | — | 6.3 | 10 | μA |
| | | In EM0 or EM1, 1 supply monitored, T > 85 °C | — | — | 14 | μA |
| | | In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C | — | 12.5 | 17 | μA |
| | | In EM0 or EM1, 4 supplies monitored, T > 85 °C | — | — | 21 | μA |
| | | In EM2, EM3 or EM4, 1 supply monitored and above threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, 1 supply monitored and below threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, 4 supplies monitored and all above threshold | — | 99 | — | nA |
| | | In EM2, EM3 or EM4, 4 supplies monitored and all below threshold | — | 99 | — | nA |
| Loading of monitored supply | I _{SENSE} | In EM0 or EM1 | — | 2 | — | μA |
| | | In EM2, EM3 or EM4 | — | 2 | — | nA |
| Threshold range | V _{VMON_RANGE} | | 1.62 | — | 3.4 | V |
| Threshold step size | N _{VMON_STESP} | Coarse | — | 200 | — | mV |
| | | Fine | — | 20 | — | mV |
| Response time | t _{VMON_RES} | Supply drops at 1V/μs rate | — | 460 | — | ns |
| Hysteresis | V _{VMON_HYST} | | — | 26 | — | mV |

4.1.12 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.19. Analog to Digital Converter (ADC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------------------|--|---------------------|-----|--------------------|------|
| Resolution | V _{RESOLUTION} | | 6 | — | 12 | Bits |
| Input voltage range ⁵ | V _{ADCIN} | Single ended | — | — | V _{FS} | V |
| | | Differential | -V _{FS} /2 | — | V _{FS} /2 | V |
| Input range of external reference voltage, single ended and differential | V _{ADCREFIN_P} | | 1 | — | V _{AVDD} | V |
| Power supply rejection ² | PSRR _{ADC} | At DC | — | 80 | — | dB |
| Analog input common mode rejection ratio | CMRR _{ADC} | At DC | — | 80 | — | dB |
| Current from all supplies, using internal reference buffer. Continuous operation. WAR- MUPMODE ⁴ = KEEPADC- WARM | I _{ADC_CONTI- NOUS_LP} | 1 Msps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³ | — | 270 | 315 | μA |
| | | 250 ksps / 4 MHz ADCCLK, BIA- SPROG = 6, GPBIASACC = 1 ³ | — | 125 | — | μA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIA- SPROG = 15, GPBIASACC = 1 ³ | — | 80 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR- MUPMODE ⁴ = NORMAL | I _{ADC_NORMAL_LP} | 35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³ | — | 45 | — | μA |
| | | 5 ksps / 16 MHz ADCCLK BIA- SPROG = 0, GPBIASACC = 1 ³ | — | 8 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ⁴ = KEEP- INSTANDBY or KEEPIN- SLOWACC | I _{ADC_STAND- BY_LP} | 125 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³ | — | 105 | — | μA |
| | | 35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³ | — | 70 | — | μA |
| Current from all supplies, using internal reference buffer. Continuous operation. WAR- MUPMODE ⁴ = KEEPADC- WARM | I _{ADC_CONTI- NOUS_HP} | 1 Msps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ³ | — | 325 | — | μA |
| | | 250 ksps / 4 MHz ADCCLK, BIA- SPROG = 6, GPBIASACC = 0 ³ | — | 175 | — | μA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIA- SPROG = 15, GPBIASACC = 0 ³ | — | 125 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR- MUPMODE ⁴ = NORMAL | I _{ADC_NORMAL_HP} | 35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ³ | — | 85 | — | μA |
| | | 5 ksps / 16 MHz ADCCLK BIA- SPROG = 0, GPBIASACC = 0 ³ | — | 16 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ⁴ = KEEP- INSTANDBY or KEEPIN- SLOWACC | I _{ADC_STAND- BY_HP} | 125 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ³ | — | 160 | — | μA |
| | | 35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ³ | — | 125 | — | μA |
| Current from HFPERCLK | I _{ADC_CLK} | HFPERCLK = 16 MHz | — | 160 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|--|-----|-------|-----|---------------|
| ADC clock frequency | f_{ADCCLK} | | — | — | 16 | MHz |
| Throughput rate | f_{ADCRATE} | | — | — | 1 | Msp/s |
| Conversion time ¹ | t_{ADCCONV} | 6 bit | — | 7 | — | cycles |
| | | 8 bit | — | 9 | — | cycles |
| | | 12 bit | — | 13 | — | cycles |
| Startup time of reference generator and ADC core | t_{ADCSTART} | WARMUPMODE ⁴ = NORMAL | — | — | 5 | μs |
| | | WARMUPMODE ⁴ = KEEPIN-STANDBY | — | — | 2 | μs |
| | | WARMUPMODE ⁴ = KEEPINSLOWACC | — | — | 1 | μs |
| SNDR at 1Msp/s and $f_{\text{IN}} = 10\text{kHz}$ | SNDR _{ADC} | Internal reference ⁷ , differential measurement | 58 | 67 | — | dB |
| | | External reference ⁶ , differential measurement | — | 68 | — | dB |
| Spurious-free dynamic range (SFDR) | SFDR _{ADC} | 1 MSamples/s, 10 kHz full-scale sine wave | — | 75 | — | dB |
| Differential non-linearity (DNL) | DNL _{ADC} | 12 bit resolution, No missing codes | -1 | — | 2 | LSB |
| Integral non-linearity (INL), End point method | INL _{ADC} | 12 bit resolution | -6 | — | 6 | LSB |
| Offset error | $V_{\text{ADCOFFSETERR}}$ | | -3 | 0 | 3 | LSB |
| Gain error in ADC | V_{ADCGAIN} | Using internal reference | — | -0.2 | 3.5 | % |
| | | Using external reference | — | -1 | — | % |
| Temperature sensor slope | $V_{\text{TS_SLOPE}}$ | | — | -1.84 | — | mV/°C |

Note:

- Derived from ADCCLK.
- PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
- In ADCn_BIASPROG register.
- In ADCn_CNTL register.
- The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
- External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is $\pm 1.25\text{ V}$.
- Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is $\pm 1.25\text{ V}$. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

4.1.13 Analog Comparator (ACMP)

Table 4.20. Analog Comparator (ACMP)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|--|------|-----|--------------------|------|
| Input voltage range | V_{ACMPIN} | ACMPVDD = ACMPn_CTRL_PWRSEL ¹ | — | — | $V_{ACMPVDD}$ | V |
| Supply voltage | $V_{ACMPVDD}$ | BIASPROG ⁴ ≤ 0x10 or FULL- BIAS ⁴ = 0 | 1.8 | — | $V_{VREGVDD_MAX}$ | V |
| | | 0x10 < BIASPROG ⁴ ≤ 0x20 and FULLBIAS ⁴ = 1 | 2.1 | — | $V_{VREGVDD_MAX}$ | V |
| Active current not including voltage reference ² | I_{ACMP} | BIASPROG ⁴ = 0x10, FULLBIAS ⁴ = 0 | — | 306 | — | nA |
| | | BIASPROG ⁴ = 0x02, FULLBIAS ⁴ = 1 | — | 6.5 | — | μA |
| | | BIASPROG ⁴ = 0x20, FULLBIAS ⁴ = 1 | — | 75 | 92 | μA |
| Current consumption of inter- nal voltage reference ² | $I_{ACMPREF}$ | VLP selected as input using 2.5 V Reference / 4 (0.625 V) | — | 50 | — | nA |
| | | VLP selected as input using VDD | — | 20 | — | nA |
| | | VBDIV selected as input using 1.25 V reference / 1 | — | 4.1 | — | μA |
| | | VADIV selected as input using VDD/1 | — | 2.4 | — | μA |
| Hysteresis ($V_{CM} = 1.25$ V, BIASPROG ⁴ = 0x10, FULL- BIAS ⁴ = 1) | $V_{ACMPHYST}$ | HYSTSEL ⁵ = HYST0 | -3 | 0 | 3 | mV |
| | | HYSTSEL ⁵ = HYST1 | 5 | 18 | 27 | mV |
| | | HYSTSEL ⁵ = HYST2 | 12 | 33 | 50 | mV |
| | | HYSTSEL ⁵ = HYST3 | 17 | 46 | 67 | mV |
| | | HYSTSEL ⁵ = HYST4 | 23 | 57 | 86 | mV |
| | | HYSTSEL ⁵ = HYST5 | 26 | 68 | 104 | mV |
| | | HYSTSEL ⁵ = HYST6 | 30 | 79 | 130 | mV |
| | | HYSTSEL ⁵ = HYST7 | 34 | 90 | 150 | mV |
| | | HYSTSEL ⁵ = HYST8 | -3 | 0 | 3 | mV |
| | | HYSTSEL ⁵ = HYST9 | -27 | -18 | -5 | mV |
| | | HYSTSEL ⁵ = HYST10 | -50 | -33 | -12 | mV |
| | | HYSTSEL ⁵ = HYST11 | -67 | -45 | -17 | mV |
| | | HYSTSEL ⁵ = HYST12 | -86 | -57 | -23 | mV |
| | | HYSTSEL ⁵ = HYST13 | -104 | -67 | -26 | mV |
| | | HYSTSEL ⁵ = HYST14 | -130 | -78 | -30 | mV |
| HYSTSEL ⁵ = HYST15 | -155 | -88 | -34 | mV | | |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|------------------|---|-----|----------|------|------------|
| Comparator delay ³ | $t_{ACMPDELAY}$ | BIASPROG ⁴ = 0x10, FULLBIAS ⁴ = 0 | — | 3.7 | — | μ s |
| | | BIASPROG ⁴ = 0x02, FULLBIAS ⁴ = 1 | — | 360 | — | ns |
| | | BIASPROG ⁴ = 0x20, FULLBIAS ⁴ = 1 | — | 35 | — | ns |
| Offset voltage | $V_{ACMPOFFSET}$ | BIASPROG ⁴ = 0x10, FULLBIAS ⁴ = 1 | -35 | — | 35 | mV |
| Reference voltage | $V_{ACMPREF}$ | Internal 1.25 V reference | 1 | 1.25 | 1.47 | V |
| | | Internal 2.5 V reference | 2 | 2.5 | 2.8 | V |
| Capacitive sense internal resistance | R_{CSRES} | CSRESSEL ⁶ = 0 | — | infinite | — | k Ω |
| | | CSRESSEL ⁶ = 1 | — | 15 | — | k Ω |
| | | CSRESSEL ⁶ = 2 | — | 27 | — | k Ω |
| | | CSRESSEL ⁶ = 3 | — | 39 | — | k Ω |
| | | CSRESSEL ⁶ = 4 | — | 51 | — | k Ω |
| | | CSRESSEL ⁶ = 5 | — | 100 | — | k Ω |
| | | CSRESSEL ⁶ = 6 | — | 162 | — | k Ω |
| | | CSRESSEL ⁶ = 7 | — | 235 | — | k Ω |

Note:

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
3. ± 100 mV differential drive.
4. In ACMPn_CTRL register.
5. In ACMPn_HYSTERESIS registers.
6. In ACMPn_INPUTSEL register.

4.1.14 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.21. Digital to Analog Converter (VDAC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------|---|-------------|------|------------|-------------|
| Output voltage | V_{DACOUT} | Single-Ended | 0 | — | V_{VREF} | V |
| | | Differential ² | $-V_{VREF}$ | — | V_{VREF} | V |
| Current consumption including references (2 channels) ¹ | I_{DAC} | 500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4 | — | 396 | — | μA |
| | | 44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4 | — | 72 | — | μA |
| | | 200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WARMUPTIME = 0x02 | — | 1.2 | — | μA |
| Current from HFPERCLK ⁴ | I_{DAC_CLK} | | — | 5.8 | — | $\mu A/MHz$ |
| Sample rate | SR_{DAC} | | — | — | 500 | ksps |
| DAC clock frequency | f_{DAC} | | — | — | 1 | MHz |
| Conversion time | $t_{DACCONV}$ | $f_{DAC} = 1MHz$ | 2 | — | — | μs |
| Settling time | $t_{DACSETTLE}$ | 50% fs step settling to 5 LSB | — | 2.5 | — | μs |
| Startup time | $t_{DACSTARTUP}$ | Enable to 90% fs output, settling to 10 LSB | — | — | 12 | μs |
| Output impedance | R_{OUT} | DRIVESTRENGTH = 2, $0.4 V \leq V_{OUT} \leq V_{OPA} - 0.4 V$, $-8 mA < I_{OUT} < 8 mA$, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, $0.4 V \leq V_{OUT} \leq V_{OPA} - 0.4 V$, $-400 \mu A < I_{OUT} < 400 \mu A$, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 2, $0.1 V \leq V_{OUT} \leq V_{OPA} - 0.1 V$, $-2 mA < I_{OUT} < 2 mA$, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, $0.1 V \leq V_{OUT} \leq V_{OPA} - 0.1 V$, $-100 \mu A < I_{OUT} < 100 \mu A$, Full supply range | — | 2 | — | Ω |
| Power supply rejection ratio ⁶ | PSRR | $V_{out} = 50\% fs, DC$ | — | 65.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|---|-------|------|-----|------|
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz | SNDR _{DAC} | 500 ksps, single-ended, internal 1.25V reference | — | 60.4 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 61.6 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 64.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 63.3 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 64.4 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 65.8 | — | dB |
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz | SNDR _{DAC_BAND} | 500 ksps, single-ended, internal 1.25V reference | — | 65.3 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 66.7 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 70.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 67.8 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 69.0 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 68.5 | — | dB |
| Total harmonic distortion | THD | | — | 70.2 | — | dB |
| Differential non-linearity ³ | DNL _{DAC} | | -0.99 | — | 1 | LSB |
| Integral non-linearity | INL _{DAC} | | -4 | — | 4 | LSB |
| Offset error ⁵ | V _{OFFSET} | T = 25 °C | -8 | — | 8 | mV |
| | | Across operating temperature range | -25 | — | 25 | mV |
| Gain error ⁵ | V _{GAIN} | T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -2.5 | — | 2.5 | % |
| | | T = 25 °C, Internal reference (REFSEL = 1V25 or 2V5) | -5 | — | 5 | % |
| | | T = 25 °C, External reference (REFSEL = VDD or EXT) | -1.8 | — | 1.8 | % |
| | | Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -3.5 | — | 3.5 | % |
| | | Across operating temperature range, Internal reference (REFSEL = 1V25 or 2V5) | -7.5 | — | 7.5 | % |
| | | Across operating temperature range, External reference (REFSEL = VDD or EXT) | -2.0 | — | 2.0 | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|-------------------|----------------|-----|-----|-----|------|
| External load capacitance, OUTSCALE=0 | C _{LOAD} | | — | — | 75 | pF |

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HUPERCLK is dependent on HUPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$, VDAC output at 90% of full scale

4.1.15 Current Digital to Analog Converter (IDAC)

Table 4.22. Current Digital to Analog Converter (IDAC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|---|------|------|-----|--------|
| Number of ranges | N_{IDAC_RANGES} | | — | 4 | — | ranges |
| Output current | I_{IDAC_OUT} | RANGSEL ¹ = RANGE0 | 0.05 | — | 1.6 | μA |
| | | RANGSEL ¹ = RANGE1 | 1.6 | — | 4.7 | μA |
| | | RANGSEL ¹ = RANGE2 | 0.5 | — | 16 | μA |
| | | RANGSEL ¹ = RANGE3 | 2 | — | 64 | μA |
| Linear steps within each range | N_{IDAC_STEPS} | | — | 32 | — | steps |
| Step size | SS_{IDAC} | RANGSEL ¹ = RANGE0 | — | 50 | — | nA |
| | | RANGSEL ¹ = RANGE1 | — | 100 | — | nA |
| | | RANGSEL ¹ = RANGE2 | — | 500 | — | nA |
| | | RANGSEL ¹ = RANGE3 | — | 2 | — | μA |
| Total accuracy, STEPSEL ¹ = 0x10 | ACC_{IDAC} | EM0 or EM1, AVDD=3.3 V, T = 25 °C | -3 | — | 3 | % |
| | | EM0 or EM1, Across operating temperature range | -18 | — | 22 | % |
| | | EM2 or EM3, Source mode, RANGSEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C | — | -2 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C | — | -1.7 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.8 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C | — | -0.7 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C | — | -0.6 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| Start up time | t_{IDAC_SU} | Output within 1% of steady state value | — | 5 | — | μs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------------|--|-----|-------|-----|------|
| Settling time, (output settled within 1% of steady state value), | t _{IDAC_SETTLE} | Range setting is changed | — | 5 | — | μs |
| | | Step value is changed | — | 1 | — | μs |
| Current consumption ² | I _{IDAC} | EM0 or EM1 Source mode, excluding output current, Across operating temperature range | — | 11 | 18 | μA |
| | | EM0 or EM1 Sink mode, excluding output current, Across operating temperature range | — | 13 | 21 | μA |
| | | EM2 or EM3 Source mode, excluding output current, T = 25 °C | — | 0.023 | — | μA |
| | | EM2 or EM3 Sink mode, excluding output current, T = 25 °C | — | 0.041 | — | μA |
| | | EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C | — | 11 | — | μA |
| | | EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C | — | 13 | — | μA |
| Output voltage compliance in source mode, source current change relative to current sourced at 0 V | I _{COMP_SRC} | RANGESEL1=0, output voltage = min(V _{IOVDD} , V _{AVDD} ² -100 mV) | — | 0.11 | — | % |
| | | RANGESEL1=1, output voltage = min(V _{IOVDD} , V _{AVDD} ² -100 mV) | — | 0.06 | — | % |
| | | RANGESEL1=2, output voltage = min(V _{IOVDD} , V _{AVDD} ² -150 mV) | — | 0.04 | — | % |
| | | RANGESEL1=3, output voltage = min(V _{IOVDD} , V _{AVDD} ² -250 mV) | — | 0.03 | — | % |
| Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD | I _{COMP_SINK} | RANGESEL1=0, output voltage = 100 mV | — | 0.12 | — | % |
| | | RANGESEL1=1, output voltage = 100 mV | — | 0.05 | — | % |
| | | RANGESEL1=2, output voltage = 150 mV | — | 0.04 | — | % |
| | | RANGESEL1=3, output voltage = 250 mV | — | 0.03 | — | % |

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.16 Capacitive Sense (CSEN)

Table 4.23. Capacitive Sense (CSEN)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|---|-----|------|-----|------|
| Single conversion time (1x accumulation) | t _{CNV} | 12-bit SAR Conversions | — | 20.2 | — | μs |
| | | 16-bit SAR Conversions | — | 26.4 | — | μs |
| | | Delta Modulation Conversion (single comparison) | — | 1.55 | — | μs |
| Maximum external capacitive load | C _{EXTMAX} | CS0CG=7 (Gain = 1x), including routing parasitics | — | 68 | — | pF |
| | | CS0CG=0 (Gain = 10x), including routing parasitics | — | 680 | — | pF |
| Maximum external series impedance | R _{EXTMAX} | | — | 1 | — | kΩ |
| Supply current, EM2 bonded conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0 | I _{CSEN_BOND} | 12-bit SAR conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 326 | — | nA |
| | | Delta Modulation conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 226 | — | nA |
| | | 12-bit SAR conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 33 | — | nA |
| | | Delta Modulation conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 25 | — | nA |
| Supply current, EM2 scan conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0 | I _{CSEN_EM2} | 12-bit SAR conversions, 20 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan ¹ | — | 690 | — | nA |
| | | Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan ¹ | — | 515 | — | nA |
| | | 12-bit SAR conversions, 200 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan ¹ | — | 79 | — | nA |
| | | Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan ¹ | — | 57 | — | nA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|------|-----|--------|
| Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM | I _{CSEN_ACTIVE} | SAR or Delta Modulation conversions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on | — | 90.5 | — | μA |
| HFPERCLK supply current | I _{CSEN_HFPERCLK} | Current contribution from HFPERCLK when clock to CSEN block is enabled. | — | 2.25 | — | μA/MHz |

Note:

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

4.1.17 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes⁸ 1.

Table 4.24. Operational Amplifier (OPAMP)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-------------------|--|------------------|------|-----------------------|------|
| Supply voltage (from AVDD) | V _{OPA} | HCMDIS = 0, Rail-to-rail input range | 2 | — | 3.8 | V |
| | | HCMDIS = 1 | 1.62 | — | 3.8 | V |
| Input voltage | V _{IN} | HCMDIS = 0, Rail-to-rail input range | V _{VSS} | — | V _{OPA} | V |
| | | HCMDIS = 1 | V _{VSS} | — | V _{OPA} -1.2 | V |
| Input impedance | R _{IN} | | 100 | — | — | MΩ |
| Output voltage | V _{OUT} | | V _{VSS} | — | V _{OPA} | V |
| Load capacitance ² | C _{LOAD} | OUTSCALE = 0 | — | — | 75 | pF |
| | | OUTSCALE = 1 | — | — | 37.5 | pF |
| Output impedance | R _{OUT} | DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -8 mA < I _{OUT} < 8 mA, Buffer connection, Full supply range | — | 0.25 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -400 μA < I _{OUT} < 400 μA, Buffer connection, Full supply range | — | 0.6 | — | Ω |
| | | DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -2 mA < I _{OUT} < 2 mA, Buffer connection, Full supply range | — | 0.4 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -100 μA < I _{OUT} < 100 μA, Buffer connection, Full supply range | — | 1 | — | Ω |
| Internal closed-loop gain | G _{CL} | Buffer connection | 0.99 | 1 | 1.01 | - |
| | | 3x Gain connection | 2.93 | 2.99 | 3.05 | - |
| | | 16x Gain connection | 15.07 | 15.7 | 16.33 | - |
| Active current ⁴ | I _{OPA} | DRIVESTRENGTH = 3, OUTSCALE = 0 | — | 580 | — | μA |
| | | DRIVESTRENGTH = 2, OUTSCALE = 0 | — | 176 | — | μA |
| | | DRIVESTRENGTH = 1, OUTSCALE = 0 | — | 13 | — | μA |
| | | DRIVESTRENGTH = 0, OUTSCALE = 0 | — | 4.7 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|------------------|---|-----|------|-----|-------|
| Open-loop gain | G _{OL} | DRIVESTRENGTH = 3 | — | 135 | — | dB |
| | | DRIVESTRENGTH = 2 | — | 137 | — | dB |
| | | DRIVESTRENGTH = 1 | — | 121 | — | dB |
| | | DRIVESTRENGTH = 0 | — | 109 | — | dB |
| Loop unit-gain frequency ⁷ | UGF | DRIVESTRENGTH = 3, Buffer connection | — | 3.38 | — | MHz |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 0.9 | — | MHz |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 132 | — | kHz |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 34 | — | kHz |
| | | DRIVESTRENGTH = 3, 3x Gain connection | — | 2.57 | — | MHz |
| | | DRIVESTRENGTH = 2, 3x Gain connection | — | 0.71 | — | MHz |
| | | DRIVESTRENGTH = 1, 3x Gain connection | — | 113 | — | kHz |
| | | DRIVESTRENGTH = 0, 3x Gain connection | — | 28 | — | kHz |
| Phase margin | PM | DRIVESTRENGTH = 3, Buffer connection | — | 67 | — | ° |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 69 | — | ° |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 63 | — | ° |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 68 | — | ° |
| Output voltage noise | N _{OUT} | DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz | — | 146 | — | μVrms |
| | | DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz | — | 163 | — | μVrms |
| | | DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz | — | 170 | — | μVrms |
| | | DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz | — | 176 | — | μVrms |
| | | DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz | — | 313 | — | μVrms |
| | | DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz | — | 271 | — | μVrms |
| | | DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz | — | 247 | — | μVrms |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz | — | 245 | — | μVrms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|--|-----|-------|-----|------------|
| Slew rate ⁵ | SR | DRIVESTRENGTH = 3, INCBW=1 ³ | — | 4.7 | — | V/ μ s |
| | | DRIVESTRENGTH = 3, INCBW=0 | — | 1.5 | — | V/ μ s |
| | | DRIVESTRENGTH = 2, INCBW=1 ³ | — | 1.27 | — | V/ μ s |
| | | DRIVESTRENGTH = 2, INCBW=0 | — | 0.42 | — | V/ μ s |
| | | DRIVESTRENGTH = 1, INCBW=1 ³ | — | 0.17 | — | V/ μ s |
| | | DRIVESTRENGTH = 1, INCBW=0 | — | 0.058 | — | V/ μ s |
| | | DRIVESTRENGTH = 0, INCBW=1 ³ | — | 0.044 | — | V/ μ s |
| | | DRIVESTRENGTH = 0, INCBW=0 | — | 0.015 | — | V/ μ s |
| Startup time ⁶ | T _{START} | DRIVESTRENGTH = 2 | — | — | 12 | μ s |
| Input offset voltage | V _{OSI} | DRIVESTRENGTH = 2 or 3, T = 25 °C | -2 | — | 2 | mV |
| | | DRIVESTRENGTH = 1 or 0, T = 25 °C | -2 | — | 2 | mV |
| | | DRIVESTRENGTH = 2 or 3, across operating temperature range | -12 | — | 12 | mV |
| | | DRIVESTRENGTH = 1 or 0, across operating temperature range | -30 | — | 30 | mV |
| DC power supply rejection ratio ⁹ | PSRR _{DC} | Input referred | — | 70 | — | dB |
| DC common-mode rejection ratio ⁹ | CMRR _{DC} | Input referred | — | 70 | — | dB |
| Total harmonic distortion | THD _{OPA} | DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V | — | 90 | — | dB |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V | — | 90 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, $V_{INPUT} = 0.5\text{ V}$, $V_{OUTPUT} = 1.5\text{ V}$. Nominal voltage gain is 3. | | | | | | |
| 2. If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. | | | | | | |
| 3. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3 , or the OPAMP may not be stable. | | | | | | |
| 4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1 , there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another $\sim 10\text{ }\mu\text{A}$ current when the OPAMP drives 1.5 V between output and ground. | | | | | | |
| 5. Step between 0.2V and $V_{OPA}-0.2\text{V}$, 10%-90% rising/falling range. | | | | | | |
| 6. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error $< 1\text{mV}$. | | | | | | |
| 7. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network. | | | | | | |
| 8. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. $V_{INPUT} = 0.5\text{ V}$, $V_{OUTPUT} = 0.5\text{ V}$. | | | | | | |
| 9. When HCMDIS=1 and input common mode transitions the region from $V_{OPA}-1.4\text{V}$ to $V_{OPA}-1\text{V}$, input offset will change. PSRR and CMRR specifications do not apply to this transition region. | | | | | | |

4.1.18 Pulse Counter (PCNT)

Table 4.25. Pulse Counter (PCNT)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------|----------|--|-----|-----|-----|------|
| Input frequency | F_{IN} | Asynchronous Single and Quadrature Modes | — | — | 20 | MHz |
| | | Sampled Modes with Debounce filter set to 0. | — | — | 8 | kHz |

4.1.19 Analog Port (APORT)

Table 4.26. Analog Port (APORT)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-------------|----------------------|-----|-----|-----|---------------|
| Supply current ^{2 1} | I_{APORT} | Operation in EM0/EM1 | — | 7 | — | μA |
| | | Operation in EM2/EM3 | — | 67 | — | nA |

Note:

- Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.
- Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

4.1.20 I2C

4.1.20.1 I2C Standard-mode (Sm)¹Table 4.27. I2C Standard-mode (Sm)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|-----|-----|------|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 100 | kHz |
| SCL clock low time | t _{LOW} | | 4.7 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 4 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 250 | — | — | ns |
| SDA hold time ³ | t _{HD_DAT} | | 100 | — | 3450 | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 4.7 | — | — | μs |
| (Repeated) START condition hold time | t _{HD_STA} | | 4 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 4 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 4.7 | — | — | μs |

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.20.2 I2C Fast-mode (Fm)¹Table 4.28. I2C Fast-mode (Fm)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|-----|-----|-----|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 400 | kHz |
| SCL clock low time | t _{LOW} | | 1.3 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 0.6 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 100 | — | — | ns |
| SDA hold time ³ | t _{HD_DAT} | | 100 | — | 900 | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 0.6 | — | — | μs |
| (Repeated) START condition hold time | t _{HD_STA} | | 0.6 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 0.6 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 1.3 | — | — | μs |

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.20.3 I2C Fast-mode Plus (Fm+)¹Table 4.29. I2C Fast-mode Plus (Fm+)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|------|-----|------|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 1000 | kHz |
| SCL clock low time | t _{LOW} | | 0.5 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 0.26 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 50 | — | — | ns |
| SDA hold time | t _{HD_DAT} | | 100 | — | — | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 0.26 | — | — | μs |
| (Repeated) START condition hold time | t _{HD_STA} | | 0.26 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 0.26 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 0.5 | — | — | μs |

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.21 USART SPI

SPI Master Timing

Table 4.30. SPI Master Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------|----------------|---------------------------|-----|------|------|
| SCLK period ^{1 3 2} | t_{SCLK} | | $2 * t_{H\text{FPERCLK}}$ | — | — | ns |
| CS to MOSI ^{1 3} | t_{CS_MO} | | -14.5 | — | 13.5 | ns |
| SCLK to MOSI ^{1 3} | t_{SCLK_MO} | | -8.5 | — | 8 | ns |
| MISO setup time ^{1 3} | t_{SU_MI} | IOVDD = 1.62 V | 92 | — | — | ns |
| | | IOVDD = 3.0 V | 42 | — | — | ns |
| MISO hold time ^{1 3} | t_{H_MI} | | -10 | — | — | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{H\text{FPERCLK}}$ is one period of the selected H FPERCLK .
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

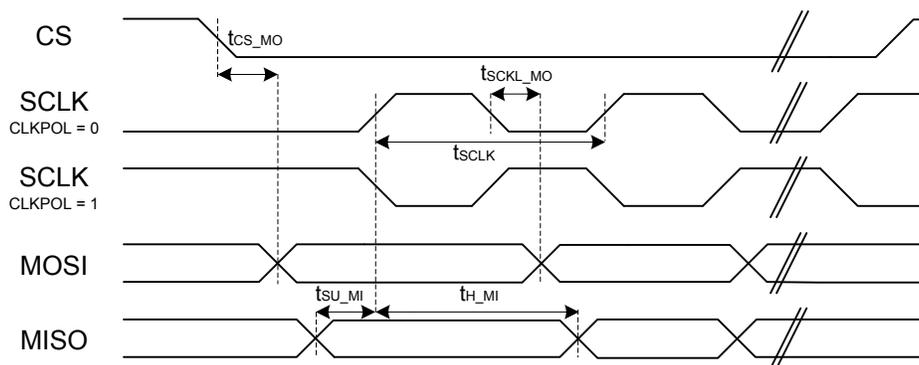


Figure 4.1. SPI Master Timing Diagram (SMSDELAY = 0)

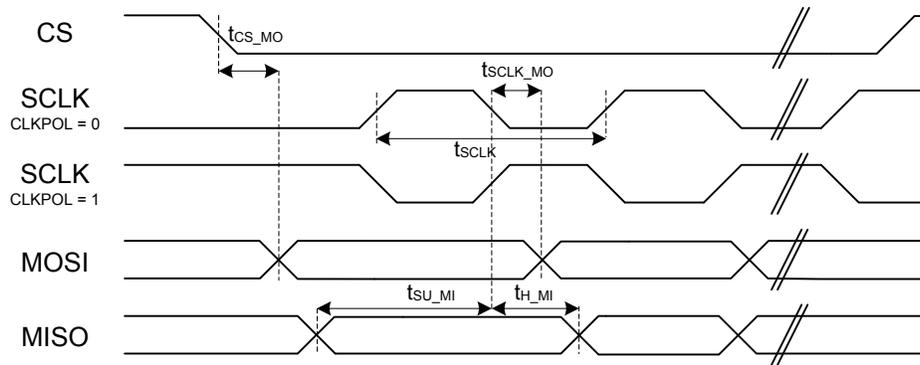


Figure 4.2. SPI Master Timing Diagram (SMSDELAY = 1)

SPI Slave Timing

Table 4.31. SPI Slave Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|-------------------|----------------|-------------------------------------|-----|-------------------------------------|------|
| SCLK period ^{1 3 2} | t_{SCLK} | | 6 * $t_{H\text{FPERCLK}}$ | — | — | ns |
| SCLK high time ^{1 3 2} | t_{SCLK_HI} | | 2.5 * $t_{H\text{FPERCLK}}$ | — | — | ns |
| SCLK low time ^{1 3 2} | t_{SCLK_LO} | | 2.5 * $t_{H\text{FPERCLK}}$ | — | — | ns |
| CS active to MISO ^{1 3} | $t_{CS_ACT_MI}$ | | 4 | — | 70 | ns |
| CS disable to MISO ^{1 3} | $t_{CS_DIS_MI}$ | | 4 | — | 50 | ns |
| MOSI setup time ^{1 3} | t_{SU_MO} | | 8 | — | — | ns |
| MOSI hold time ^{1 3 2} | t_{H_MO} | | 7 | — | — | ns |
| SCLK to MISO ^{1 3 2} | t_{SCLK_MI} | | 10 + 1.5 * $t_{H\text{FPERCLK}}$ | — | 65 + 2.5 * $t_{H\text{FPERCLK}}$ | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{H\text{FPERCLK}}$ is one period of the selected H FPERCLK .
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

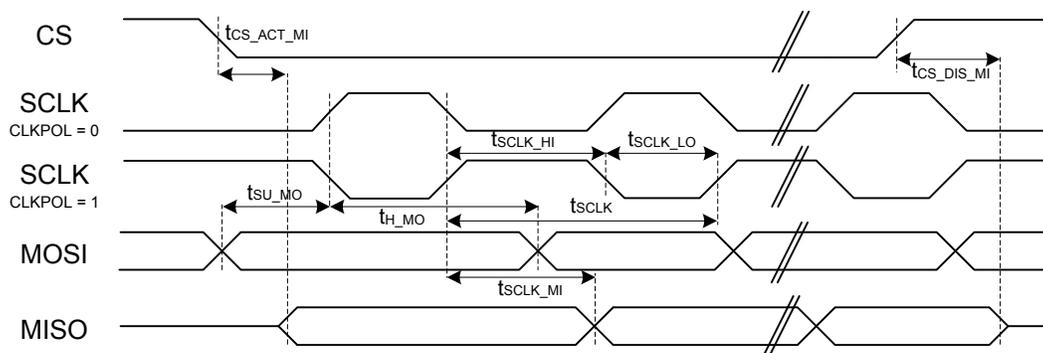


Figure 4.3. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

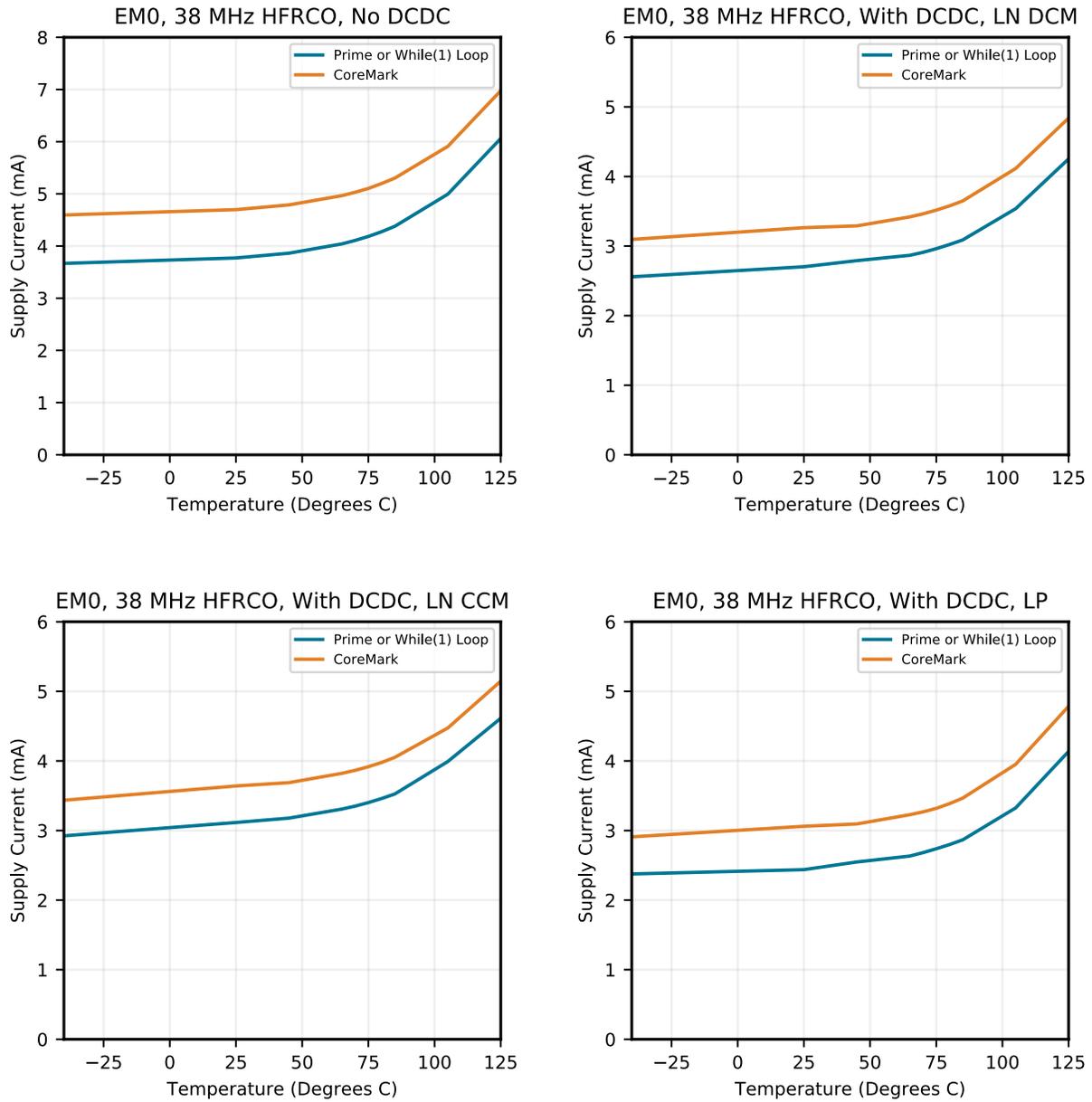


Figure 4.4. EM0 Active Mode Typical Supply Current vs. Temperature

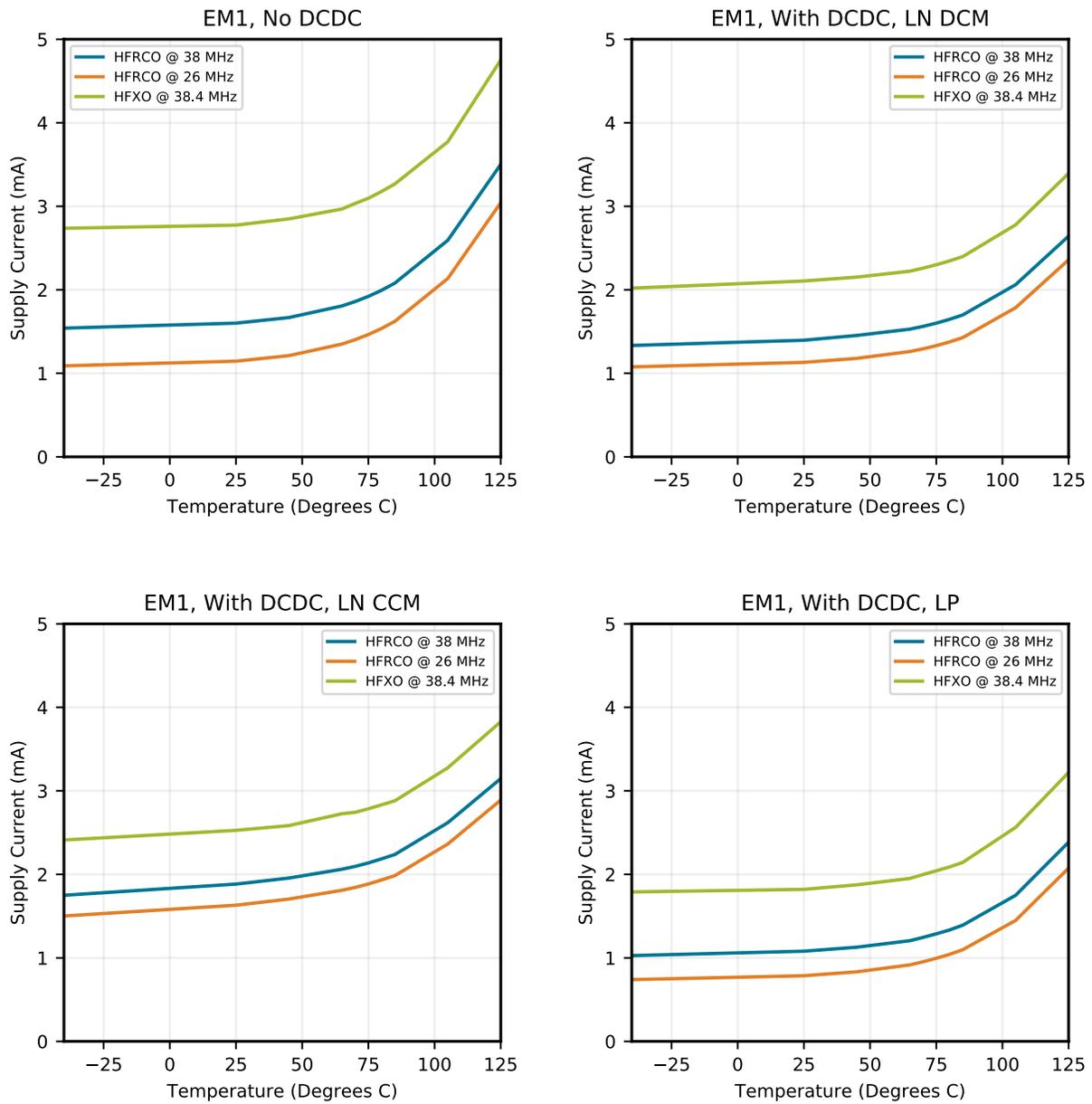


Figure 4.5. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

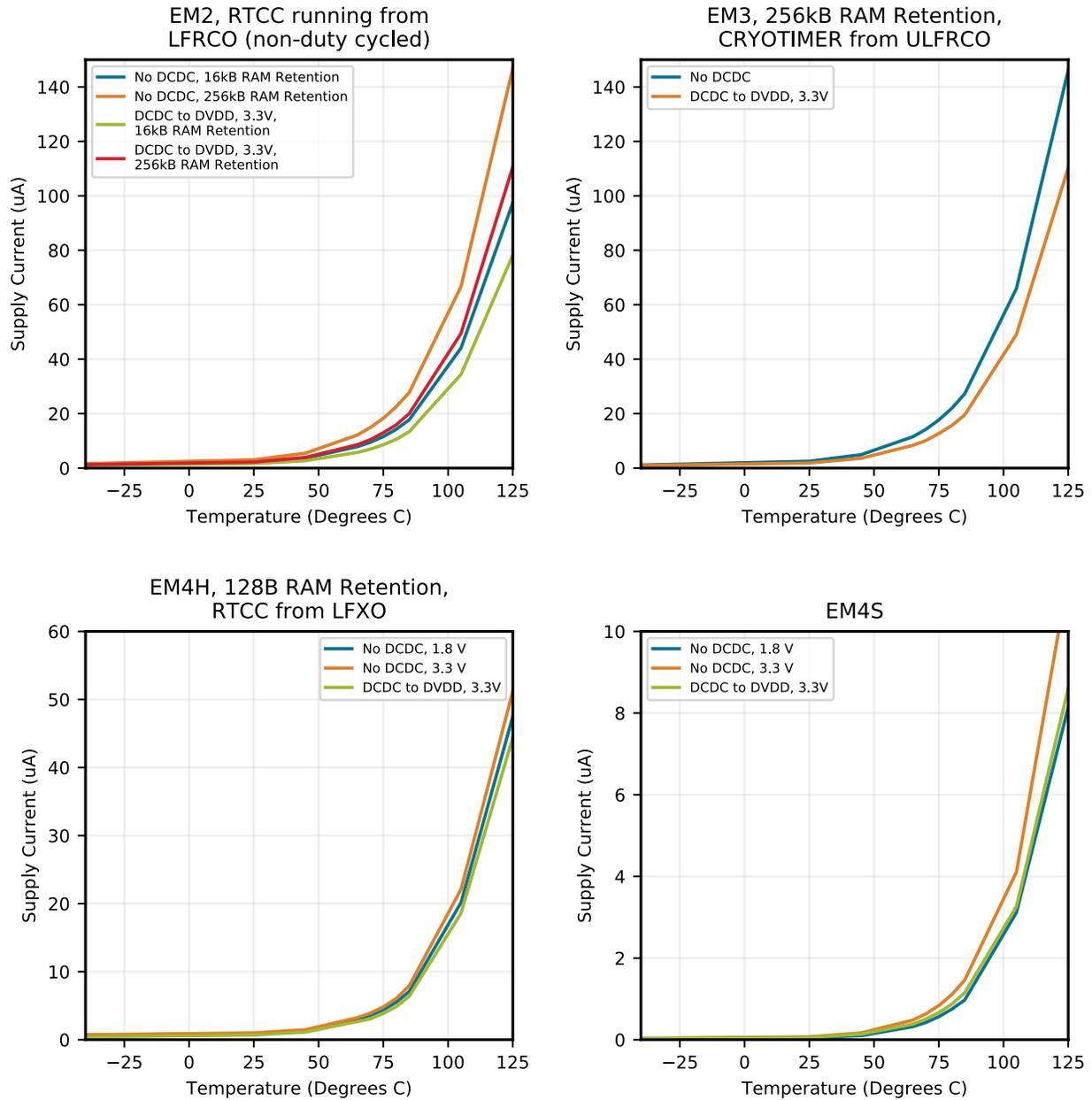


Figure 4.6. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

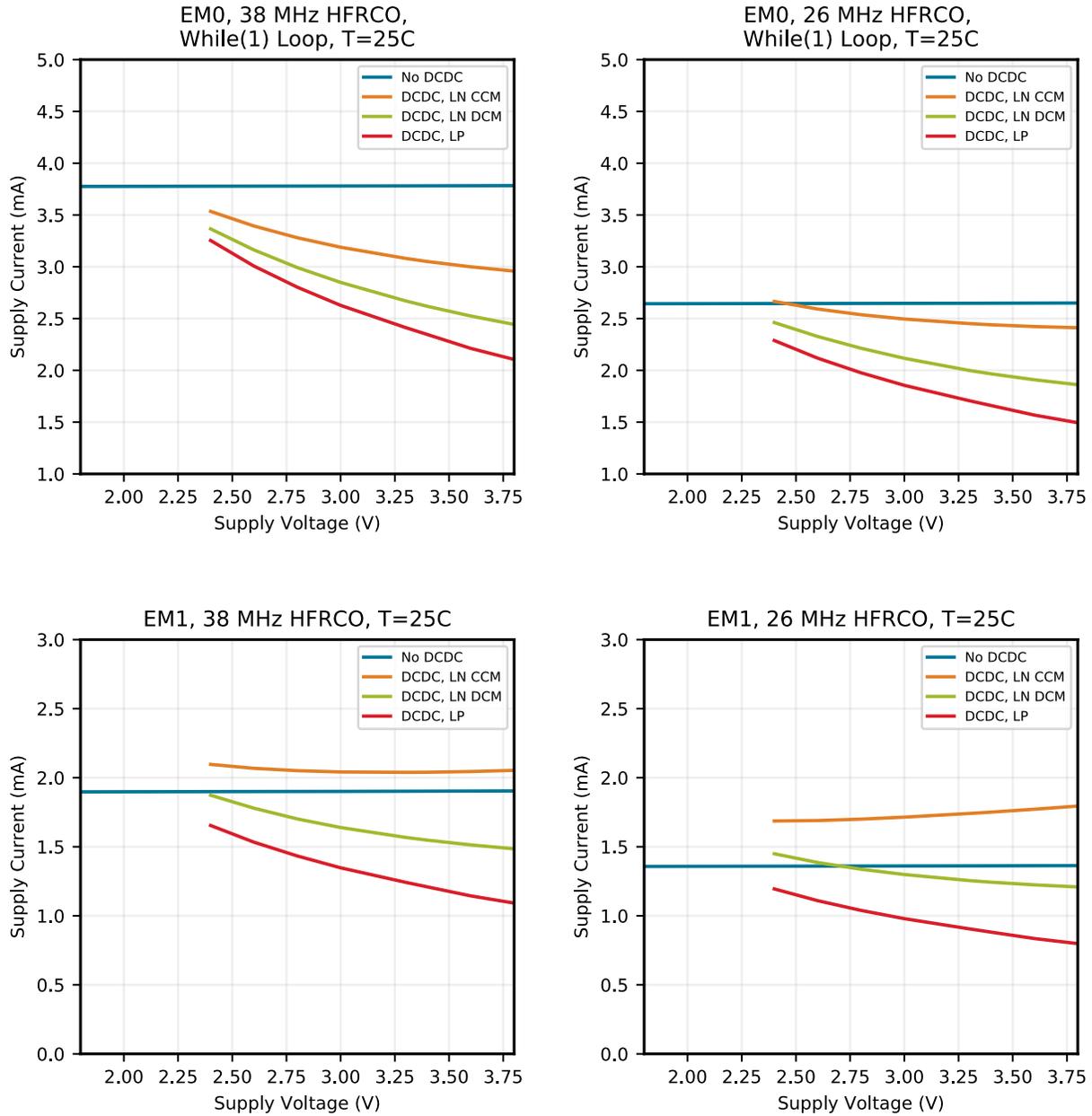


Figure 4.7. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

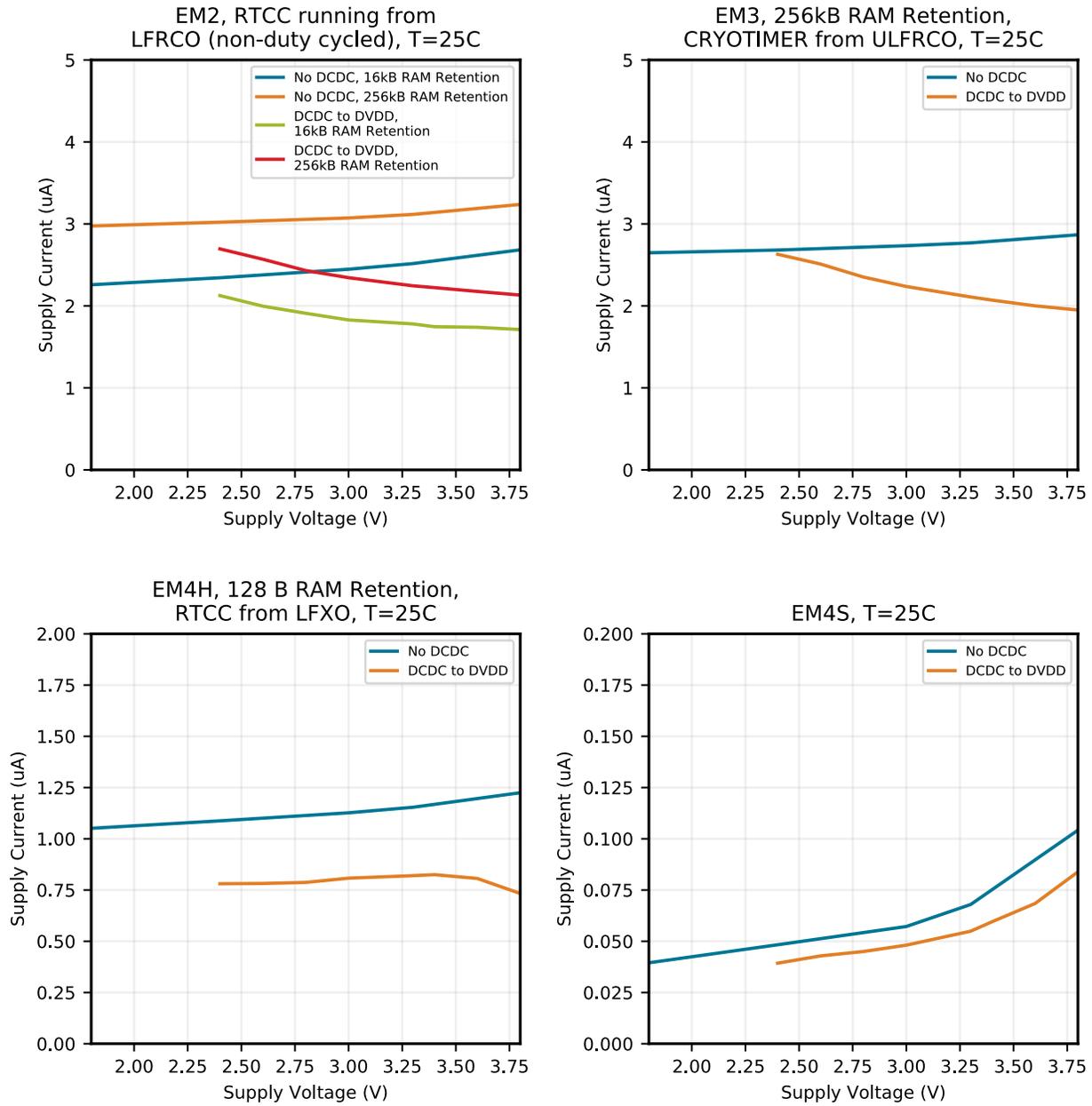


Figure 4.8. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Supply

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 μ H, CDCDC = 4.7 μ F, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

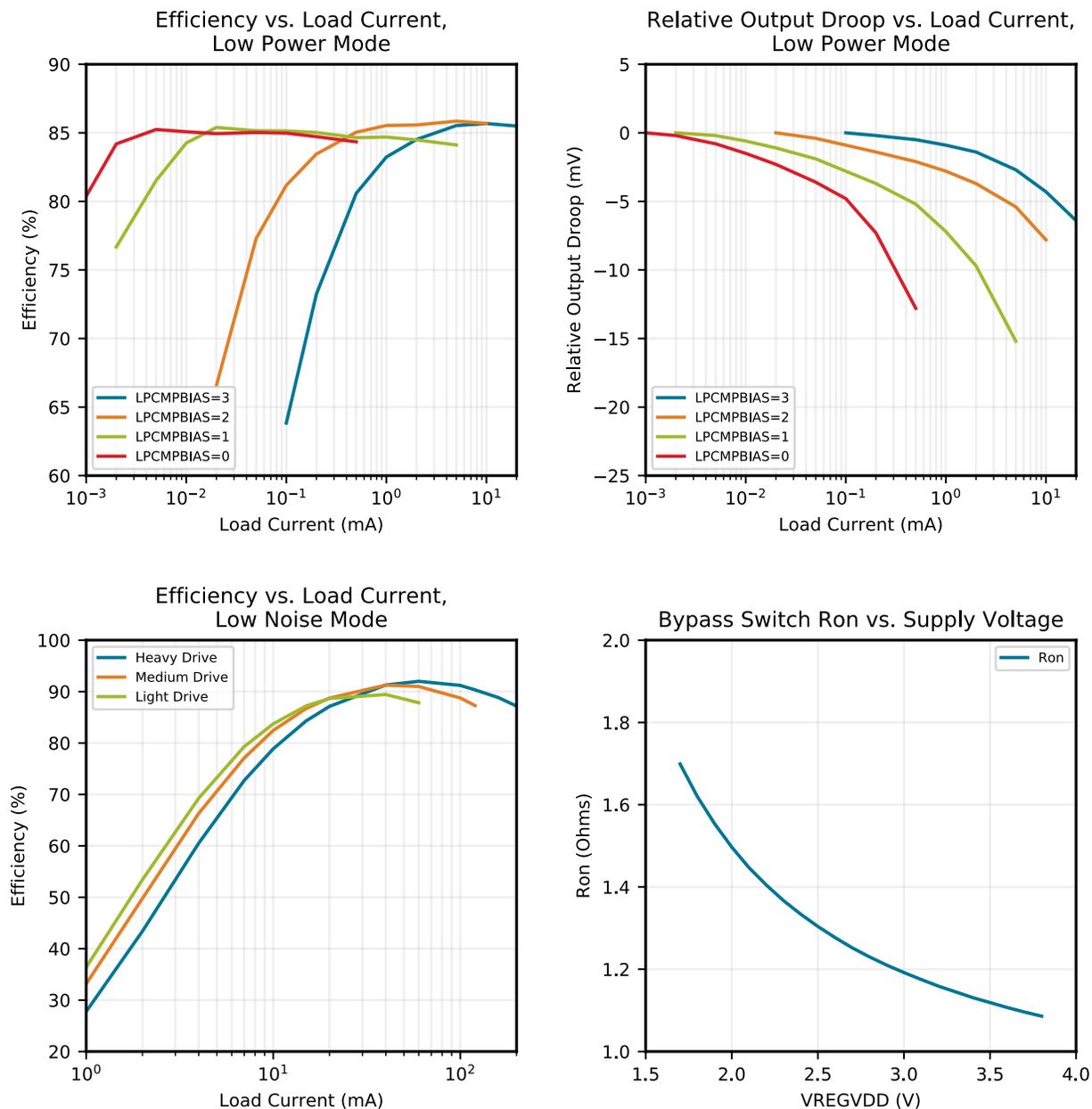


Figure 4.9. DC-DC Converter Typical Performance Characteristics

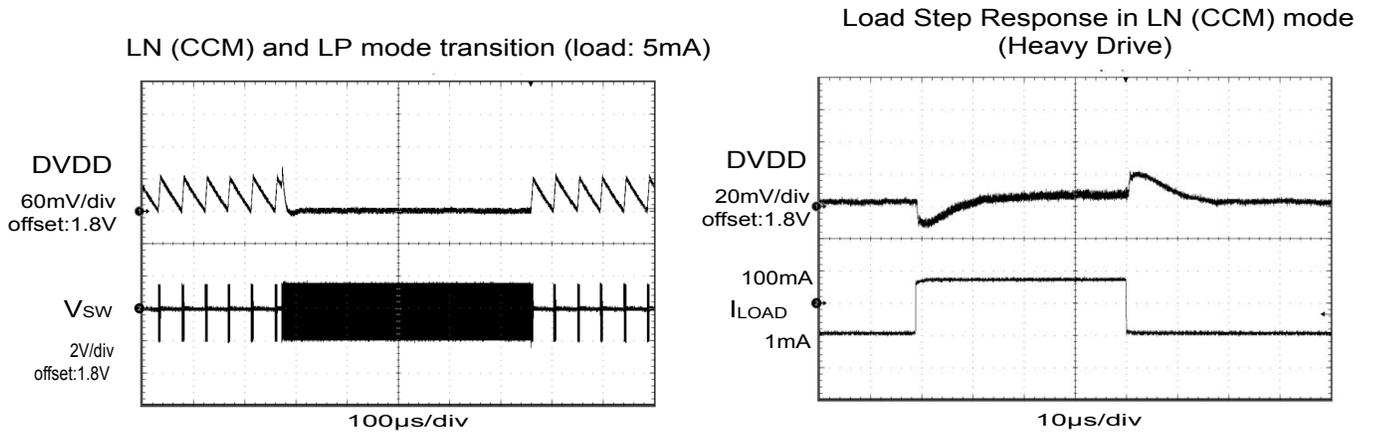


Figure 4.10. DC-DC Converter Transition Waveforms

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in [Figure 5.1 EFM32JG12 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 66](#).

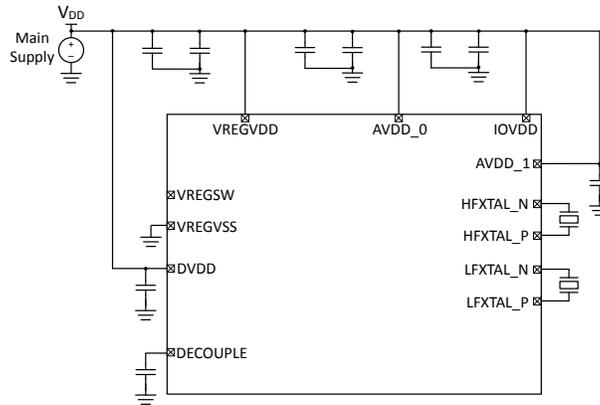


Figure 5.1. EFM32JG12 Typical Application Circuit, Direct Supply, No DC-DC Converter

A typical application circuit using the internal DC-DC converter is shown in [Figure 5.2 EFM32JG12 Typical Application Circuit Using the DC-DC Converter on page 66](#). The MCU operates from the DC-DC converter supply.

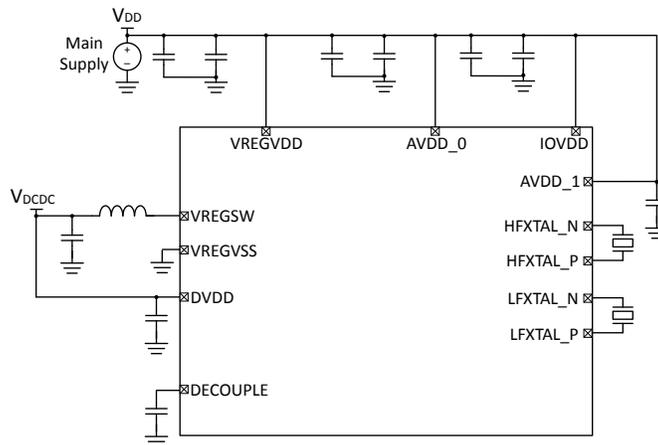


Figure 5.2. EFM32JG12 Typical Application Circuit Using the DC-DC Converter

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 EFM32JG12B5xx in BGA125 Device Pinout

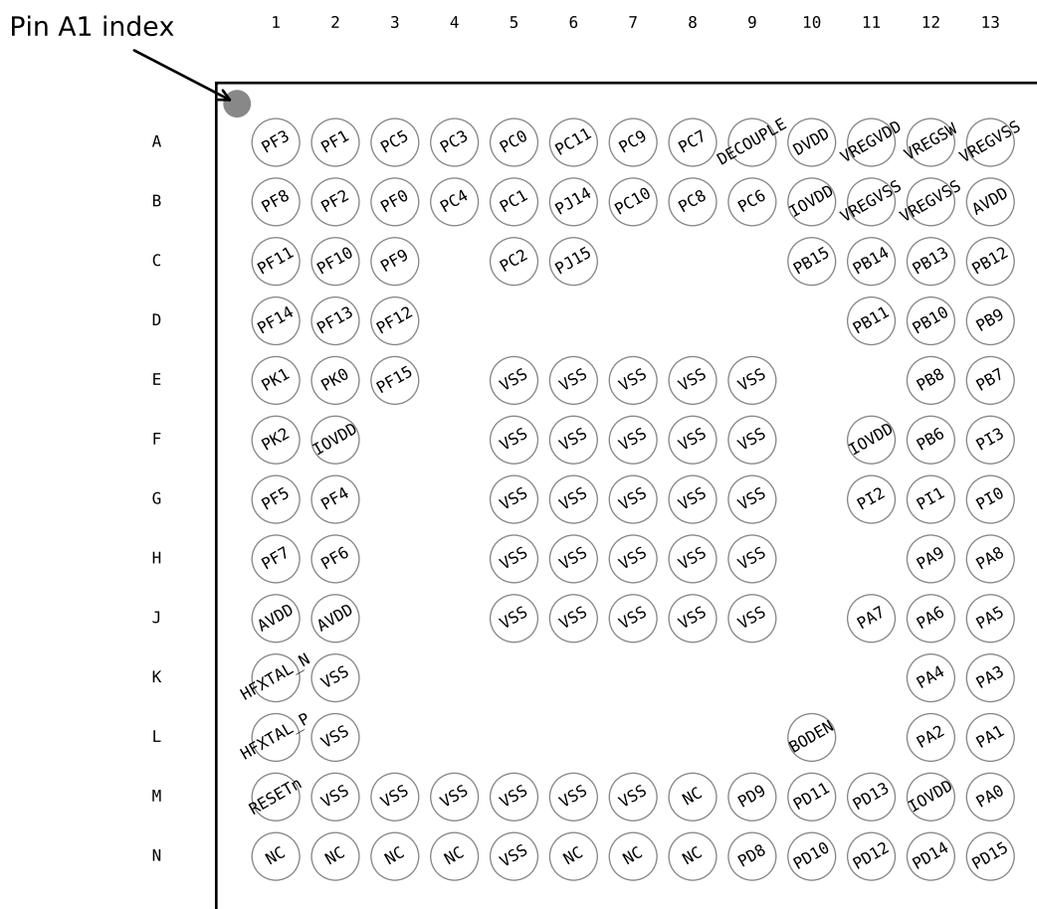


Figure 6.1. EFM32JG12B5xx in BGA125 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.3 GPIO Functionality Table](#) or [6.4 Alternate Functionality Overview](#).

Table 6.1. EFM32JG12B5xx in BGA125 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|-------------|
| PF3 | A1 | GPIO (5V) | PF1 | A2 | GPIO (5V) |
| PC5 | A3 | GPIO (5V) | PC3 | A4 | GPIO (5V) |
| PC0 | A5 | GPIO (5V) | PC11 | A6 | GPIO (5V) |
| PC9 | A7 | GPIO (5V) | PC7 | A8 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|-------------------------|--|----------|-----------------|-------------------------------|
| DECOUPLE | A9 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. | DVDD | A10 | Digital power supply. |
| VREGVDD | A11 | Voltage regulator VDD input | VREGSW | A12 | DCDC regulator switching node |
| VREGVSS | A13 B11 B12 | Voltage regulator VSS | PF8 | B1 | GPIO (5V) |
| PF2 | B2 | GPIO (5V) | PF0 | B3 | GPIO (5V) |
| PC4 | B4 | GPIO (5V) | PC1 | B5 | GPIO (5V) |
| PJ14 | B6 | GPIO (5V) | PC10 | B7 | GPIO (5V) |
| PC8 | B8 | GPIO (5V) | PC6 | B9 | GPIO (5V) |
| IOVDD | B10 F2 F11 M12 | Digital IO power supply. | AVDD | B13 J1 J2 | Analog power supply. |
| PF11 | C1 | GPIO (5V) | PF10 | C2 | GPIO (5V) |
| PF9 | C3 | GPIO (5V) | PC2 | C5 | GPIO (5V) |
| PJ15 | C6 | GPIO (5V) | PB15 | C10 | GPIO |
| PB14 | C11 | GPIO | PB13 | C12 | GPIO |
| PB12 | C13 | GPIO | PF14 | D1 | GPIO (5V) |
| PF13 | D2 | GPIO (5V) | PF12 | D3 | GPIO (5V) |
| PB11 | D11 | GPIO | PB10 | D12 | GPIO (5V) |
| PB9 | D13 | GPIO (5V) | PK1 | E1 | GPIO (5V) |
| PK0 | E2 | GPIO | PF15 | E3 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--|---|----------|--------|---|
| VSS | E5 E6 E7 E8 E9 F5 F6 F7 F8 F9 G5 G6 G7 G8 G9 H5 H6 H7 H8 H9 J5 J6 J7 J8 J9 K2 L2 M2 M3 M4 M5 M6 M7 N5 | Ground | PB8 | E12 | GPIO (5V) |
| PB7 | E13 | GPIO (5V) | PK2 | F1 | GPIO (5V) |
| PB6 | F12 | GPIO (5V) | PI3 | F13 | GPIO (5V) |
| PF5 | G1 | GPIO (5V) | PF4 | G2 | GPIO (5V) |
| PI2 | G11 | GPIO (5V) | PI1 | G12 | GPIO (5V) |
| PI0 | G13 | GPIO (5V) | PF7 | H1 | GPIO (5V) |
| PF6 | H2 | GPIO (5V) | PA9 | H12 | GPIO (5V) |
| PA8 | H13 | GPIO (5V) | PA7 | J11 | GPIO (5V) |
| PA6 | J12 | GPIO (5V) | PA5 | J13 | GPIO (5V) |
| HFXTAL_N | K1 | High Frequency Crystal input pin. | PA4 | K12 | GPIO |
| PA3 | K13 | GPIO | HFXTAL_P | L1 | High Frequency Crystal output pin. |
| BODEN | L10 | Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. | PA2 | L12 | GPIO |
| PA1 | L13 | GPIO | RESETn | M1 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--|-------------|----------|--------|-------------|
| NC | M8 N1 N2 N3 N4 N6 N7 N8 | No Connect. | PD9 | M9 | GPIO (5V) |
| PD11 | M10 | GPIO (5V) | PD13 | M11 | GPIO |
| PA0 | M13 | GPIO | PD8 | N9 | GPIO (5V) |
| PD10 | N10 | GPIO (5V) | PD12 | N11 | GPIO (5V) |
| PD14 | N12 | GPIO | PD15 | N13 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

6.2 EFM32JG12B5xx in QFN48 Device Pinout

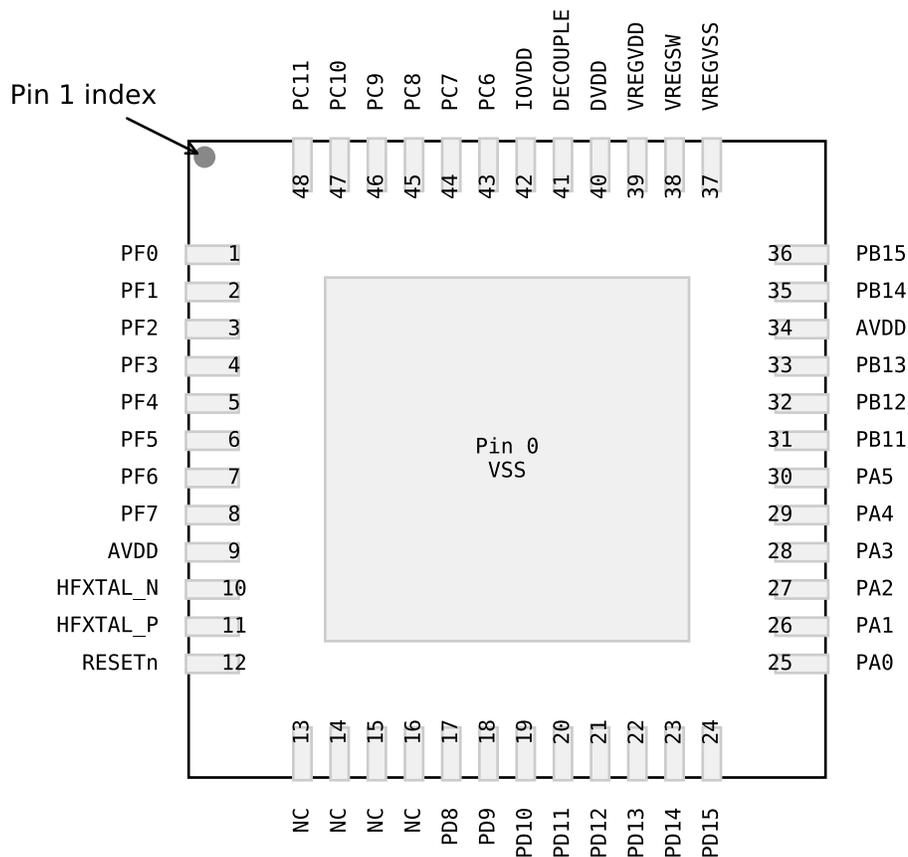


Figure 6.2. EFM32JG12B5xx in QFN48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.3 GPIO Functionality Table](#) or [6.4 Alternate Functionality Overview](#).

Table 6.2. EFM32JG12B5xx in QFN48 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-----------------------------------|----------|---------|------------------------------------|
| VSS | 0 | Ground | PF0 | 1 | GPIO (5V) |
| PF1 | 2 | GPIO (5V) | PF2 | 3 | GPIO (5V) |
| PF3 | 4 | GPIO (5V) | PF4 | 5 | GPIO (5V) |
| PF5 | 6 | GPIO (5V) | PF6 | 7 | GPIO (5V) |
| PF7 | 8 | GPIO (5V) | AVDD | 9 34 | Analog power supply. |
| HFXTAL_N | 10 | High Frequency Crystal input pin. | HFXTAL_P | 11 | High Frequency Crystal output pin. |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|----------------------|--|
| RESETn | 12 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | NC | 13 14 15 16 | No Connect. |
| PD8 | 17 | GPIO (5V) | PD9 | 18 | GPIO (5V) |
| PD10 | 19 | GPIO (5V) | PD11 | 20 | GPIO (5V) |
| PD12 | 21 | GPIO (5V) | PD13 | 22 | GPIO |
| PD14 | 23 | GPIO | PD15 | 24 | GPIO |
| PA0 | 25 | GPIO | PA1 | 26 | GPIO |
| PA2 | 27 | GPIO | PA3 | 28 | GPIO |
| PA4 | 29 | GPIO | PA5 | 30 | GPIO (5V) |
| PB11 | 31 | GPIO | PB12 | 32 | GPIO |
| PB13 | 33 | GPIO | PB14 | 35 | GPIO |
| PB15 | 36 | GPIO | VREGVSS | 37 | Voltage regulator VSS |
| VREGSW | 38 | DCDC regulator switching node | VREGVDD | 39 | Voltage regulator VDD input |
| DVDD | 40 | Digital power supply. | DECOUPLE | 41 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. |
| IOVDD | 42 | Digital IO power supply. | PC6 | 43 | GPIO (5V) |
| PC7 | 44 | GPIO (5V) | PC8 | 45 | GPIO (5V) |
| PC9 | 46 | GPIO (5V) | PC10 | 47 | GPIO (5V) |
| PC11 | 48 | GPIO (5V) | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The PD8 GPIO pin is not available (no-connect) on other device families, and should not be used if direct pin compatibility across multiple families is required.

6.3 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [6.4 Alternate Functionality Overview](#) for a list of GPIO locations available for each function.

Table 6.3. GPIO Functionality Table

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|---|--|
| | Analog | Timers | Communication | Other |
| PF3 | BUSAY BUSBX | TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 WTIM0_CDTI2 #31 WTIM1_CC0 #27 WTIM1_CC1 #25 WTIM1_CC2 #23 WTIM1_CC3 #21 LE- TIM0_OUT0 #27 LE- TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26 | US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 US2_TX #16 US2_RX #15 US2_CLK #14 US2_CS #13 US2_CTS #12 US2_RTS #11 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26 | CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI |
| PF1 | BUSAY BUSBX | TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 WTIM0_CDTI1 #31 WTIM0_CDTI2 #29 WTIM1_CC0 #25 WTIM1_CC1 #23 WTIM1_CC2 #21 WTIM1_CC3 #19 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24 | US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 US2_TX #15 US2_RX #14 US2_CLK #13 US2_CS #12 US2_CTS #11 US2_RTS #10 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24 | PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS BOOT_RX |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|--|-------|
| | Analog | Timers | Communication | Other |
| PC5 | BUSAY BUSBX | WTIM0_CC0 #25 WTIM0_CC1 #23 WTIM0_CC2 #21 WTIM0_CDTI0 #17 WTIM0_CDTI1 #15 WTIM0_CDTI2 #13 WTIM1_CC0 #9 WTIM1_CC1 #7 WTIM1_CC2 #5 WTIM1_CC3 #3 PCNT1_S0IN #18 PCNT1_S1IN #17 PCNT2_S0IN #18 PCNT2_S1IN #17 | US3_TX #23 US3_RX #22 US3_CLK #21 US3_CS #20 US3_CTS #19 US3_RTS #18 I2C1_SDA #18 I2C1_SCL #17 | |
| PC3 | BUSAY BUSBX | WTIM0_CC0 #23 WTIM0_CC1 #21 WTIM0_CC2 #19 WTIM0_CDTI0 #15 WTIM0_CDTI1 #13 WTIM0_CDTI2 #11 WTIM1_CC0 #7 WTIM1_CC1 #5 WTIM1_CC2 #3 WTIM1_CC3 #1 PCNT1_S0IN #16 PCNT1_S1IN #15 PCNT2_S0IN #16 PCNT2_S1IN #15 | US3_TX #21 US3_RX #20 US3_CLK #19 US3_CS #18 US3_CTS #17 US3_RTS #16 I2C1_SDA #16 I2C1_SCL #15 | |
| PC0 | BUSBY BUSAX | WTIM0_CC0 #20 WTIM0_CC1 #18 WTIM0_CC2 #16 WTIM0_CDTI0 #12 WTIM0_CDTI1 #10 WTIM0_CDTI2 #8 WTIM1_CC0 #4 WTIM1_CC1 #2 WTIM1_CC2 #0 PCNT1_S0IN #13 PCNT1_S1IN #12 PCNT2_S0IN #13 PCNT2_S1IN #12 | US3_TX #18 US3_RX #17 US3_CLK #16 US3_CS #15 US3_CTS #14 US3_RTS #13 I2C1_SDA #13 I2C1_SCL #12 | |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|---|--|---|
| | Analog | Timers | Communication | Other |
| PC11 | BUSAY BUSBX | TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 WTIM0_CC0 #31 WTIM0_CC1 #29 WTIM0_CC2 #27 WTIM0_CDTI0 #23 WTIM0_CDTI1 #21 WTIM0_CDTI2 #19 WTIM1_CC0 #15 WTIM1_CC1 #13 WTIM1_CC2 #11 WTIM1_CC3 #9 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 PCNT2_S0IN #20 PCNT2_S1IN #19 | US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 I2C1_SDA #20 I2C1_SCL #19 | CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3 |
| PC9 | BUSAY BUSBX | TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 WTIM0_CC0 #29 WTIM0_CC1 #27 WTIM0_CC2 #25 WTIM0_CDTI0 #21 WTIM0_CDTI1 #19 WTIM0_CDTI2 #17 WTIM1_CC0 #13 WTIM1_CC1 #11 WTIM1_CC2 #9 WTIM1_CC3 #7 LE- TIM0_OUT0 #14 LE- TIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13 | US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13 | PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14 ETM_TD2 #3 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|---|---|--|
| | Analog | Timers | Communication | Other |
| PC7 | BUSAY BUSBX | TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 WTIM0_CC0 #27 WTIM0_CC1 #25 WTIM0_CC2 #23 WTIM0_CDTI0 #19 WTIM0_CDTI1 #17 WTIM0_CDTI2 #15 WTIM1_CC0 #11 WTIM1_CC1 #9 WTIM1_CC2 #7 WTIM1_CC3 #5 LE- TIM0_OUT0 #12 LE- TIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11 | US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11 | CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12 ETM_TD0 #3 |
| PF8 | BUSBY BUSAX | WTIM1_CC1 #30 WTIM1_CC2 #28 WTIM1_CC3 #26 PCNT1_S0IN #21 PCNT1_S1IN #20 PCNT2_S0IN #21 PCNT2_S1IN #20 | US2_TX #21 US2_RX #20 US2_CLK #19 US2_CS #18 US2_CTS #17 US2_RTS #16 I2C1_SDA #21 I2C1_SCL #20 | ETM_TCLK #0 |
| PF2 | BUSBY BUSAX | TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 WTIM0_CDTI2 #30 WTIM1_CC0 #26 WTIM1_CC1 #24 WTIM1_CC2 #22 WTIM1_CC3 #20 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25 | US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25 | CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO DBG_SWO #0 GPIO_EM4WU0 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|---|---|
| | Analog | Timers | Communication | Other |
| PF0 | BUSBY BUSAX | TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 WTIM0_CDTI1 #30 WTIM0_CDTI2 #28 WTIM1_CC0 #24 WTIM1_CC1 #22 WTIM1_CC2 #20 WTIM1_CC3 #18 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23 | US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 US2_TX #14 US2_RX #13 US2_CLK #12 US2_CS #11 US2_CTS #10 US2_RTS #9 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23 | PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK BOOT_TX |
| PC4 | BUSBY BUSAX | WTIM0_CC0 #24 WTIM0_CC1 #22 WTIM0_CC2 #20 WTIM0_CDTI0 #16 WTIM0_CDTI1 #14 WTIM0_CDTI2 #12 WTIM1_CC0 #8 WTIM1_CC1 #6 WTIM1_CC2 #4 WTIM1_CC3 #2 PCNT1_S0IN #17 PCNT1_S1IN #16 PCNT2_S0IN #17 PCNT2_S1IN #16 | US3_TX #22 US3_RX #21 US3_CLK #20 US3_CS #19 US3_CTS #18 US3_RTS #17 I2C1_SDA #17 I2C1_SCL #16 | |
| PC1 | BUSAY BUSBX | WTIM0_CC0 #21 WTIM0_CC1 #19 WTIM0_CC2 #17 WTIM0_CDTI0 #13 WTIM0_CDTI1 #11 WTIM0_CDTI2 #9 WTIM1_CC0 #5 WTIM1_CC1 #3 WTIM1_CC2 #1 PCNT1_S0IN #14 PCNT1_S1IN #13 PCNT2_S0IN #14 PCNT2_S1IN #13 | US3_TX #19 US3_RX #18 US3_CLK #17 US3_CS #16 US3_CTS #15 US3_RTS #14 I2C1_SDA #14 I2C1_SCL #13 | |
| PJ14 | BUSACMP1Y BU- SACMP1X | PCNT1_S0IN #11 PCNT1_S1IN #10 PCNT2_S0IN #11 PCNT2_S1IN #10 | US3_TX #16 US3_RX #15 US3_CLK #14 US3_CS #13 US3_CTS #12 US3_RTS #11 I2C1_SDA #11 I2C1_SCL #10 | LES_ALTEX2 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|---|--|---|
| | Analog | Timers | Communication | Other |
| PC10 | BUSBY BUSAX | TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 WTIM0_CC0 #30 WTIM0_CC1 #28 WTIM0_CC2 #26 WTIM0_CDTI0 #22 WTIM0_CDTI1 #20 WTIM0_CDTI2 #18 WTIM1_CC0 #14 WTIM1_CC1 #12 WTIM1_CC2 #10 WTIM1_CC3 #8 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14 PCNT2_S0IN #19 PCNT2_S1IN #18 | US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14 I2C1_SDA #19 I2C1_SCL #18 | CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 ETM_TD3 #3 GPIO_EM4WU12 |
| PC8 | BUSBY BUSAX | TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 WTIM0_CC0 #28 WTIM0_CC1 #26 WTIM0_CC2 #24 WTIM0_CDTI0 #20 WTIM0_CDTI1 #18 WTIM0_CDTI2 #16 WTIM1_CC0 #12 WTIM1_CC1 #10 WTIM1_CC2 #8 WTIM1_CC3 #6 LE- TIM0_OUT0 #13 LE- TIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12 | US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12 | PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13 ETM_TD1 #3 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|---|--|
| | Analog | Timers | Communication | Other |
| PC6 | BUSBY BUSAX | TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 WTIM0_CC0 #26 WTIM0_CC1 #24 WTIM0_CC2 #22 WTIM0_CDTI0 #18 WTIM0_CDTI1 #16 WTIM0_CDTI2 #14 WTIM1_CC0 #10 WTIM1_CC1 #8 WTIM1_CC2 #6 WTIM1_CC3 #4 LE-TIM0_OUT0 #11 LE-TIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10 | US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10 | CMU_CLK0 #2 CMU_CLKI0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11 ETM_TCLK #3 |
| PF11 | BUSAY BUSBX | WTIM1_CC2 #31 WTIM1_CC3 #29 PCNT1_S0IN #24 PCNT1_S1IN #23 PCNT2_S0IN #24 PCNT2_S1IN #23 | US2_TX #24 US2_RX #23 US2_CLK #22 US2_CS #21 US2_CTS #20 US2_RTS #19 US3_TX #24 US3_RX #23 US3_CLK #22 US3_CS #21 US3_CTS #20 US3_RTS #19 I2C1_SDA #24 I2C1_SCL #23 | ETM_TD2 #0 |
| PF10 | BUSBY BUSAX | WTIM1_CC2 #30 WTIM1_CC3 #28 PCNT1_S0IN #23 PCNT1_S1IN #22 PCNT2_S0IN #23 PCNT2_S1IN #22 | US2_TX #23 US2_RX #22 US2_CLK #21 US2_CS #20 US2_CTS #19 US2_RTS #18 I2C1_SDA #23 I2C1_SCL #22 | ETM_TD1 #0 |
| PF9 | BUSAY BUSBX | WTIM1_CC1 #31 WTIM1_CC2 #29 WTIM1_CC3 #27 PCNT1_S0IN #22 PCNT1_S1IN #21 PCNT2_S0IN #22 PCNT2_S1IN #21 | US2_TX #22 US2_RX #21 US2_CLK #20 US2_CS #19 US2_CTS #18 US2_RTS #17 I2C1_SDA #22 I2C1_SCL #21 | ETM_TD0 #0 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|---|---|--|
| | Analog | Timers | Communication | Other |
| PC2 | BUSBY BUSAX | WTIM0_CC0 #22 WTIM0_CC1 #20 WTIM0_CC2 #18 WTIM0_CDTI0 #14 WTIM0_CDTI1 #12 WTIM0_CDTI2 #10 WTIM1_CC0 #6 WTIM1_CC1 #4 WTIM1_CC2 #2 WTIM1_CC3 #0 PCNT1_S0IN #15 PCNT1_S1IN #14 PCNT2_S0IN #15 PCNT2_S1IN #14 | US3_TX #20 US3_RX #19 US3_CLK #18 US3_CS #17 US3_CTS #16 US3_RTS #15 I2C1_SDA #15 I2C1_SCL #14 | |
| PJ15 | BUSACMP1Y BUSACMP1X | PCNT1_S0IN #12 PCNT1_S1IN #11 PCNT2_S0IN #12 PCNT2_S1IN #11 | US3_TX #17 US3_RX #16 US3_CLK #15 US3_CS #14 US3_CTS #13 US3_RTS #12 I2C1_SDA #12 I2C1_SCL #11 | LES_ALTEX3 |
| PB15 | BUSCY BUSDX LFX TAL_P | TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 WTIM0_CC0 #19 WTIM0_CC1 #17 WTIM0_CC2 #15 WTIM0_CDTI0 #11 WTIM0_CDTI1 #9 WTIM0_CDTI2 #7 WTIM1_CC0 #3 WTIM1_CC1 #1 LE-TIM0_OUT0 #10 LE-TIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9 | US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9 | CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10 |
| PB14 | BUSDY BUSCX LFX TAL_N | TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 WTIM0_CC0 #18 WTIM0_CC1 #16 WTIM0_CC2 #14 WTIM0_CDTI0 #10 WTIM0_CDTI1 #8 WTIM0_CDTI2 #6 WTIM1_CC0 #2 WTIM1_CC1 #0 LE-TIM0_OUT0 #9 LE-TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8 | US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8 | CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|---|---|
| | Analog | Timers | Communication | Other |
| PB13 | BUSCY BUSDX OPA2_N | TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 WTIM0_CC0 #17 WTIM0_CC1 #15 WTIM0_CC2 #13 WTIM0_CDTI0 #9 WTIM0_CDTI1 #7 WTIM0_CDTI2 #5 WTIM1_CC0 #1 LE-TIM0_OUT0 #8 LE-TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7 | US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7 | CMU_CLKI0 #0 PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9 |
| PB12 | BUSDY BUSCX OPA2_OUT | TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 WTIM0_CC0 #16 WTIM0_CC1 #14 WTIM0_CC2 #12 WTIM0_CDTI0 #8 WTIM0_CDTI1 #6 WTIM0_CDTI2 #4 WTIM1_CC0 #0 LE-TIM0_OUT0 #7 LE-TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6 | US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6 | PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7 |
| PF14 | BUSBY BUSAX | PCNT1_S0IN #27 PCNT1_S1IN #26 PCNT2_S0IN #27 PCNT2_S1IN #26 | US2_TX #27 US2_RX #26 US2_CLK #25 US2_CS #24 US2_CTS #23 US2_RTS #22 US3_TX #27 US3_RX #26 US3_CLK #25 US3_CS #24 US3_CTS #23 US3_RTS #22 I2C1_SDA #27 I2C1_SCL #26 | |
| PF13 | BUSAY BUSBX | WTIM1_CC3 #31 PCNT1_S0IN #26 PCNT1_S1IN #25 PCNT2_S0IN #26 PCNT2_S1IN #25 | US2_TX #26 US2_RX #25 US2_CLK #24 US2_CS #23 US2_CTS #22 US2_RTS #21 US3_TX #26 US3_RX #25 US3_CLK #24 US3_CS #23 US3_CTS #22 US3_RTS #21 I2C1_SDA #26 I2C1_SCL #25 | |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|---|--|--|
| | Analog | Timers | Communication | Other |
| PF12 | BUSBY BUSAX | WTIM1_CC3 #30 PCNT1_S0IN #25 PCNT1_S1IN #24 PCNT2_S0IN #25 PCNT2_S1IN #24 | US2_TX #25 US2_RX #24 US2_CLK #23 US2_CS #22 US2_CTS #21 US2_RTS #20 US3_TX #25 US3_RX #24 US3_CLK #23 US3_CS #22 US3_CTS #21 US3_RTS #20 I2C1_SDA #25 I2C1_SCL #24 | ETM_TD3 #0 |
| PB11 | BUSCY BUSDX OPA2_P | TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 WTIM0_CC0 #15 WTIM0_CC1 #13 WTIM0_CC2 #11 WTIM0_CDTI0 #7 WTIM0_CDTI1 #5 WTIM0_CDTI2 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5 | US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 US3_TX #15 US3_RX #14 US3_CLK #13 US3_CS #12 US3_CTS #11 US3_RTS #10 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5 | PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6 |
| PB10 | OPA2_OUTALT #1 BUSDY BUSCX | WTIM0_CC0 #14 WTIM0_CC1 #12 WTIM0_CC2 #10 WTIM0_CDTI0 #6 WTIM0_CDTI1 #4 WTIM0_CDTI2 #2 PCNT1_S0IN #10 PCNT1_S1IN #9 PCNT2_S0IN #10 PCNT2_S1IN #9 | US2_TX #13 US2_RX #12 US2_CLK #11 US2_CS #10 US2_CTS #9 US2_RTS #8 US3_TX #14 US3_RX #13 US3_CLK #12 US3_CS #11 US3_CTS #10 US3_RTS #9 I2C1_SDA #10 I2C1_SCL #9 | |
| PB9 | OPA2_OUTALT #0 BUSCY BUSDX | WTIM0_CC0 #13 WTIM0_CC1 #11 WTIM0_CC2 #9 WTIM0_CDTI0 #5 WTIM0_CDTI1 #3 WTIM0_CDTI2 #1 PCNT1_S0IN #9 PCNT1_S1IN #8 PCNT2_S0IN #9 PCNT2_S1IN #8 | US2_TX #12 US2_RX #11 US2_CLK #10 US2_CS #9 US2_CTS #8 US2_RTS #7 US3_TX #13 US3_RX #12 US3_CLK #11 US3_CS #10 US3_CTS #9 US3_RTS #8 I2C1_SDA #9 I2C1_SCL #8 | |
| PK1 | | PCNT1_S0IN #30 PCNT1_S1IN #29 PCNT2_S0IN #30 PCNT2_S1IN #29 | US2_TX #30 US2_RX #29 US2_CLK #28 US2_CS #27 US2_CTS #26 US2_RTS #25 US3_TX #30 US3_RX #29 US3_CLK #28 US3_CS #27 US3_CTS #26 US3_RTS #25 I2C1_SDA #30 I2C1_SCL #29 | |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|---|-------------------------|
| | Analog | Timers | Communication | Other |
| PK0 | IDAC0_OUT | PCNT1_S0IN #29 PCNT1_S1IN #28 PCNT2_S0IN #29 PCNT2_S1IN #28 | US2_TX #29 US2_RX #28 US2_CLK #27 US2_CS #26 US2_CTS #25 US2_RTS #24 US3_TX #29 US3_RX #28 US3_CLK #27 US3_CS #26 US3_CTS #25 US3_RTS #24 I2C1_SDA #29 I2C1_SCL #28 | |
| PF15 | BUSAY BUSBX | PCNT1_S0IN #28 PCNT1_S1IN #27 PCNT2_S0IN #28 PCNT2_S1IN #27 | US2_TX #28 US2_RX #27 US2_CLK #26 US2_CS #25 US2_CTS #24 US2_RTS #23 US3_TX #28 US3_RX #27 US3_CLK #26 US3_CS #25 US3_CTS #24 US3_RTS #23 I2C1_SDA #28 I2C1_SCL #27 | |
| PB8 | BUSDY BUSCX | WTIM0_CC0 #12 WTIM0_CC1 #10 WTIM0_CC2 #8 WTIM0_CDTI0 #4 WTIM0_CDTI1 #2 WTIM0_CDTI2 #0 PCNT1_S0IN #8 PCNT1_S1IN #7 PCNT2_S0IN #8 PCNT2_S1IN #7 | US2_TX #11 US2_RX #10 US2_CLK #9 US2_CS #8 US2_CTS #7 US2_RTS #6 US3_TX #12 US3_RX #11 US3_CLK #10 US3_CS #9 US3_CTS #8 US3_RTS #7 I2C1_SDA #8 I2C1_SCL #7 | ETM_TD3 #2 |
| PB7 | BUSCY BUSDX | WTIM0_CC0 #11 WTIM0_CC1 #9 WTIM0_CC2 #7 WTIM0_CDTI0 #3 WTIM0_CDTI1 #1 PCNT1_S0IN #7 PCNT1_S1IN #6 PCNT2_S0IN #7 PCNT2_S1IN #6 | US2_TX #10 US2_RX #9 US2_CLK #8 US2_CS #7 US2_CTS #6 US2_RTS #5 US3_TX #11 US3_RX #10 US3_CLK #9 US3_CS #8 US3_CTS #7 US3_RTS #6 I2C1_SDA #7 I2C1_SCL #6 | ETM_TD2 #2 |
| PK2 | | PCNT1_S0IN #31 PCNT1_S1IN #30 PCNT2_S0IN #31 PCNT2_S1IN #30 | US2_TX #31 US2_RX #30 US2_CLK #29 US2_CS #28 US2_CTS #27 US2_RTS #26 US3_TX #31 US3_RX #30 US3_CLK #29 US3_CS #28 US3_CTS #27 US3_RTS #26 I2C1_SDA #31 I2C1_SCL #30 | |
| PB6 | BUSDY BUSCX | WTIM0_CC0 #10 WTIM0_CC1 #8 WTIM0_CC2 #6 WTIM0_CDTI0 #2 WTIM0_CDTI1 #0 PCNT1_S0IN #6 PCNT1_S1IN #5 PCNT2_S0IN #6 PCNT2_S1IN #5 | US2_TX #9 US2_RX #8 US2_CLK #7 US2_CS #6 US2_CTS #5 US2_RTS #4 US3_TX #10 US3_RX #9 US3_CLK #8 US3_CS #7 US3_CTS #6 US3_RTS #5 I2C1_SDA #6 I2C1_SCL #5 | CMU_CLKI0 #3 ETM_TD1 #2 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|--|--|
| | Analog | Timers | Communication | Other |
| PI3 | BUSADC0Y BUSADC0X | PCNT1_S0IN #5 PCNT1_S1IN #4 PCNT2_S0IN #5 PCNT2_S1IN #4 | US2_TX #8 US2_RX #7 US2_CLK #6 US2_CS #5 US2_CTS #4 US2_RTS #3 US3_TX #9 US3_RX #8 US3_CLK #7 US3_CS #6 US3_CTS #5 US3_RTS #4 I2C1_SDA #5 I2C1_SCL #4 | LES_ALTEX7 ETM_TD0 #2 |
| PF5 | BUSAY BUSBX | TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 WTIM1_CC0 #29 WTIM1_CC1 #27 WTIM1_CC2 #25 WTIM1_CC3 #23 LE- TIM0_OUT0 #29 LE- TIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28 | US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 US2_TX #18 US2_RX #17 US2_CLK #16 US2_CS #15 US2_CTS #14 US2_RTS #13 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28 | PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29 |
| PF4 | BUSBY BUSAX | TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 WTIM1_CC0 #28 WTIM1_CC1 #26 WTIM1_CC2 #24 WTIM1_CC3 #22 LE- TIM0_OUT0 #28 LE- TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27 | US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 US2_TX #17 US2_RX #16 US2_CLK #15 US2_CS #14 US2_CTS #13 US2_RTS #12 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27 | PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28 |
| PI2 | BUSADC0Y BUSADC0X | PCNT1_S0IN #4 PCNT1_S1IN #3 PCNT2_S0IN #4 PCNT2_S1IN #3 | US2_TX #7 US2_RX #6 US2_CLK #5 US2_CS #4 US2_CTS #3 US2_RTS #2 US3_TX #8 US3_RX #7 US3_CLK #6 US3_CS #5 US3_CTS #4 US3_RTS #3 I2C1_SDA #4 I2C1_SCL #3 | LES_ALTEX6 ETM_TCLK #2 |
| PI1 | BUSADC0Y BUSADC0X | | US2_TX #6 US2_RX #5 US2_CLK #4 US2_CS #3 US2_CTS #2 US2_RTS #1 | LES_ALTEX5 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|--|--|
| | Analog | Timers | Communication | Other |
| PI0 | BUSADC0Y BUSADC0X | | US2_TX #5 US2_RX #4 US2_CLK #3 US2_CS #2 US2_CTS #1 US2_RTS #0 | LES_ALTEX4 |
| PF7 | BUSAY BUSBX | TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC0 #31 WTIM1_CC1 #29 WTIM1_CC2 #27 WTIM1_CC3 #25 LE- TIM0_OUT0 #31 LE- TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19 | US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30 | CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1 |
| PF6 | BUSBY BUSAX | TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 WTIM1_CC0 #30 WTIM1_CC1 #28 WTIM1_CC2 #26 WTIM1_CC3 #24 LE- TIM0_OUT0 #30 LE- TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 PCNT1_S0IN #19 PCNT1_S1IN #18 | US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29 | CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30 |
| PA9 | BUSACMP0Y BU- SACMP0X | WTIM0_CC0 #9 WTIM0_CC1 #7 WTIM0_CC2 #5 WTIM0_CDTI0 #1 PCNT1_S0IN #3 PCNT1_S1IN #2 PCNT2_S0IN #3 PCNT2_S1IN #2 | US2_TX #4 US2_RX #3 US2_CLK #2 US2_CS #1 US2_CTS #0 US2_RTS #31 I2C1_SDA #3 I2C1_SCL #2 | LES_ALTEX1 ETM_TD3 #1 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|---|---|--|
| | Analog | Timers | Communication | Other |
| PA8 | BUSACMP0Y BU-SACMP0X | WTIM0_CC0 #8 WTIM0_CC1 #6 WTIM0_CC2 #4 WTIM0_CDTI0 #0 PCNT1_S0IN #2 PCNT1_S1IN #1 PCNT2_S0IN #2 PCNT2_S1IN #1 | US2_TX #3 US2_RX #2 US2_CLK #1 US2_CS #0 US2_CTS #31 US2_RTS #30 I2C1_SDA #2 I2C1_SCL #1 | LES_ALTEX0 ETM_TD2 #1 |
| PA7 | BUSCY BUSDX | WTIM0_CC0 #7 WTIM0_CC1 #5 WTIM0_CC2 #3 PCNT1_S0IN #1 PCNT1_S1IN #0 PCNT2_S0IN #1 PCNT2_S1IN #0 | US2_TX #2 US2_RX #1 US2_CLK #0 US2_CS #31 US2_CTS #30 US2_RTS #29 I2C1_SDA #1 I2C1_SCL #0 | LES_CH15 ETM_TD1 #1 |
| PA6 | BUSDY BUSCX | WTIM0_CC0 #6 WTIM0_CC1 #4 WTIM0_CC2 #2 PCNT1_S0IN #0 PCNT1_S1IN #31 PCNT2_S0IN #0 PCNT2_S1IN #31 | US2_TX #1 US2_RX #0 US2_CLK #31 US2_CS #30 US2_CTS #29 US2_RTS #28 I2C1_SDA #0 I2C1_SCL #31 | LES_CH14 ETM_TD0 #1 |
| PA5 | VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSCY BUSDX | TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 WTIM0_CC0 #5 WTIM0_CC1 #3 WTIM0_CC2 #1 LE-TIM0_OUT0 #5 LE-TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4 | US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 US2_TX #0 US2_RX #31 US2_CLK #30 US2_CS #29 US2_CTS #28 US2_RTS #27 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4 | CMU_CLKI0 #4 PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5 LES_CH13 ETM_TCLK #1 |
| PA4 | VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSDY BUSCX OPA0_N | TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 WTIM0_CC0 #4 WTIM0_CC1 #2 WTIM0_CC2 #0 LE-TIM0_OUT0 #4 LE-TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3 | US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3 | PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4 LES_CH12 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|--|--|---|
| | Analog | Timers | Communication | Other |
| PA3 | BUSCY BUSDX VDAC0_OUT0 / OPA0_OUT | TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 WTIM0_CC0 #3 WTIM0_CC1 #1 LE- TIM0_OUT0 #3 LE- TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2 | US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2 | PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 LES_CH11 GPIO_EM4WU8 |
| PA2 | VDAC0_OUT1ALT / OPA1_OUTALT #1 BUS- DY BUSCX OPA0_P | TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 WTIM0_CC0 #2 WTIM0_CC1 #0 LE- TIM0_OUT0 #2 LE- TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1 | US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1 | PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2 LES_CH10 |
| PA1 | BUSCY BUSDX ADC0_EXTP VDAC0_EXT | TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 WTIM0_CC0 #1 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0 | US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0 | CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 LES_CH9 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|---|---|--|
| | Analog | Timers | Communication | Other |
| PD9 | BUSCY BUSDX | TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 WTIM0_CC1 #31 WTIM0_CC2 #29 WTIM0_CDTI0 #25 WTIM0_CDTI1 #23 WTIM0_CDTI2 #21 WTIM1_CC0 #17 WTIM1_CC1 #15 WTIM1_CC2 #13 WTIM1_CC3 #11 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16 | US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 US3_TX #1 US3_RX #0 US3_CLK #31 US3_CS #30 US3_CTS #29 US3_RTS #28 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16 | CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 LES_CH1 |
| PD11 | BUSCY BUSDX | TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 WTIM0_CC2 #31 WTIM0_CDTI0 #27 WTIM0_CDTI1 #25 WTIM0_CDTI2 #23 WTIM1_CC0 #19 WTIM1_CC1 #17 WTIM1_CC2 #15 WTIM1_CC3 #13 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18 | US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 US3_TX #3 US3_RX #2 US3_CLK #1 US3_CS #0 US3_CTS #31 US3_RTS #30 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18 | PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 LES_CH3 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|--|---|--|--|
| | Analog | Timers | Communication | Other |
| PD13 | VDAC0_OUT0ALT / OPA0_OUTALT #1 BUS-CY BUSDX OPA1_P | TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 WTIM1_CC0 #21 WTIM1_CC1 #19 WTIM1_CC2 #17 WTIM1_CC3 #15 LE-TIM0_OUT0 #21 LE-TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20 | US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 US3_TX #5 US3_RX #4 US3_CLK #3 US3_CS #2 US3_CTS #1 US3_RTS #0 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20 | PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5 |
| PA0 | BUSDY BUSCX ADC0_EXTN | TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31 | US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31 | CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8 |
| PD8 | BUSDY BUSCX | WTIM0_CC1 #30 WTIM0_CC2 #28 WTIM0_CDTI0 #24 WTIM0_CDTI1 #22 WTIM0_CDTI2 #20 WTIM1_CC0 #16 WTIM1_CC1 #14 WTIM1_CC2 #12 WTIM1_CC3 #10 | US3_TX #0 US3_RX #31 US3_CLK #30 US3_CS #29 US3_CTS #28 US3_RTS #27 | LES_CH0 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|--|--|--|--|
| | Analog | Timers | Communication | Other |
| PD10 | BUSDY BUSCX | TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 WTIM0_CC2 #30 WTIM0_CDTI0 #26 WTIM0_CDTI1 #24 WTIM0_CDTI2 #22 WTIM1_CC0 #18 WTIM1_CC1 #16 WTIM1_CC2 #14 WTIM1_CC3 #12 LE- TIM0_OUT0 #18 LE- TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17 | US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 US3_TX #2 US3_RX #1 US3_CLK #0 US3_CS #31 US3_CTS #30 US3_RTS #29 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17 | CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18 LES_CH2 |
| PD12 | VDAC0_OUT1ALT / OPA1_OUTALT #0 BUS- DY BUSCX | TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 WTIM0_CDTI0 #28 WTIM0_CDTI1 #26 WTIM0_CDTI2 #24 WTIM1_CC0 #20 WTIM1_CC1 #18 WTIM1_CC2 #16 WTIM1_CC3 #14 LE- TIM0_OUT0 #20 LE- TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19 | US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 US3_TX #4 US3_RX #3 US3_CLK #2 US3_CS #1 US3_CTS #0 US3_RTS #31 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19 | PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 LES_CH4 |

| GPIO Name | Pin Alternate Functionality / Description | | | |
|-----------|---|---|---|--|
| | Analog | Timers | Communication | Other |
| PD14 | BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT | TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 WTIM1_CC0 #22 WTIM1_CC1 #20 WTIM1_CC2 #18 WTIM1_CC3 #16 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21 | US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 US3_TX #6 US3_RX #5 US3_CLK #4 US3_CS #3 US3_CTS #2 US3_RTS #1 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21 | CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4 |
| PD15 | VDAC0_OUT0ALT / OPA0_OUTALT #2 BUS- CY BUSDX OPA1_N | TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI1 #29 WTIM0_CDTI2 #27 WTIM1_CC0 #23 WTIM1_CC1 #21 WTIM1_CC2 #19 WTIM1_CC3 #17 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22 | US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 US3_TX #7 US3_RX #6 US3_CLK #5 US3_CS #4 US3_CTS #3 US3_RTS #2 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22 | CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2 |

6.4 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to [6.3 GPIO Functionality Table](#) for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.4. Alternate Functionality Overview

| Alternate Functionality | LOCATION | | | | | | | | Description |
|----------------------------|--|--|---|---|---|--|--|--|---|
| | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | |
| ACMP0_O | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Analog comparator ACMP0, digital output. |
| ACMP1_O | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Analog comparator ACMP1, digital output. |
| ADC0_EXTN | 0: PA0 | | | | | | | | Analog to digital converter ADC0 external reference input negative pin. |
| ADC0_EXTP | 0: PA1 | | | | | | | | Analog to digital converter ADC0 external reference input positive pin. |
| BOOT_RX | 0: PF1 | | | | | | | | Bootloader RX. |
| BOOT_TX | 0: PF0 | | | | | | | | Bootloader TX. |
| CMU_CLK0 | 0: PA1 1: PB15 2: PC6 3: PC11 | 4: PD9 5: PD14 6: PF2 7: PF7 | | | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | 0: PA0 1: PB14 2: PC7 3: PC10 | 4: PD10 5: PD15 6: PF3 7: PF6 | | | | | | | Clock Management Unit, clock output number 1. |
| CMU_CLKI0 | 0: PB13 1: PF7 2: PC6 3: PB6 | 4: PA5 | | | | | | | Clock Management Unit, clock input number 0. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|-------|--------|---------|---------|---------|---------|---------|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| DBG_SWCLKTCK | 0: PF0 | | | | | | | | <p>Debug-interface Serial Wire clock input and JTAG Test Clock.</p> <p>Note that this function is enabled to the pin out of reset, and has a built-in pull down.</p> |
| DBG_SWDIOTMS | 0: PF1 | | | | | | | | <p>Debug-interface Serial Wire data input / output and JTAG Test Mode Select.</p> <p>Note that this function is enabled to the pin out of reset, and has a built-in pull up.</p> |
| DBG_SWO | 0: PF2 1: PB13 2: PD15 3: PC11 | | | | | | | | <p>Debug-interface Serial Wire viewer Output.</p> <p>Note that this function is not enabled after reset, and must be enabled by software to be used.</p> |
| DBG_TDI | 0: PF3 | | | | | | | | <p>Debug-interface JTAG Test Data In.</p> <p>Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.</p> |
| DBG_TDO | 0: PF2 | | | | | | | | <p>Debug-interface JTAG Test Data Out.</p> <p>Note that this function becomes available after the first valid JTAG command is received.</p> |
| ETM_TCLK | 0: PF8 1: PA5 2: PI2 3: PC6 | | | | | | | | <p>Embedded Trace Module ETM clock .</p> |

| Alternate | LOCATION | | | | | | | | |
|---------------|--|---|---|--|---|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| ETM_TD0 | 0: PF9 1: PA6 2: PI3 3: PC7 | | | | | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | 0: PF10 1: PA7 2: PB6 3: PC8 | | | | | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | 0: PF11 1: PA8 2: PB7 3: PC9 | | | | | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | 0: PF12 1: PA9 2: PB8 3: PC10 | | | | | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | 0: PF2 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | 0: PF7 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | 0: PD14 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU8 | 0: PA3 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU9 | 0: PB13 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU12 | 0: PC10 | | | | | | | | Pin can be used to wake the system up from EM4 |
| I2C0_SCL | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | I2C0 Serial Data input / output. |
| I2C1_SCL | 0: PA7 1: PA8 2: PA9 3: PI2 | 4: PI3 5: PB6 6: PB7 7: PB8 | 8: PB9 9: PB10 10: PJ14 11: PJ15 | 12: PC0 13: PC1 14: PC2 15: PC3 | 16: PC4 17: PC5 18: PC10 19: PC11 | 20: PF8 21: PF9 22: PF10 23: PF11 | 24: PF12 25: PF13 26: PF14 27: PF15 | 28: PK0 29: PK1 30: PK2 31: PA6 | I2C1 Serial Clock Line input / output. |

| Alternate | LOCATION | | | | | | | | Description |
|------------|--------------------------------------|--------------------------------------|--|---|---|--|--|---|------------------------------------|
| | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | |
| I2C1_SDA | 0: PA6 1: PA7 2: PA8 3: PA9 | 4: PI2 5: PI3 6: PB6 7: PB7 | 8: PB8 9: PB9 10: PB10 11: PJ14 | 12: PJ15 13: PC0 14: PC1 15: PC2 | 16: PC3 17: PC4 18: PC5 19: PC10 | 20: PC11 21: PF8 22: PF9 23: PF10 | 24: PF11 25: PF12 26: PF13 27: PF14 | 28: PF15 29: PK0 30: PK1 31: PK2 | I2C1 Serial Data input / output. |
| IDAC0_OUT | 0: PK0 | | | | | | | | IDAC0 output. |
| LES_ALTEX0 | 0: PA8 | | | | | | | | LESENSE alternate excite output 0. |
| LES_ALTEX1 | 0: PA9 | | | | | | | | LESENSE alternate excite output 1. |
| LES_ALTEX2 | 0: PJ14 | | | | | | | | LESENSE alternate excite output 2. |
| LES_ALTEX3 | 0: PJ15 | | | | | | | | LESENSE alternate excite output 3. |
| LES_ALTEX4 | 0: PI0 | | | | | | | | LESENSE alternate excite output 4. |
| LES_ALTEX5 | 0: PI1 | | | | | | | | LESENSE alternate excite output 5. |
| LES_ALTEX6 | 0: PI2 | | | | | | | | LESENSE alternate excite output 6. |
| LES_ALTEX7 | 0: PI3 | | | | | | | | LESENSE alternate excite output 7. |
| LES_CH0 | 0: PD8 | | | | | | | | LESENSE channel 0. |
| LES_CH1 | 0: PD9 | | | | | | | | LESENSE channel 1. |
| LES_CH2 | 0: PD10 | | | | | | | | LESENSE channel 2. |

| Alternate | LOCATION | | | | | | | | Description |
|-----------|----------|-------|--------|---------|---------|---------|---------|---------|---------------------|
| | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | |
| LES_CH3 | 0: PD11 | | | | | | | | LESENSE channel 3. |
| LES_CH4 | 0: PD12 | | | | | | | | LESENSE channel 4. |
| LES_CH5 | 0: PD13 | | | | | | | | LESENSE channel 5. |
| LES_CH6 | 0: PD14 | | | | | | | | LESENSE channel 6. |
| LES_CH7 | 0: PD15 | | | | | | | | LESENSE channel 7. |
| LES_CH8 | 0: PA0 | | | | | | | | LESENSE channel 8. |
| LES_CH9 | 0: PA1 | | | | | | | | LESENSE channel 9. |
| LES_CH10 | 0: PA2 | | | | | | | | LESENSE channel 10. |
| LES_CH11 | 0: PA3 | | | | | | | | LESENSE channel 11. |
| LES_CH12 | 0: PA4 | | | | | | | | LESENSE channel 12. |
| LES_CH13 | 0: PA5 | | | | | | | | LESENSE channel 13. |
| LES_CH14 | 0: PA6 | | | | | | | | LESENSE channel 14. |
| LES_CH15 | 0: PA7 | | | | | | | | LESENSE channel 15. |

| Alternate | LOCATION | | | | | | | | Description |
|-------------|--------------------------------------|---|---|--|---|--|--|--|---|
| | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | |
| LETIM0_OUT0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | LEUART0 Receive input. |
| LEU0_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | 0: PB14 | | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | 0: PB15 | | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| OPA0_N | 0: PA4 | | | | | | | | Operational Amplifier 0 external negative input. |
| OPA0_P | 0: PA2 | | | | | | | | Operational Amplifier 0 external positive input. |
| OPA1_N | 0: PD15 | | | | | | | | Operational Amplifier 1 external negative input. |
| OPA1_P | 0: PD13 | | | | | | | | Operational Amplifier 1 external positive input. |
| OPA2_N | 0: PB13 | | | | | | | | Operational Amplifier 2 external negative input. |
| OPA2_OUT | 0: PB12 | | | | | | | | Operational Amplifier 2 output. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|---|---|--|---|--|--|---|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| OPA2_OUTALT | 0: PB9 1: PB10 | | | | | | | | Operational Amplifier 2 alternative output. |
| OPA2_P | 0: PB11 | | | | | | | | Operational Amplifier 2 external positive input. |
| PCNT0_S0IN | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | 0: PA6 1: PA7 2: PA8 3: PA9 | 4: PI2 5: PI3 6: PB6 7: PB7 | 8: PB8 9: PB9 10: PB10 11: PJ14 | 12: PJ15 13: PC0 14: PC1 15: PC2 | 16: PC3 17: PC4 18: PC5 19: PF6 | 20: PF7 21: PF8 22: PF9 23: PF10 | 24: PF11 25: PF12 26: PF13 27: PF14 | 28: PF15 29: PK0 30: PK1 31: PK2 | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | 0: PA7 1: PA8 2: PA9 3: PI2 | 4: PI3 5: PB6 6: PB7 7: PB8 | 8: PB9 9: PB10 10: PJ14 11: PJ15 | 12: PC0 13: PC1 14: PC2 15: PC3 | 16: PC4 17: PC5 18: PF6 19: PF7 | 20: PF8 21: PF9 22: PF10 23: PF11 | 24: PF12 25: PF13 26: PF14 27: PF15 | 28: PK0 29: PK1 30: PK2 31: PA6 | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | 0: PA6 1: PA7 2: PA8 3: PA9 | 4: PI2 5: PI3 6: PB6 7: PB7 | 8: PB8 9: PB9 10: PB10 11: PJ14 | 12: PJ15 13: PC0 14: PC1 15: PC2 | 16: PC3 17: PC4 18: PC5 19: PC10 | 20: PC11 21: PF8 22: PF9 23: PF10 | 24: PF11 25: PF12 26: PF13 27: PF14 | 28: PF15 29: PK0 30: PK1 31: PK2 | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | 0: PA7 1: PA8 2: PA9 3: PI2 | 4: PI3 5: PB6 6: PB7 7: PB8 | 8: PB9 9: PB10 10: PJ14 11: PJ15 | 12: PC0 13: PC1 14: PC2 15: PC3 | 16: PC4 17: PC5 18: PC10 19: PC11 | 20: PF8 21: PF9 22: PF10 23: PF11 | 24: PF12 25: PF13 26: PF14 27: PF15 | 28: PK0 29: PK1 30: PK2 31: PA6 | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | 0: PF0 1: PF1 2: PF2 3: PF3 | 4: PF4 5: PF5 6: PF6 7: PF7 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | 0: PF1 1: PF2 2: PF3 3: PF4 | 4: PF5 5: PF6 6: PF7 7: PF0 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | 0: PF2 1: PF3 2: PF4 3: PF5 | 4: PF6 5: PF7 6: PF0 7: PF1 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | 0: PF3 1: PF4 2: PF5 3: PF6 | 4: PF7 5: PF0 6: PF1 7: PF2 | 8: PD9 9: PD10 10: PD11 11: PD12 | 12: PD13 13: PD14 14: PD15 | | | | | Peripheral Reflex System PRS, channel 3. |
| PRS_CH4 | 0: PD9 1: PD10 2: PD11 3: PD12 | 4: PD13 5: PD14 6: PD15 | | | | | | | Peripheral Reflex System PRS, channel 4. |

| Alternate | LOCATION | | | | | | | | |
|---------------|--|--|---|--|--|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| PRS_CH5 | 0: PD10 1: PD11 2: PD12 3: PD13 | 4: PD14 5: PD15 6: PD9 | | | | | | | Peripheral Reflex System PRS, channel 5. |
| PRS_CH6 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PD9 | 12: PD10 13: PD11 14: PD12 15: PD13 | 16: PD14 17: PD15 | | | | Peripheral Reflex System PRS, channel 6. |
| PRS_CH7 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PA0 | | | | | | Peripheral Reflex System PRS, channel 7. |
| PRS_CH8 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PA0 10: PA1 | | | | | | Peripheral Reflex System PRS, channel 8. |
| PRS_CH9 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PA0 9: PA1 10: PA2 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 | | | | Peripheral Reflex System PRS, channel 9. |
| PRS_CH10 | 0: PC6 1: PC7 2: PC8 3: PC9 | 4: PC10 5: PC11 | | | | | | | Peripheral Reflex System PRS, channel 10. |
| PRS_CH11 | 0: PC7 1: PC8 2: PC9 3: PC10 | 4: PC11 5: PC6 | | | | | | | Peripheral Reflex System PRS, channel 11. |
| TIM0_CC0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDT10 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDT11 | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDT12 | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | Timer 0 Complimentary Dead Time Insertion channel 2. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|--|---|---|--|--|--|--|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| TIM1_CC0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | Timer 1 Capture Compare input / output channel 2. |
| TIM1_CC3 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | Timer 1 Capture Compare input / output channel 3. |
| US0_CLK | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | USART0 clock input / output. |
| US0_CS | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | USART0 chip select input / output. |
| US0_CTS | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | USART0 Clear To Send hardware flow control input. |
| US0_RTS | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | USART0 Request To Send hardware flow control output. |
| US0_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | USART1 clock input / output. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|--|---|---|--|--|--|--|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US1_CS | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | USART1 chip select input / output. |
| US1_CTS | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | USART1 Clear To Send hardware flow control input. |
| US1_RTS | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | USART1 Request To Send hardware flow control output. |
| US1_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | 0: PA7 1: PA8 2: PA9 3: PI0 | 4: PI1 5: PI2 6: PI3 7: PB6 | 8: PB7 9: PB8 10: PB9 11: PB10 | 12: PF0 13: PF1 14: PF3 15: PF4 | 16: PF5 17: PF6 18: PF7 19: PF8 | 20: PF9 21: PF10 22: PF11 23: PF12 | 24: PF13 25: PF14 26: PF15 27: PK0 | 28: PK1 29: PK2 30: PA5 31: PA6 | USART2 clock input / output. |
| US2_CS | 0: PA8 1: PA9 2: PI0 3: PI1 | 4: PI2 5: PI3 6: PB6 7: PB7 | 8: PB8 9: PB9 10: PB10 11: PF0 | 12: PF1 13: PF3 14: PF4 15: PF5 | 16: PF6 17: PF7 18: PF8 19: PF9 | 20: PF10 21: PF11 22: PF12 23: PF13 | 24: PF14 25: PF15 26: PK0 27: PK1 | 28: PK2 29: PA5 30: PA6 31: PA7 | USART2 chip select input / output. |
| US2_CTS | 0: PA9 1: PI0 2: PI1 3: PI2 | 4: PI3 5: PB6 6: PB7 7: PB8 | 8: PB9 9: PB10 10: PF0 11: PF1 | 12: PF3 13: PF4 14: PF5 15: PF6 | 16: PF7 17: PF8 18: PF9 19: PF10 | 20: PF11 21: PF12 22: PF13 23: PF14 | 24: PF15 25: PK0 26: PK1 27: PK2 | 28: PA5 29: PA6 30: PA7 31: PA8 | USART2 Clear To Send hardware flow control input. |
| US2_RTS | 0: PI0 1: PI1 2: PI2 3: PI3 | 4: PB6 5: PB7 6: PB8 7: PB9 | 8: PB10 9: PF0 10: PF1 11: PF3 | 12: PF4 13: PF5 14: PF6 15: PF7 | 16: PF8 17: PF9 18: PF10 19: PF11 | 20: PF12 21: PF13 22: PF14 23: PF15 | 24: PK0 25: PK1 26: PK2 27: PA5 | 28: PA6 29: PA7 30: PA8 31: PA9 | USART2 Request To Send hardware flow control output. |
| US2_RX | 0: PA6 1: PA7 2: PA8 3: PA9 | 4: PI0 5: PI1 6: PI2 7: PI3 | 8: PB6 9: PB7 10: PB8 11: PB9 | 12: PB10 13: PF0 14: PF1 15: PF3 | 16: PF4 17: PF5 18: PF6 19: PF7 | 20: PF8 21: PF9 22: PF10 23: PF11 | 24: PF12 25: PF13 26: PF14 27: PF15 | 28: PK0 29: PK1 30: PK2 31: PA5 | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | | |
|------------------------------|--|--|---|--|--|--|--|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US2_TX | 0: PA5 1: PA6 2: PA7 3: PA8 | 4: PA9 5: PI0 6: PI1 7: PI2 | 8: PI3 9: PB6 10: PB7 11: PB8 | 12: PB9 13: PB10 14: PF0 15: PF1 | 16: PF3 17: PF4 18: PF5 19: PF6 | 20: PF7 21: PF8 22: PF9 23: PF10 | 24: PF11 25: PF12 26: PF13 27: PF14 | 28: PF15 29: PK0 30: PK1 31: PK2 | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| US3_CLK | 0: PD10 1: PD11 2: PD12 3: PD13 | 4: PD14 5: PD15 6: PI2 7: PI3 | 8: PB6 9: PB7 10: PB8 11: PB9 | 12: PB10 13: PB11 14: PJ14 15: PJ15 | 16: PC0 17: PC1 18: PC2 19: PC3 | 20: PC4 21: PC5 22: PF11 23: PF12 | 24: PF13 25: PF14 26: PF15 27: PK0 | 28: PK1 29: PK2 30: PD8 31: PD9 | USART3 clock input / output. |
| US3_CS | 0: PD11 1: PD12 2: PD13 3: PD14 | 4: PD15 5: PI2 6: PI3 7: PB6 | 8: PB7 9: PB8 10: PB9 11: PB10 | 12: PB11 13: PJ14 14: PJ15 15: PC0 | 16: PC1 17: PC2 18: PC3 19: PC4 | 20: PC5 21: PF11 22: PF12 23: PF13 | 24: PF14 25: PF15 26: PK0 27: PK1 | 28: PK2 29: PD8 30: PD9 31: PD10 | USART3 chip select input / output. |
| US3_CTS | 0: PD12 1: PD13 2: PD14 3: PD15 | 4: PI2 5: PI3 6: PB6 7: PB7 | 8: PB8 9: PB9 10: PB10 11: PB11 | 12: PJ14 13: PJ15 14: PC0 15: PC1 | 16: PC2 17: PC3 18: PC4 19: PC5 | 20: PF11 21: PF12 22: PF13 23: PF14 | 24: PF15 25: PK0 26: PK1 27: PK2 | 28: PD8 29: PD9 30: PD10 31: PD11 | USART3 Clear To Send hardware flow control input. |
| US3_RTS | 0: PD13 1: PD14 2: PD15 3: PI2 | 4: PI3 5: PB6 6: PB7 7: PB8 | 8: PB9 9: PB10 10: PB11 11: PJ14 | 12: PJ15 13: PC0 14: PC1 15: PC2 | 16: PC3 17: PC4 18: PC5 19: PF11 | 20: PF12 21: PF13 22: PF14 23: PF15 | 24: PK0 25: PK1 26: PK2 27: PD8 | 28: PD9 29: PD10 30: PD11 31: PD12 | USART3 Request To Send hardware flow control output. |
| US3_RX | 0: PD9 1: PD10 2: PD11 3: PD12 | 4: PD13 5: PD14 6: PD15 7: PI2 | 8: PI3 9: PB6 10: PB7 11: PB8 | 12: PB9 13: PB10 14: PB11 15: PJ14 | 16: PJ15 17: PC0 18: PC1 19: PC2 | 20: PC3 21: PC4 22: PC5 23: PF11 | 24: PF12 25: PF13 26: PF14 27: PF15 | 28: PK0 29: PK1 30: PK2 31: PD8 | USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO). |
| US3_TX | 0: PD8 1: PD9 2: PD10 3: PD11 | 4: PD12 5: PD13 6: PD14 7: PD15 | 8: PI2 9: PI3 10: PB6 11: PB7 | 12: PB8 13: PB9 14: PB10 15: PB11 | 16: PJ14 17: PJ15 18: PC0 19: PC1 | 20: PC2 21: PC3 22: PC4 23: PC5 | 24: PF11 25: PF12 26: PF13 27: PF14 | 28: PF15 29: PK0 30: PK1 31: PK2 | USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI). |
| VDAC0_EXT | 0: PA1 | | | | | | | | Digital to analog converter VDAC0 external reference input pin. |
| VDAC0_OUT0 / OPA0_OUT | 0: PA3 | | | | | | | | Digital to Analog Converter DAC0 output channel number 0. |
| VDAC0_OUT0ALT / OPA0_OUT-ALT | 0: PA5 1: PD13 2: PD15 | | | | | | | | Digital to Analog Converter DAC0 alternative output for channel 0. |

| Alternate | LOCATION | | | | | | | | |
|-------------------------------|--|--|--|--|--|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| VDAC0_OUT1 / OPA1_OUT | 0: PD14 | | | | | | | | Digital to Analog Converter DAC0 output channel number 1. |
| VDAC0_OUT1AL T / OPA1_OUT-ALT | 0: PD12 1: PA2 2: PA4 | | | | | | | | Digital to Analog Converter DAC0 alternative output for channel 1. |
| WTIM0_CC0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PA6 7: PA7 | 8: PA8 9: PA9 10: PB6 11: PB7 | 12: PB8 13: PB9 14: PB10 15: PB11 | 16: PB12 17: PB13 18: PB14 19: PB15 | 20: PC0 21: PC1 22: PC2 23: PC3 | 24: PC4 25: PC5 26: PC6 27: PC7 | 28: PC8 29: PC9 30: PC10 31: PC11 | Wide timer 0 Capture Compare input / output channel 0. |
| WTIM0_CC1 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PA6 5: PA7 6: PA8 7: PA9 | 8: PB6 9: PB7 10: PB8 11: PB9 | 12: PB10 13: PB11 14: PB12 15: PB13 | 16: PB14 17: PB15 18: PC0 19: PC1 | 20: PC2 21: PC3 22: PC4 23: PC5 | 24: PC6 25: PC7 26: PC8 27: PC9 | 28: PC10 29: PC11 30: PD8 31: PD9 | Wide timer 0 Capture Compare input / output channel 1. |
| WTIM0_CC2 | 0: PA4 1: PA5 2: PA6 3: PA7 | 4: PA8 5: PA9 6: PB6 7: PB7 | 8: PB8 9: PB9 10: PB10 11: PB11 | 12: PB12 13: PB13 14: PB14 15: PB15 | 16: PC0 17: PC1 18: PC2 19: PC3 | 20: PC4 21: PC5 22: PC6 23: PC7 | 24: PC8 25: PC9 26: PC10 27: PC11 | 28: PD8 29: PD9 30: PD10 31: PD11 | Wide timer 0 Capture Compare input / output channel 2. |
| WTIM0_CDTI0 | 0: PA8 1: PA9 2: PB6 3: PB7 | 4: PB8 5: PB9 6: PB10 7: PB11 | 8: PB12 9: PB13 10: PB14 11: PB15 | 12: PC0 13: PC1 14: PC2 15: PC3 | 16: PC4 17: PC5 18: PC6 19: PC7 | 20: PC8 21: PC9 22: PC10 23: PC11 | 24: PD8 25: PD9 26: PD10 27: PD11 | 28: PD12 29: PD13 30: PD14 31: PD15 | Wide timer 0 Complimentary Dead Time Insertion channel 0. |
| WTIM0_CDTI1 | 0: PB6 1: PB7 2: PB8 3: PB9 | 4: PB10 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC0 11: PC1 | 12: PC2 13: PC3 14: PC4 15: PC5 | 16: PC6 17: PC7 18: PC8 19: PC9 | 20: PC10 21: PC11 22: PD8 23: PD9 | 24: PD10 25: PD11 26: PD12 27: PD13 | 28: PD14 29: PD15 30: PF0 31: PF1 | Wide timer 0 Complimentary Dead Time Insertion channel 1. |
| WTIM0_CDTI2 | 0: PB8 1: PB9 2: PB10 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC0 9: PC1 10: PC2 11: PC3 | 12: PC4 13: PC5 14: PC6 15: PC7 | 16: PC8 17: PC9 18: PC10 19: PC11 | 20: PD8 21: PD9 22: PD10 23: PD11 | 24: PD12 25: PD13 26: PD14 27: PD15 | 28: PF0 29: PF1 30: PF2 31: PF3 | Wide timer 0 Complimentary Dead Time Insertion channel 2. |
| WTIM1_CC0 | 0: PB12 1: PB13 2: PB14 3: PB15 | 4: PC0 5: PC1 6: PC2 7: PC3 | 8: PC4 9: PC5 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD8 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Wide timer 1 Capture Compare input / output channel 0. |
| WTIM1_CC1 | 0: PB14 1: PB15 2: PC0 3: PC1 | 4: PC2 5: PC3 6: PC4 7: PC5 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD8 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PF8 31: PF9 | Wide timer 1 Capture Compare input / output channel 1. |
| WTIM1_CC2 | 0: PC0 1: PC1 2: PC2 3: PC3 | 4: PC4 5: PC5 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD8 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PF8 29: PF9 30: PF10 31: PF11 | Wide timer 1 Capture Compare input / output channel 2. |
| WTIM1_CC3 | 0: PC2 1: PC3 2: PC4 3: PC5 | 4: PC6 5: PC7 6: PC8 7: PC9 | 8: PC10 9: PC11 10: PD8 11: PD9 | 12: PD10 13: PD11 14: PD12 15: PD13 | 16: PD14 17: PD15 18: PF0 19: PF1 | 20: PF2 21: PF3 22: PF4 23: PF5 | 24: PF6 25: PF7 26: PF8 27: PF9 | 28: PF10 29: PF11 30: PF12 31: PF13 | Wide timer 1 Capture Compare input / output channel 3. |

6.5 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 6.3 APORT Connection Diagram on page 104 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

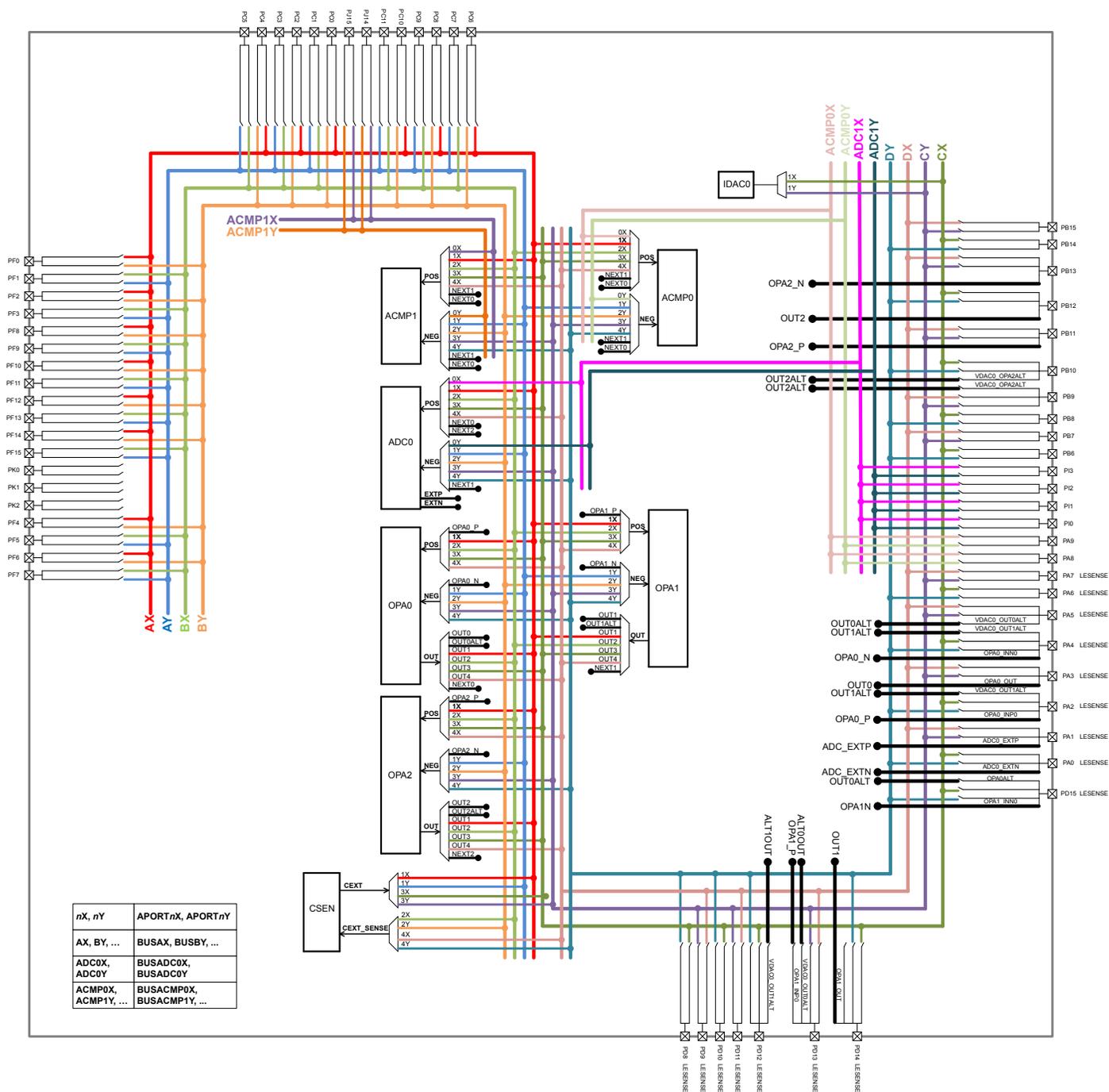


Figure 6.3. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.5. ACMP0 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | APORT0Y | APORT0X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|-----------|-----------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | BUSACMP0Y | BUSACMP0X | Bus |
| PB14 | PB15 | PB15 | PB14 | PF14 | PF15 | PF15 | PF14 | | | CH31 |
| | PB13 | PB13 | | PF14 | | | | | | CH30 |
| PB12 | PB11 | PB11 | PB12 | PF12 | PF13 | PF13 | PF12 | | | CH29 |
| | PB11 | PB11 | | PF12 | PF11 | PF11 | | | | CH28 |
| PB10 | | | PB10 | PF10 | | | PF10 | | | CH27 |
| | PB9 | PB9 | | PF10 | PF9 | PF9 | | | | CH26 |
| PB8 | | | PB8 | PF8 | | | PF8 | | | CH25 |
| | PB7 | PB7 | | PF8 | PF7 | PF7 | | | | CH24 |
| PB6 | | | PB6 | PF6 | | | PF6 | | | CH23 |
| | | | | PF6 | PF5 | PF5 | | | | CH22 |
| | | | | | PF5 | | | | | CH21 |
| | | | | PF4 | | | PF4 | | | CH20 |
| | | | | | PF3 | PF3 | | | | CH19 |
| | | | | PF2 | | | PF2 | | | CH18 |
| | | | | | PF1 | PF1 | | | | CH17 |
| | | | | PF0 | | | PF0 | | | CH16 |
| | PA7 | PA7 | | | | | | | | CH15 |
| PA6 | | | PA6 | | | | | | | CH14 |
| | PA5 | PA5 | | | | | | | | CH13 |
| | | | | | | | | | | CH12 |
| PA4 | | | PA4 | | | | | | | CH11 |
| | PA3 | PA3 | | | PC11 | PC11 | | | | CH10 |
| PA2 | | | PA2 | PC10 | | | PC10 | | | CH9 |
| | PA1 | PA1 | | | PC9 | PC9 | | | | CH8 |
| PA0 | | | PA0 | PC8 | | | PC8 | | | CH7 |
| | PD15 | PD15 | | | PC7 | PC7 | | | | CH6 |
| PD14 | | | PD14 | PC6 | | | PC6 | | | CH5 |
| | PD13 | PD13 | | | PC5 | PC5 | | | | CH4 |
| PD12 | | | PD12 | PC4 | | | PC4 | | | CH3 |
| | PD11 | PD11 | | | PC3 | PC3 | | | | CH2 |
| PD10 | | | PD10 | PC2 | | | PC2 | | | CH1 |
| | PD9 | PD9 | | | PC1 | PC1 | | PA9 | PA9 | CH0 |
| PD8 | | | PD8 | PC0 | | | PC0 | PA8 | PA8 | CH0 |

Table 6.6. ACMP1 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | APORT0Y | APORT0X | Port Bus |
|---------|---------|---------|---------|---------|---------|---------|---------|-----------|-----------|----------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | BUSACMP1Y | BUSACMP1X | CH31 |
| PB14 | PB15 | PB15 | PB14 | PF14 | PF15 | PF15 | PF14 | | | CH30 |
| PB12 | PB13 | PB13 | PB12 | PF12 | PF13 | PF13 | PF12 | | | CH29 |
| | PB11 | PB11 | | | PF11 | PF11 | | | | CH28 |
| PB10 | | | PB10 | PF10 | | | PF10 | | | CH27 |
| | PB9 | PB9 | | | PF9 | PF9 | | | | CH26 |
| PB8 | | | PB8 | PF8 | | | PF8 | | | CH25 |
| | PB7 | PB7 | | | PF7 | PF7 | | | | CH24 |
| PB6 | | | PB6 | PF6 | | | PF6 | | | CH23 |
| | | | | | PF5 | PF5 | | | | CH22 |
| | | | | | | | | | | CH21 |
| | | | | | PF3 | PF3 | PF4 | | | CH20 |
| | | | | | | | | | | CH19 |
| | | | | | PF2 | PF2 | PF2 | | | CH18 |
| | | | | | | | | | | CH17 |
| | | | | | PF1 | PF1 | PF0 | | | CH16 |
| | | | | | | | | | | CH15 |
| PA6 | PA7 | PA7 | PA6 | | | | | | | CH14 |
| | PA5 | PA5 | | | | | | | | CH13 |
| | | | | | | | | | | CH12 |
| PA4 | | | PA4 | | | | | | | CH11 |
| | PA3 | PA3 | | | PC11 | PC11 | | | | CH10 |
| PA2 | | | PA2 | PC10 | | | PC10 | | | CH9 |
| | PA1 | PA1 | | | PC9 | PC9 | | | | CH8 |
| PA0 | | | PA0 | PC8 | | | PC8 | | | CH7 |
| | PD15 | PD15 | | | PC7 | PC7 | | PJ15 | PJ15 | CH6 |
| PD14 | | | PD14 | PC6 | | | PC6 | PJ14 | PJ14 | CH5 |
| | PD13 | PD13 | | | PC5 | PC5 | | | | CH4 |
| PD12 | | | PD12 | PC4 | | | PC4 | | | CH3 |
| | PD11 | PD11 | | | PC3 | PC3 | | | | CH2 |
| PD10 | | | PD10 | PC2 | | | PC2 | | | CH1 |
| | PD9 | PD9 | | | PC1 | PC1 | | | | CH0 |
| PD8 | | | PD8 | PC0 | | | PC0 | | | |

Table 6.7. ADC0 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | APORT0Y | APORT0X | Port Bus |
|---------|---------|---------|---------|---------|---------|---------|---------|----------|----------|----------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | BUSADC0Y | BUSADC0X | CH31 |
| PB14 | PB15 | PB15 | PB14 | PF14 | PF15 | PF15 | PF14 | | | CH30 |
| PB12 | PB13 | PB13 | PB12 | PF12 | PF13 | PF13 | PF12 | | | CH29 |
| PB10 | PB11 | PB11 | PB10 | PF10 | PF11 | PF11 | PF10 | | | CH28 |
| PB8 | PB9 | PB9 | PB8 | PF8 | PF9 | PF9 | PF8 | | | CH27 |
| PB6 | PB7 | PB7 | PB6 | PF6 | PF7 | PF7 | PF6 | | | CH26 |
| | | | | | | | | | | CH25 |
| | | | | | | | | | | CH24 |
| | | | | | | | | | | CH23 |
| | | | | | | | | | | CH22 |
| | | | | | | | | | | CH21 |
| | | | | | | | | | | CH20 |
| | | | | | | | | | | CH19 |
| | | | | | | | | | | CH18 |
| | | | | | | | | | | CH17 |
| | | | | | | | | | | CH16 |
| | | | | | | | | | | CH15 |
| PA6 | PA7 | PA7 | PA6 | | | | | | | CH14 |
| | | | | | | | | | | CH13 |
| | | | | | | | | | | CH12 |
| | | | | | | | | | | CH11 |
| | | | | | | | | | | CH10 |
| PA2 | PA3 | PA3 | PA2 | PC10 | PC11 | PC11 | PC10 | | | CH9 |
| | | | | | | | | | | CH8 |
| PA0 | PA1 | PA1 | PA0 | PC8 | PC9 | PC9 | PC8 | | | CH7 |
| | | | | | | | | | | CH6 |
| PD14 | PD15 | PD15 | PD14 | PC6 | PC7 | PC7 | PC6 | | | CH5 |
| | | | | | | | | | | CH4 |
| PD12 | PD13 | PD13 | PD12 | PC4 | PC5 | PC5 | PC4 | | | CH3 |
| | | | | | | | | | | CH2 |
| PD10 | PD11 | PD11 | PD10 | PC2 | PC3 | PC3 | PC2 | PI3 | PI3 | CH1 |
| | | | | | | | | PI2 | PI2 | CH0 |
| PD8 | PD9 | PD9 | PD8 | PC0 | PC1 | PC1 | PC0 | PI0 | PI0 | |

Table 6.8. CSEN Bus and Pin Mapping

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | | |
|-------------------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|--|
| CEXT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSCX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PF0 | | | | PC11 | | | PC9 | | PC8 | | | | | | | | |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | | | PA2 | | PA0 | | | | | | | | |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | PA7 | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | | | |
| APORT1X | BUSAX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT3X | BUSCX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT3Y | BUSCY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CEXT_SENSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | | PC11 | | | PC9 | | PC8 | | | | | | | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | | PC0 | | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | PA6 | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 | | | |
| APORT2X | BUSBX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT2Y | BUSBY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT4X | BUSDX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT4Y | BUSDY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 6.9. IDAC0 Bus and Pin Mapping

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | | |
|---------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|------|-----|------|-----|------|-----|------|-----|-----|--|
| APORT1X | BUSCX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | | | |
| APORT1X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 | |
| APORT1Y | BUSCY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSCX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSCY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSCX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSCY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 6.10. VDAC0 / OPA Bus and Pin Mapping

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---------------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|-----|-----|
| OPA0_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | PA7 | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | PA6 | | | PA4 | | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| OPA0_P | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | PA6 | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | PA7 | | | PA5 | | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | | |
|------------------------------|---------|---------|---------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|--|
| VDAC0_OUT1 / OPA1_OUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT4Y | APORT3Y | APORT2Y | APORT1Y | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BUSDY | BUSCY | BUSBY | BUSAY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PB14 | PB15 | PF14 | PF15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PB12 | PB13 | PF12 | PF13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PB10 | PB11 | PF10 | PF11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PB8 | PB9 | PF8 | PF9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PB6 | PB7 | PF6 | PF7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PA6 | PA7 | PF0 | PF1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PA4 | PA5 | PF0 | PF1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PA2 | PA3 | PC10 | PC11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PA0 | PA1 | PC8 | PC9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD14 | PD15 | PC6 | PC7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD12 | PD13 | PC4 | PC5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD10 | PD11 | PC2 | PC3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD8 | PD9 | PC0 | PC1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

7. BGA125 Package Specifications

7.1 BGA125 Package Dimensions

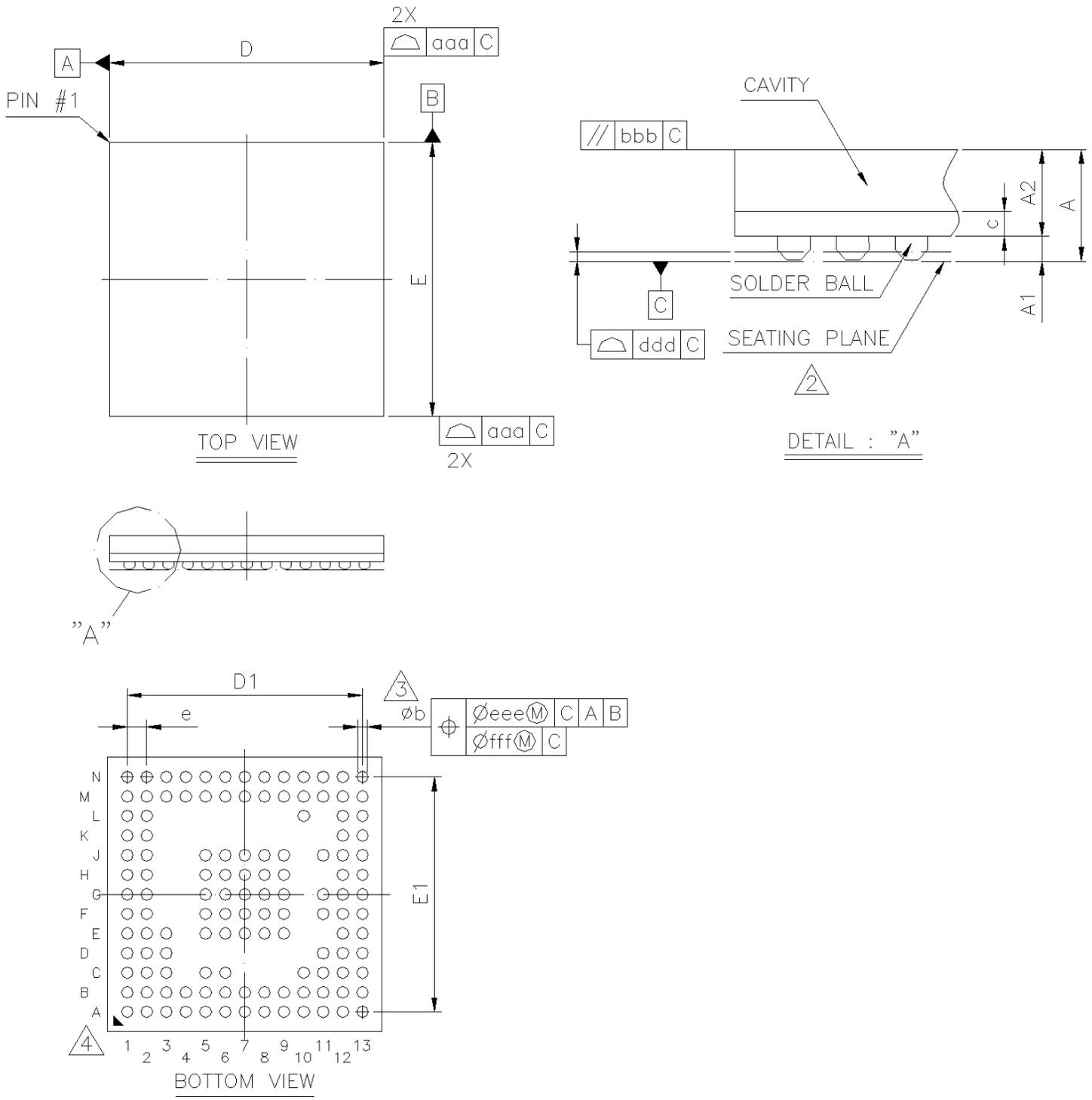


Figure 7.1. BGA125 Package Drawing

Table 7.1. BGA125 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|------|------|------|
| A | 0.80 | 0.87 | 0.94 |
| A1 | 0.16 | 0.21 | 0.26 |
| A2 | 0.61 | 0.66 | 0.71 |
| c | 0.17 | 0.21 | 0.25 |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| D1 | — | 6.00 | — |
| E1 | — | 6.00 | — |
| e | — | 0.50 | — |
| b | 0.25 | 0.30 | 0.35 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ddd | 0.08 | | |
| eee | 0.15 | | |
| fff | 0.05 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7.2 BGA125 PCB Land Pattern

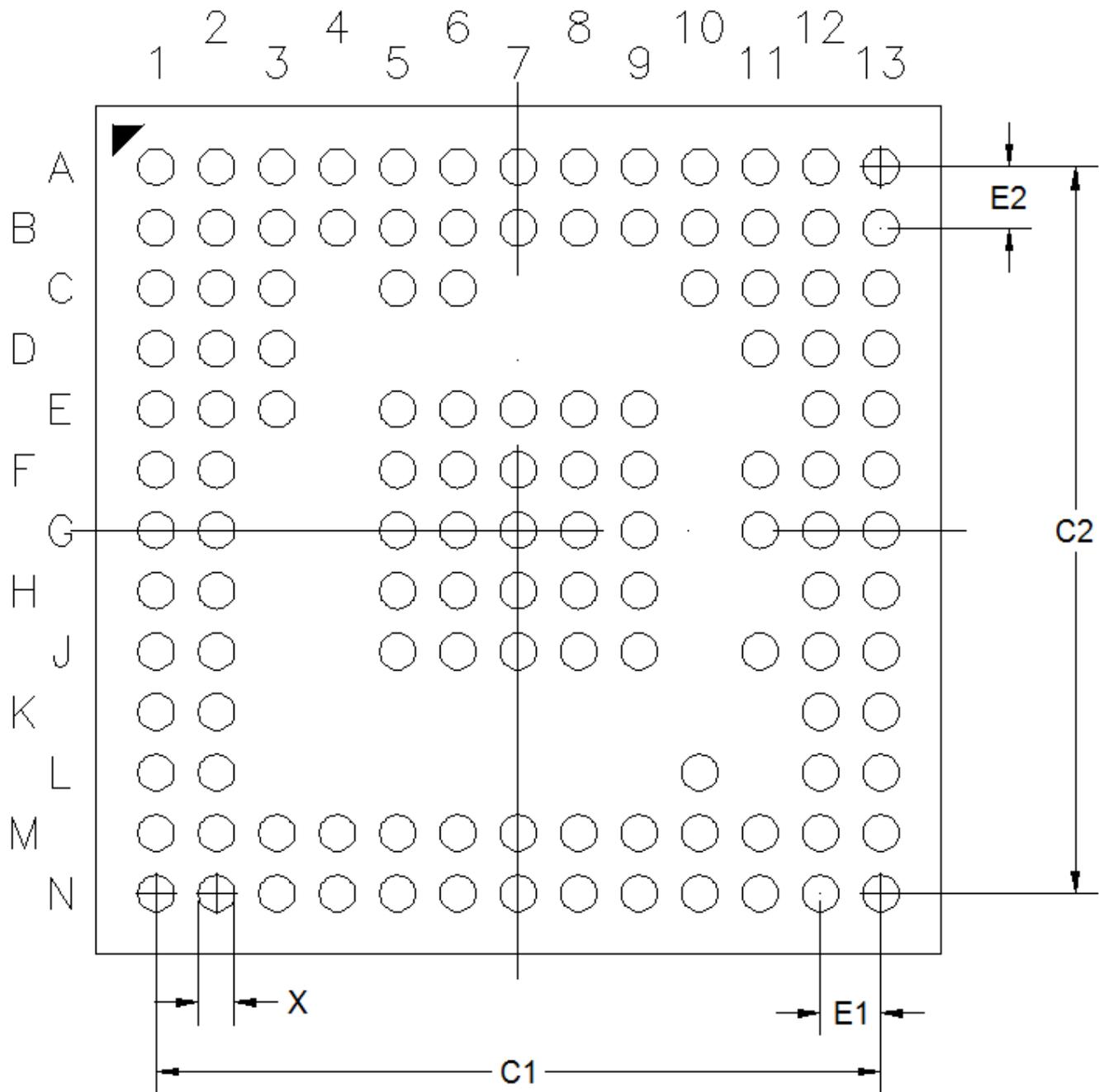


Figure 7.2. BGA125 PCB Land Pattern Drawing

Table 7.2. BGA125 PCB Land Pattern Dimensions

| Dimension | Min | Nom | Max |
|-----------|-----|------|-----|
| X | | 0.25 | |
| C1 | | 6.00 | |
| C2 | | 6.00 | |
| E1 | | 0.5 | |
| E2 | | 0.5 | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Note: Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

7.3 BGA125 Package Marking



Figure 7.3. BGA125 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. QFN48 Package Specifications

8.1 QFN48 Package Dimensions

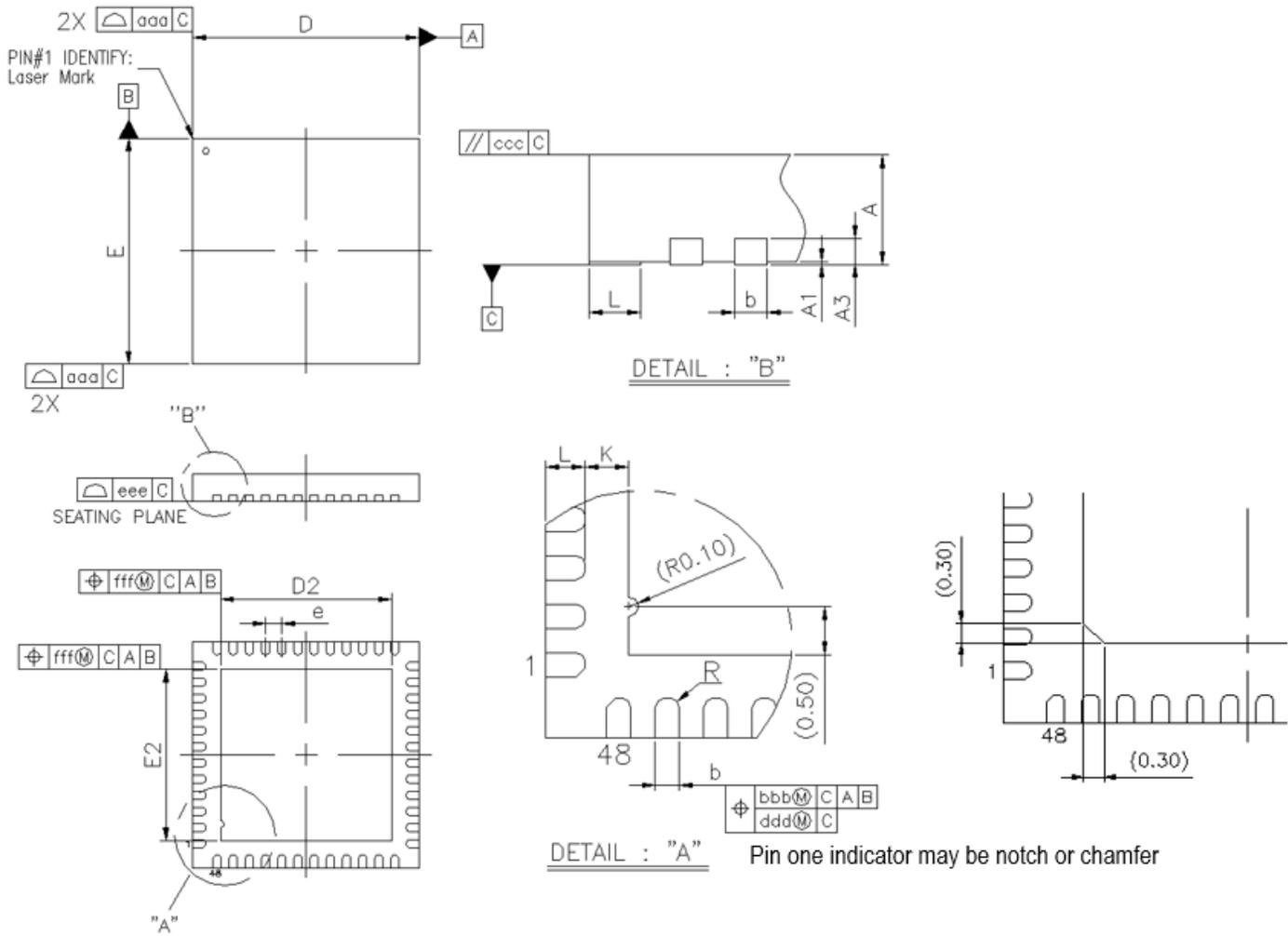


Figure 8.1. QFN48 Package Drawing

Table 8.1. QFN48 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| D2 | 5.15 | 5.30 | 5.45 |
| E2 | 5.15 | 5.30 | 5.45 |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| R | 0.09 | — | — |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN48 PCB Land Pattern

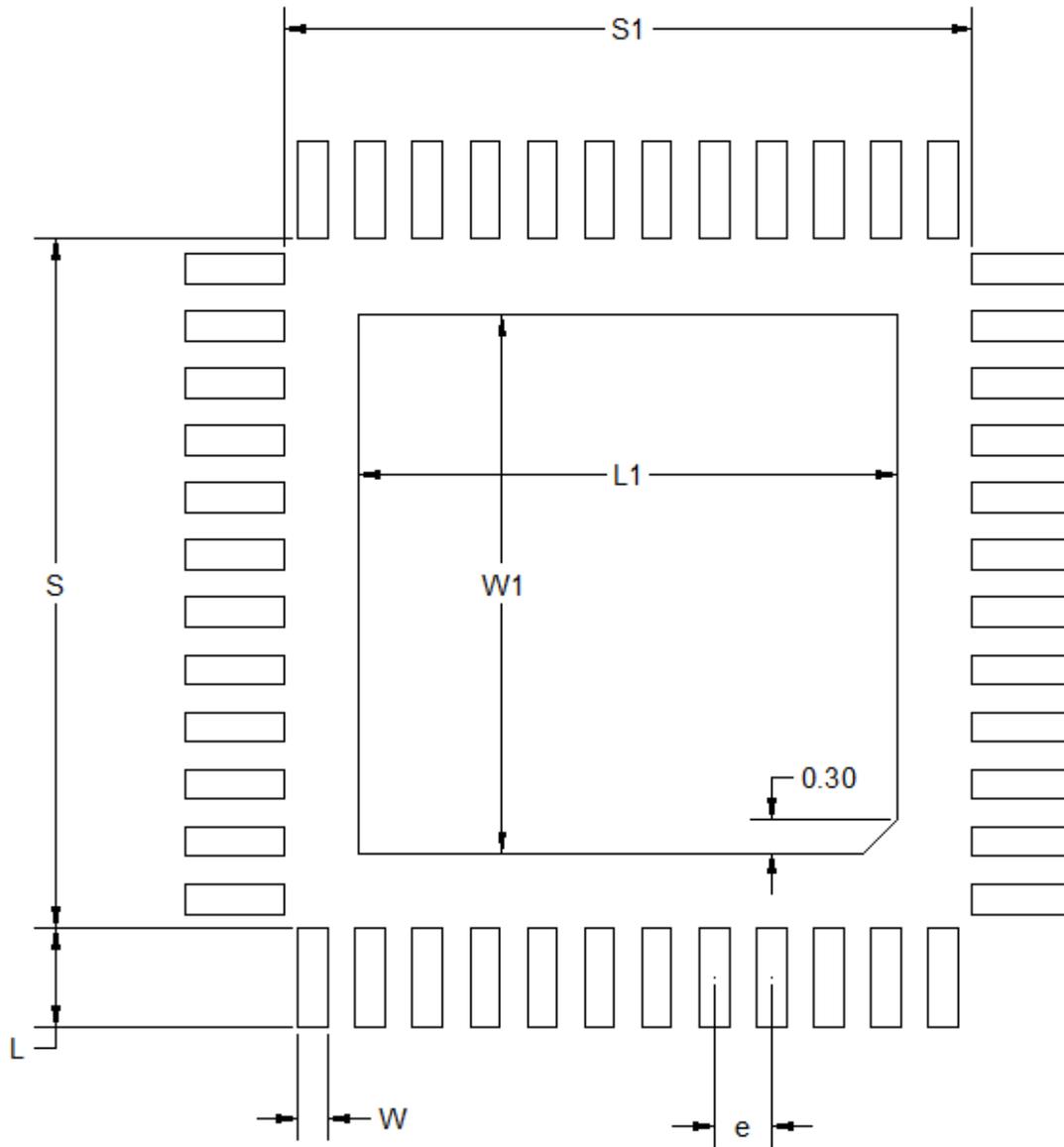


Figure 8.2. QFN48 PCB Land Pattern Drawing

Table 8.2. QFN48 PCB Land Pattern Dimensions

| Dimension | Typ |
|-----------|------|
| S1 | 6.01 |
| S | 6.01 |
| L1 | 4.70 |
| W1 | 4.70 |
| e | 0.50 |
| W | 0.26 |
| L | 0.86 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Note: Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

8.3 QFN48 Package Marking



Figure 8.3. QFN48 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

9. Revision History

Revision 1.3

June, 2022

- Updated [3.5.3 Real Time Counter and Calendar \(RTCC\)](#) to remove AUXHFRCO as a clock source.
- Added HFSRCCLK frequency in [Table 4.2 General Operating Conditions on page 19](#).
- Added timing specifications for RESETn low time and clarified V_{IL} and V_{IH} logic levels for RESETn pins in [Table 4.17 General-Purpose I/O \(GPIO\) on page 35](#).
- Removed BIASPROG = 1, FULLBIAS = 0 specifications from [Table 4.20 Analog Comparator \(ACMP\) on page 40](#).
- Updated Hysteresis max values in [Table 4.20 Analog Comparator \(ACMP\) on page 40](#).
- Updated the note in [Table 4.24 Operational Amplifier \(OPAMP\) on page 49](#).
- Added [Figure 4.2 SPI Master Timing Diagram \(SMSDELAY = 1\) on page 57](#).
- Added a note to [Table 8.2 QFN48 PCB Land Pattern Dimensions on page 121](#) and [Table 7.2 BGA125 PCB Land Pattern Dimensions on page 116](#).

Revision 1.2

November, 2019

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated [3.5.4 Low Energy Timer \(LETIMER\)](#) lowest energy mode.
- Added a Note about the operating voltage in [3.7.3 True Random Number Generator \(TRNG\)](#).
- Reworded or removed mentions of “modules” in reference to device peripherals in system overview.

Revision 1.1

February, 2018

- Updated [2. Ordering Information](#) to revision-C OPNs.
- [System Overview](#) Updates
 - Added "4-pin JTAG" to debug interface options in Processor Core section.
 - Memory maps updated with LE peripherals and new formatting.
- [4.1.1 Absolute Maximum Ratings](#): Added footnotes to clarify V_{DIGPIN} specification for 5V tolerant GPIO.
- [Table 4.2 General Operating Conditions on page 19](#):
 - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
 - Added footnote for additional information on peak current during voltage scaling operations.
- [4.1.4 DC-DC Converter](#): Expanded footnote on control loop settings to include appnote and register field reference.
- [Table 4.16 Flash Memory Characteristics⁵ on page 34](#): Device Erase Time typical values corrected from 69 to 82 ms.
- [Table 4.21 Digital to Analog Converter \(VDAC\) on page 42](#): Gain Error min/max specifications relaxed for REFSEL on 1V25LN, VDD, and EXT settings.
- [Table 4.22 Current Digital to Analog Converter \(IDAC\) on page 45](#): Total accuracy STEPSEL value setting corrected from 0x80 to 0x10.
- [Table 4.26 Analog Port \(APORT\) on page 52](#): Operation in EM2/EM3 supply current changed from 915 to 67 nA (silicon fix from rev B to C).

Revision 1.0

2017-06-30

- Finalized specification tables. All tables were updated with latest characterization data and production test limits.
- Updated typical performance graphs for DC-DC.
- Minor typographical, clarity, and consistency improvements.
- Condensed pin function tables with new formatting.

Revision 0.5

2017-02-10

- Updated Feature List and Front Page with latest characterization numbers.
- List of OPNs in Ordering Table consolidated.
- Electrical Characteristics Table Changes
 - All specification tables updated with latest characterization data and production test limits.
 - Split HFRCO/AUXHFRCO table into separate tables for HFRCO and AUXHFRCO.
 - OPAMP, CSEN, and VDAC specification line items updated to match test conditions.
 - Added tables for Analog Port (APORT) and Pulse Counter (PCNT).
- Added Typical Performance Curves for supply current and DCDC parameters.
- Added APORT Connection Diagram.

Revision 0.2

December 9th, 2016

Initial release.

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