

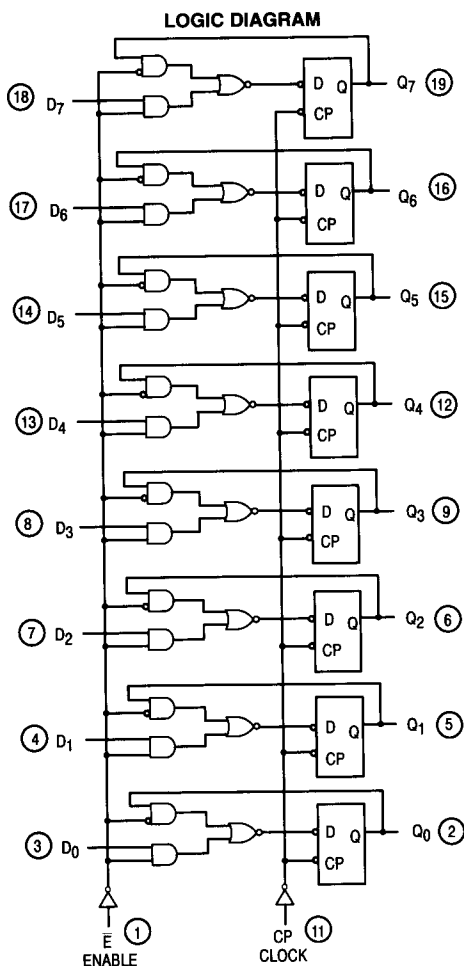


D-Type Flip-Flop With Enable

ELECTRICALLY TESTED PER:
MIL-M-38510/32504

The 54LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

- 8-Bit High-Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip-Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diode Limits High-Speed Termination Effects



Military 54LS377



AVAILABLE AS:

- 1) JAN: JM38510/32504BXA
- 2) SMD: N/A
- 3) 883: 54LS377/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\bar{E}$	1	1	1	GND
Q ₀	2	2	2	VCC
D ₀	3	3	3	VCC
D ₁	4	4	4	VCC
Q ₁	5	5	5	VCC
Q ₂	6	6	6	VCC
D ₂	7	7	7	VCC
D ₃	8	8	8	VCC
Q ₃	9	9	9	VCC
GND	10	10	10	GND
CP	11	11	11	CP1
Q ₄	12	12	12	VCC
D ₄	13	13	13	VCC
D ₅	14	14	14	VCC
Q ₅	15	15	15	VCC
Q ₆	16	16	16	VCC
D ₆	17	17	17	VCC
D ₇	18	18	18	VCC
Q ₇	19	19	19	VCC
VCC	20	20	20	VCC

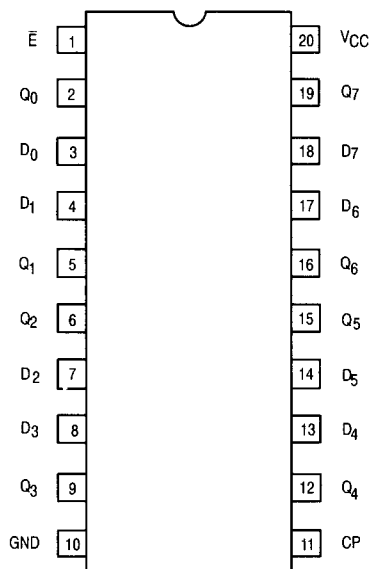
BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

$\bar{E}$	CP	D _n	Q _n	$\bar{Q}_n$
H		X	No Change	No Change
L		H	H	L
L		L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

CONNECTION DIAGRAM



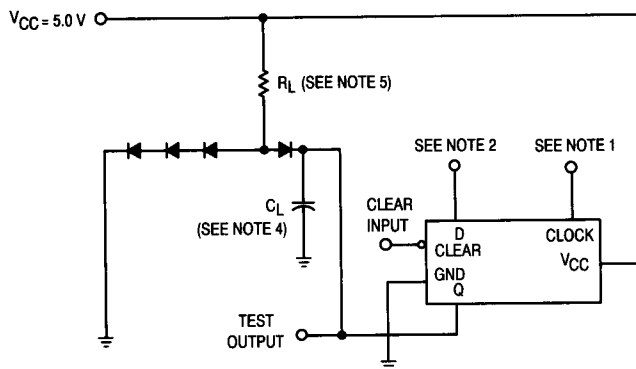
Pin Names		Loading (Note a)	
		HIGH	LOW
$\bar{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0 - D_3	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0 - Q_3	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
Q_0 - Q_3	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

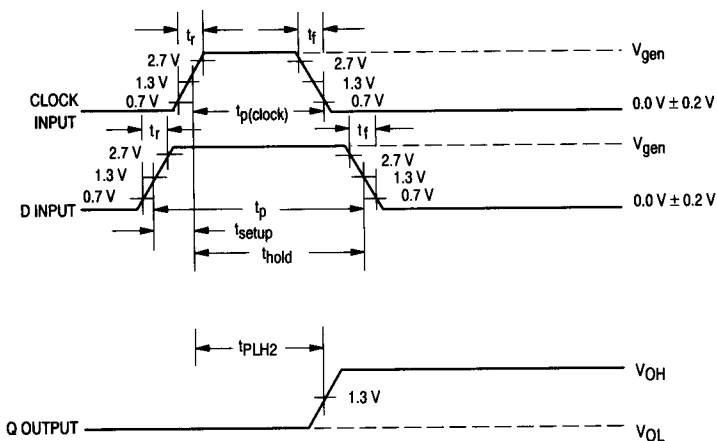
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

54LS377

AC TEST CIRCUIT



HIGH-LEVEL SWITCHING WAVEFORMS

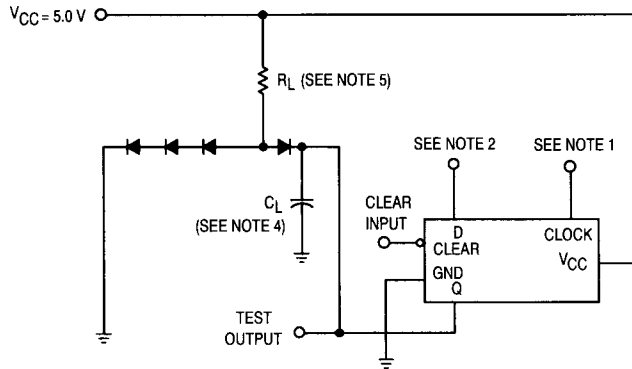


NOTES:

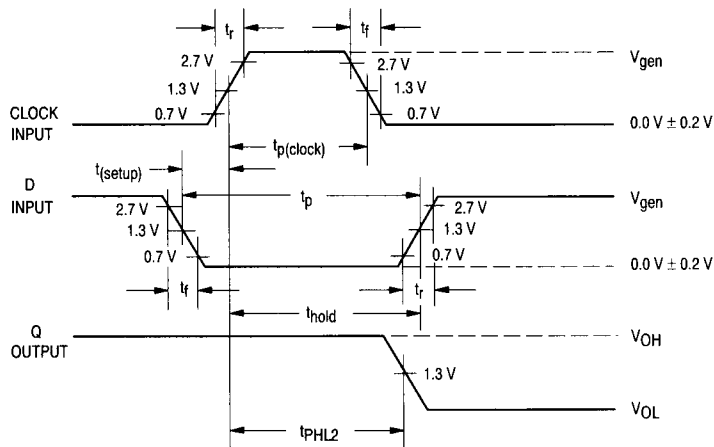
1. Clock input pulse has the following characteristics:
 $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_p(\text{clock}) = 30 \text{ ns}$,
and $\text{PRR} \leq 1.0 \text{ MHz}$.
2. D input has the following characteristics:
 $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_{setup} = 20 \text{ ns}$,
 $t_{hold} = 5.0 \text{ ns}$, $t_p = 25 \text{ ns}$, and PRR is 50% of the clock PRR .
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.

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AC TEST CIRCUIT



LOW-LEVEL SWITCHING WAVEFORMS



NOTES:

1. Clock input pulse has the following characteristics:
 $V_{gen} = 3.0 V \pm 0.2 V$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_p(\text{clock}) = 30 \text{ ns}$,
and $PRR \leq 1.0 \text{ MHz}$. When testing f_{MAX} , $PRR = \text{see table}$,
and $t_0 = t_1 \leq 6.0 \text{ ns}$.
2. D input has the following characteristics:
 $V_{gen} = 3.0 V \pm 0.2 V$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_{setup} = 20 \text{ ns}$,
 $t_{hold} = 5.0 \text{ ns}$, $t_p = 25 \text{ ns}$, and PRR is 50% of the clock PRR .
For f_{MAX} , $t_0 = t_1 \leq 6.0 \text{ ns}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = – 0.4 mA, V _{IH} = 2.0 V, E = 0.7 V, other inputs are open, CLK = (See Note 1).
V _{OL}	Logical “0” Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V, E = 0.7 V, other inputs are open, CLK = (See Note 1).
V _{IC}	Input Clamping Voltage		– 1.5					V	V _{CC} = 4.5 V, I _{IN} = – 18 mA, other inputs are open.
I _{IH}	Logical “1” Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, E = 0.7 V, CLK = (See Note 2), V _{OUT} = GND.
I _{IL1}	Logical “0” Input Current	– 105	– 345	– 105	– 345	– 105	– 345	μA	V _{CC} = 5.5 V, V _{IL} = 0.4 V (E), other inputs are open.
I _{IL2}	Logical “0” Input Current	– 160	– 400	– 160	– 400	– 160	– 400	μA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, other inputs are open.
I _{CC}	Power Supply Current Off		32		32		32	mA	V _{CC} = 5.5 V, V _{IN} = GND (all inputs), CLK = (See Note 2).
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output High-Low	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PLH2} t _{PLH2}	Propagation Delay /Data-Output Low-High	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
f _{MAX}	Maximum Clock Frequency	30 30		25		25		MHz	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.

NOTES:

1.  2.5 V minimum/5.5 V maximum
0.0 V
2.  2.5 V minimum/5.5 V maximum
0.0 V