Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2661, DECEMBER 1982—REVISED DECEMBER 1985

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability . . . 'ALS632A and 'ALS633**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'ALS632A	52-pin	yes	3-State
'ALS633	52-pin	yes	Open-Collector
'ALS634	48-pin	no	3-State
'ALS635	48-pin	no	Open-Collector

description

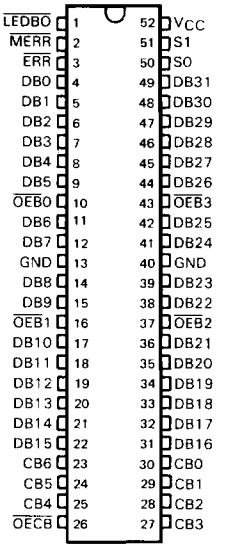
The 'ALS632A and 'ALS633 through 'ALS635 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('ALS632A and 'ALS633) or 48-pin ('ALS634 and 'ALS635) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

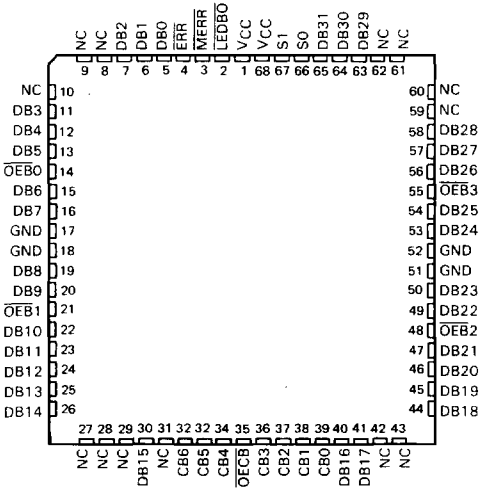
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

'ALS632A, 'ALS633 . . . JD PACKAGE
(TOP VIEW)



'ALS632A, 'ALS633 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

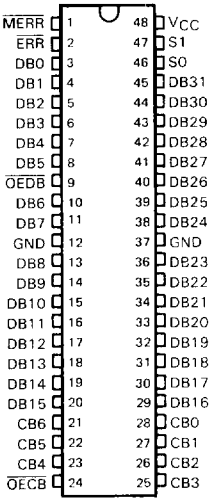
2

LSI Devices

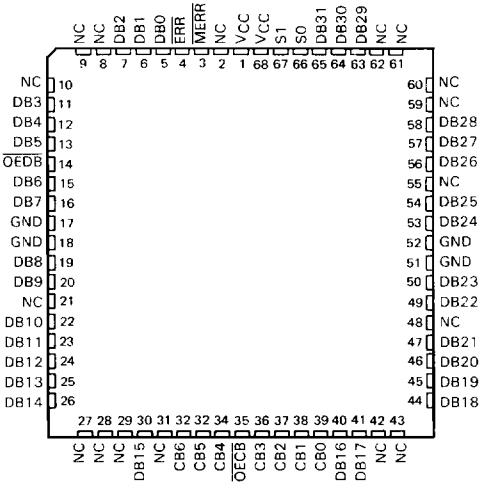
Read-modify-write (byte-control) operations can be performed with the 'ALS632A and 'ALS633 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

'ALS634, 'ALS635 . . . JD PACKAGE
(TOP VIEW)



'ALS634, 'ALS635 . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1 S0	DATA I/O	DB CONTROL $\overline{\text{OEBn}}$ OR $\overline{\text{OEDB}}$	DB OUTPUT LATCH ('ALS632A, 'ALS633) $\overline{\text{LEDBO}}$	CHECK I/O	CB CONTROL $\overline{\text{OECB}}$	ERROR FLAGS $\overline{\text{ERR}}$ $\overline{\text{MERR}}$
Write	Generate check word	L L	Input	H	X	Output check bits†	L	H H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

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TABLE 2. PARITY ALGORITHM

CHECK WORD	32-BIT DATA WORD																													
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X				X	X		X		X	X			X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X			X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{\text{MERR}}$ and a low on $\overline{\text{ERR}}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	$\overline{\text{ERR}}$	$\overline{\text{MERR}}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{\text{ERR}}$) will be set low while the dual error flag ($\overline{\text{MERR}}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH ('ALS632A, 'ALS633) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

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TABLE 5. SYNDROME DECODING

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	DB12
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X= error in check bit X
DB Y= error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS632A and 'ALS633 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEB}$n†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$	ERROR FLAG $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

†$\overline{OEB}$0 controls DB0-DB7 (BYTE0), $\overline{OEB}$1 controls DB8-DB15 (BYTE1), $\overline{OEB}$3 controls DB16-DB23 (BYTE2), $\overline{OEB}$3 controls DB24-DB31 (BYTE3).

diagnostic operations

The 'ALS632A and 'ALS633 thru 'ALS635 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the 'ALS632A and 'ALS633, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'ALS634 and 'ALS635 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('ALS632A and 'ALS633) and Table 8 ('ALS634 and 'ALS635) list the diagnostic functions.

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TABLE 7. 'ALS632A, 'ALS633 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEB_n}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

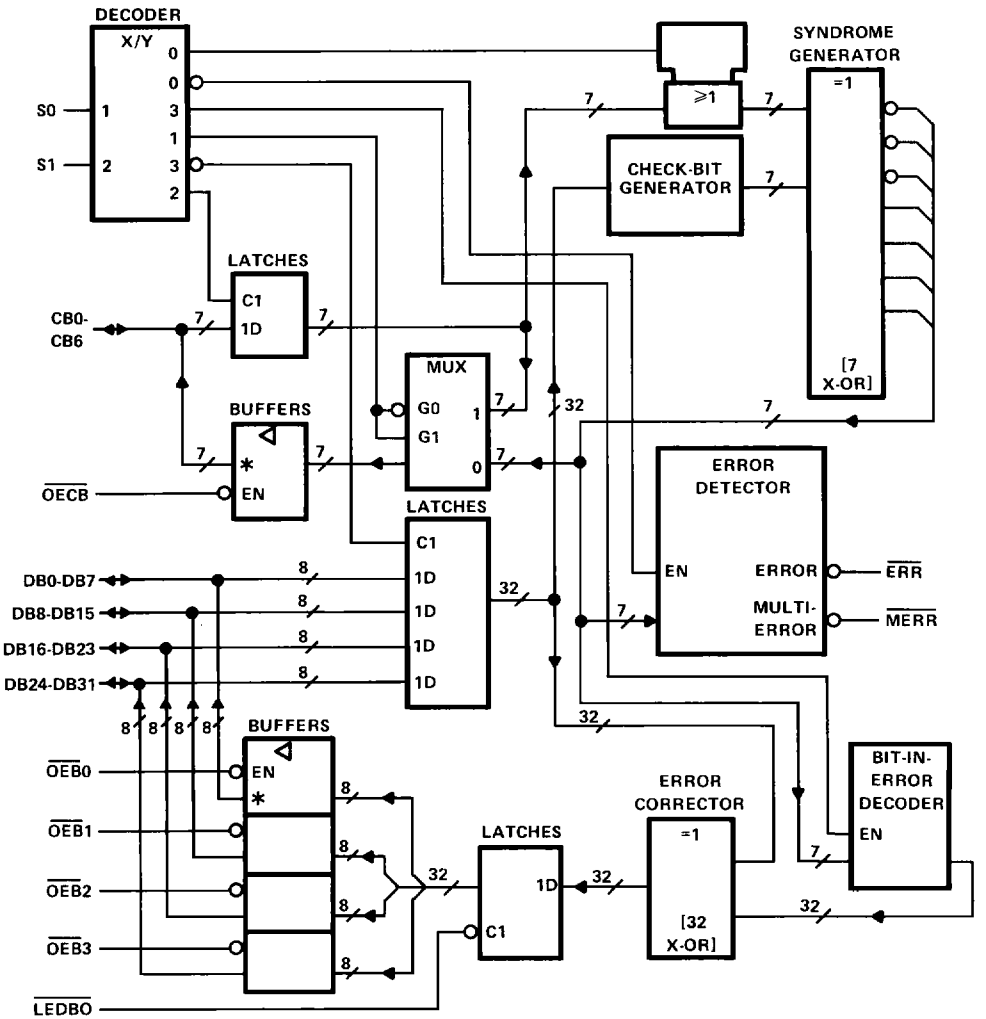
†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

TABLE 8. 'ALS634, 'ALS635 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	DB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Latched input check bits	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	L	Enabled	
Latch diagnostic data into input latch	H	H	Latched input diagnostic data word	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

'ALS632A, 'ALS633 logic diagram (positive logic)



*'ALS632A has 3-state (▽) check-bit and data outputs.
'ALS633 has open-collector (◇) check-bit and data outputs.

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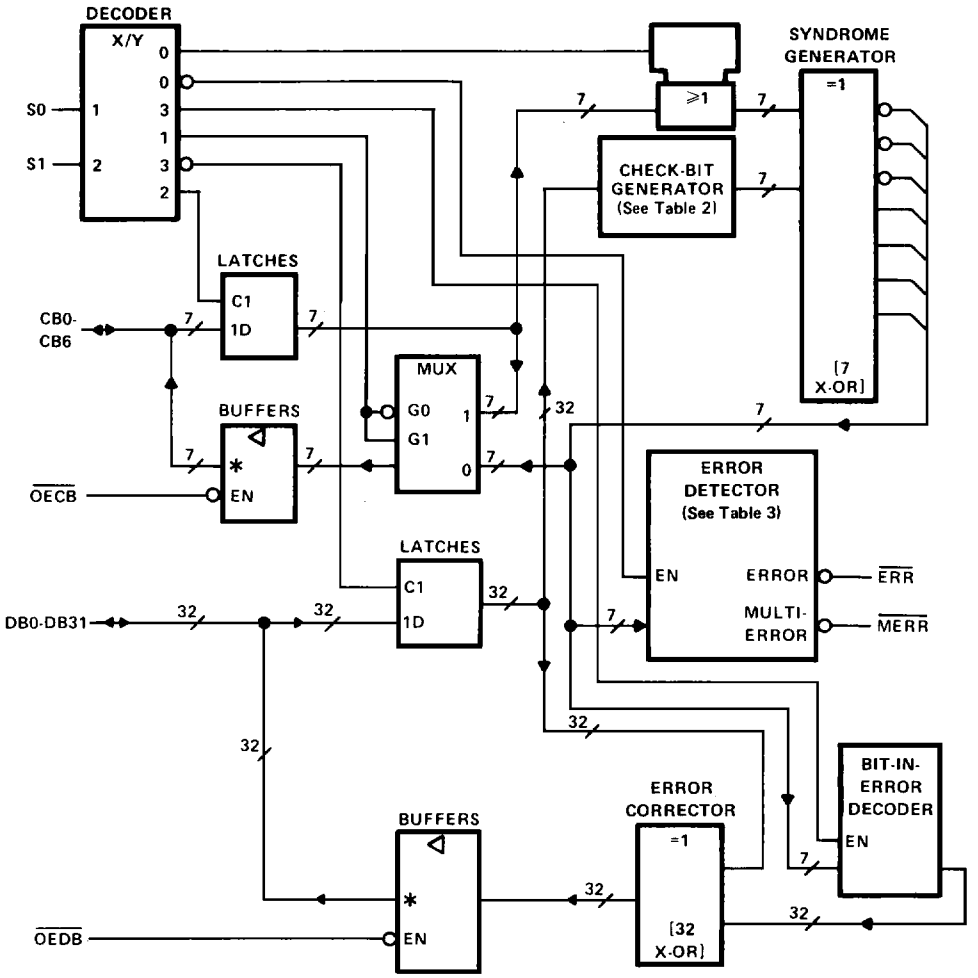
'ALS634, 'ALS635 logic diagram (positive logic)



*'ALS634 has 3-state (▽) check-bit and data outputs.
'ALS635 has open-collector (⏀) check-bit and data outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range:
SN74ALS632A, SN74ALS633 thru SN74ALS635 . . . . . 0°C to 70°C
Operating case temperature range:
SN54ALS632A, SN54ALS633 thru SN54ALS635 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS632A SN54ALS633 THRU SN54ALS635			SN74ALS632A SN74ALS633 THRU SN74ALS635			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB ‘ALS632A, ‘ALS634			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low	25			25			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	15			10			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)†	45			45			
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓†	0			0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)	0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)	15			10			
		(6) Diagnostic check word before the later of S1↓ or S0↑	15			10			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)‡	25			20			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	35			30			ns
		(9) Data and check word after S0↑ (S1 = H)	20			15			
		(10) Data word after S1↑ (S0 = H)	20			15			
		(11) Check word after the later of S1↓ or S0↑	20			15			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)‡	0			0			
t_{corr}	Correction time (see Figure 1)		65			58			ns
T_C	Operating case temperature		−55		125				°C
T_A	Operating free-air temperature					0		70	°C

†These times ensure that corrected data is saved in the output data latch.
‡These times ensure that the diagnostic data word is saved in the output data latch.

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'ALS632A, 'ALS634 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS632A SN54ALS634			SN74ALS632A SN74ALS634			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150	250		150	250	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS632A switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS632A, T_A = 0°C to 70°C for SN74ALS632A

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS632A		SN74ALS632A		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	67	15	55	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω	15	67	15	55	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	48	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	5	30	5	25	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	48	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	10	60	10	50	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns

'ALS634 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS634, T_A = 0°C to 70°C for SN74ALS634

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS634		SN74ALS634		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
			S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	67	15	55	ns
			S1 = L, S0 = H, R_L = 500 Ω	15	67	15	55	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	48	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	5	30	5	25	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	48	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t_{en}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{dis}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{en}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	30	ns
t_{dis}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns

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'ALS633 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS633			SN74ALS633			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150	250		150	250	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS633 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS633, T_A = 0°C to 70°C for SN74ALS633

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS633		SN74ALS633		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	67	15	55	ns
			S1 = L, S0 = H, R_L = 500 Ω	15	67	15	55	
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω	10	75	10	60	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	5	30	5	25	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω	10	70	10	60	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω	15	70	15	50	ns
t_{pd}	S1↑	CB	S0 = H, R_L = 680 Ω	10	60	10	45	ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PLH}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns
t_{PHL}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω	2	35	2	30	ns

'ALS635 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS635			SN74ALS635			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V							mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V							
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	All others‡									
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	All others‡									
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150			150		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'ALS635 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS635, T_A = 0°C to 70°C for SN74ALS635

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS635			SN74ALS635			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500 Ω		40			40		
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω		40			40		ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω		14			14		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω		40			40		ns
t_{pd}	S1↑	DB	S0 = H, R_L = 680 Ω		40			40		ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PLH}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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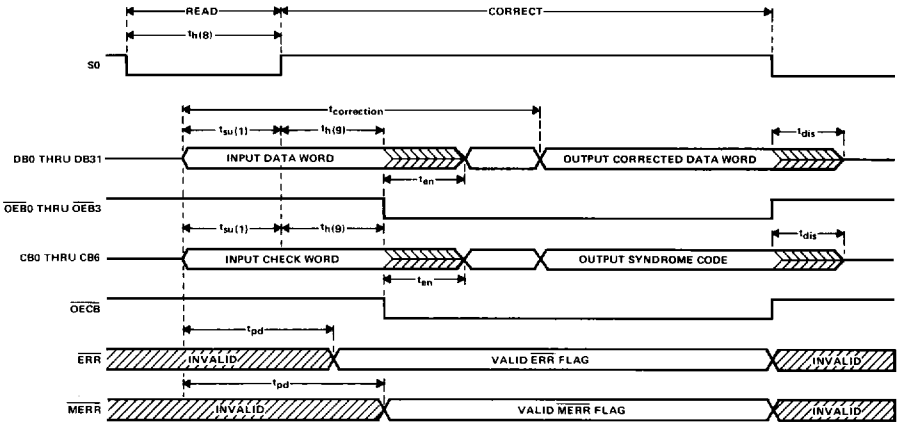

FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

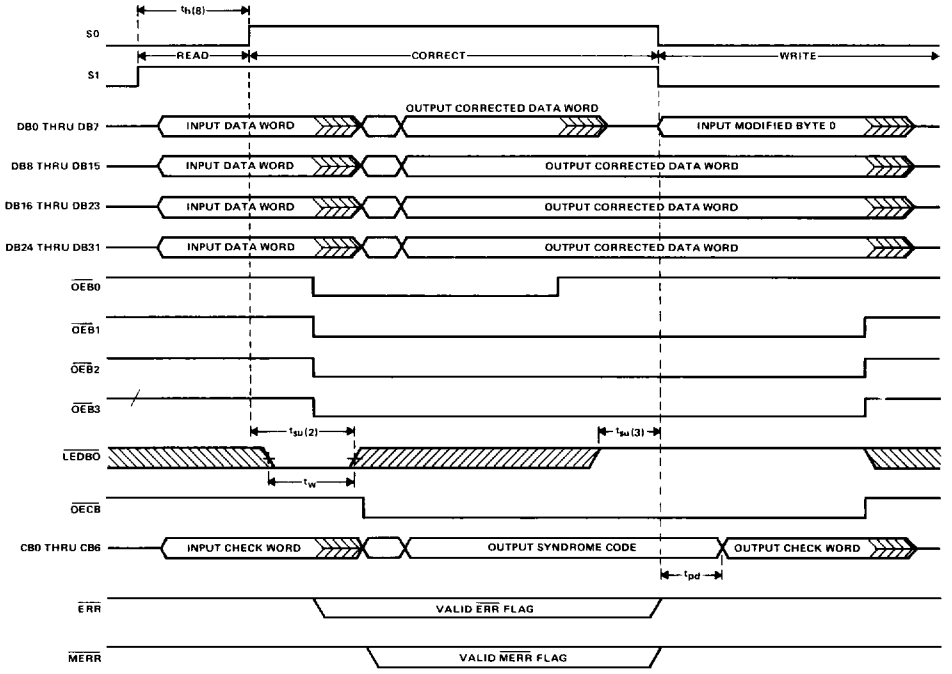

FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

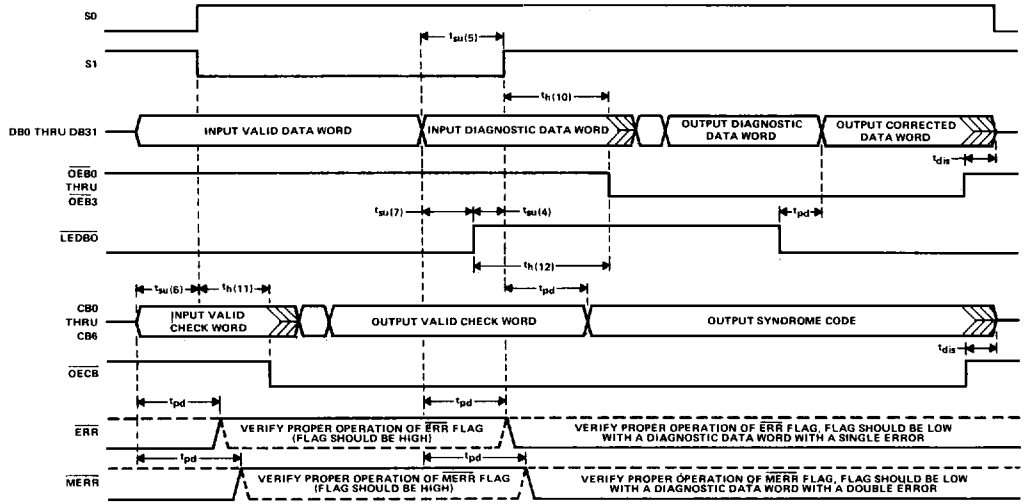

FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

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