

# CM2030

## HDMI Transmitter Port Protection and Interface Device

### Product Description

The CM2030 HDMI Transmitter Port Protection and Interface Device is specifically designed for next generation HDMI Host interface protection.

An integrated package provides all ESD, level shifting/isolation, overcurrent output protection and backdrive protection for an HDMI port in a single 38-pin TSSOP package.

The CM2030 also incorporates a silicon overcurrent protection device for +5 V supply voltage output to the connector.

CM2030 is ideal for applications which do not require HDMI certification but can benefit from level shifters and backdrive protection.

### Features

- Supports Thin Dielectric and 2-layer Boards
- Minimizes TMDS Skew with 0.05 pF Matching
- Long HDMI Cable Support with Integrated I<sup>2</sup>C Accelerator
- Supports Direct Connection to CEC Microcontroller
- Integrated I<sup>2</sup>C Level Shifting to CMOS Level Including Low Logic Level Voltages
- Integrated 8 kV ESD Protection and Backdrive Protection on All External I/O Lines
- Multiport I<sup>2</sup>C Support Eliminates Need for Analog Mux on DDC Lines
- Simplified Layout with Matched 0.5 mm Trace Spacing
- These Devices are Pb-Free and are RoHS Compliant

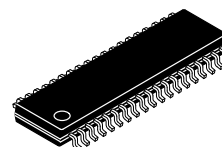
### Applications

- PC and Consumer Electronics
- Set Top Box, DVD RW, PC, Graphics Cards



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**TSSOP 38  
TR SUFFIX  
CASE 948AG**

### MARKING DIAGRAM

CM2030-A0TR

CM2030-A0TR = Specific Device Code

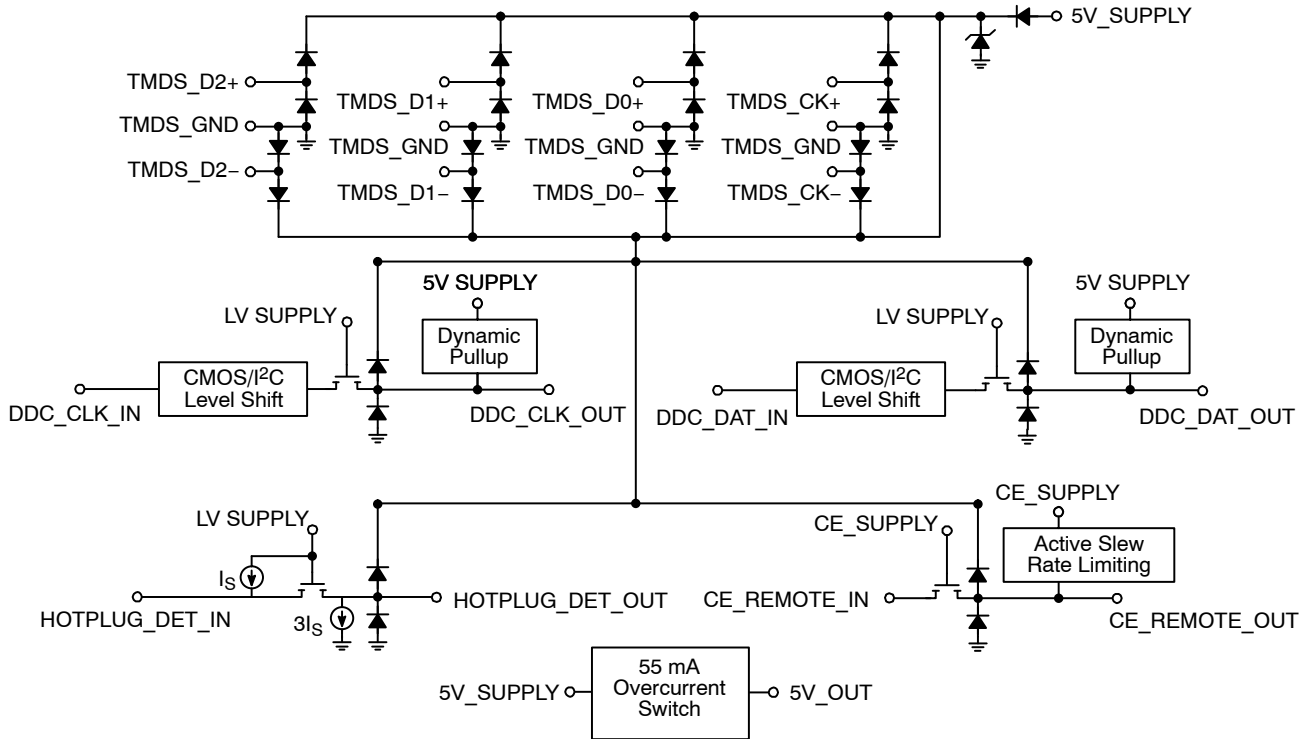
### ORDERING INFORMATION

| Device      | Package               | Shipping <sup>†</sup> |
|-------------|-----------------------|-----------------------|
| CM2030-A0TR | TSSOP-38<br>(Pb-Free) | 2500/Tape & Reel      |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

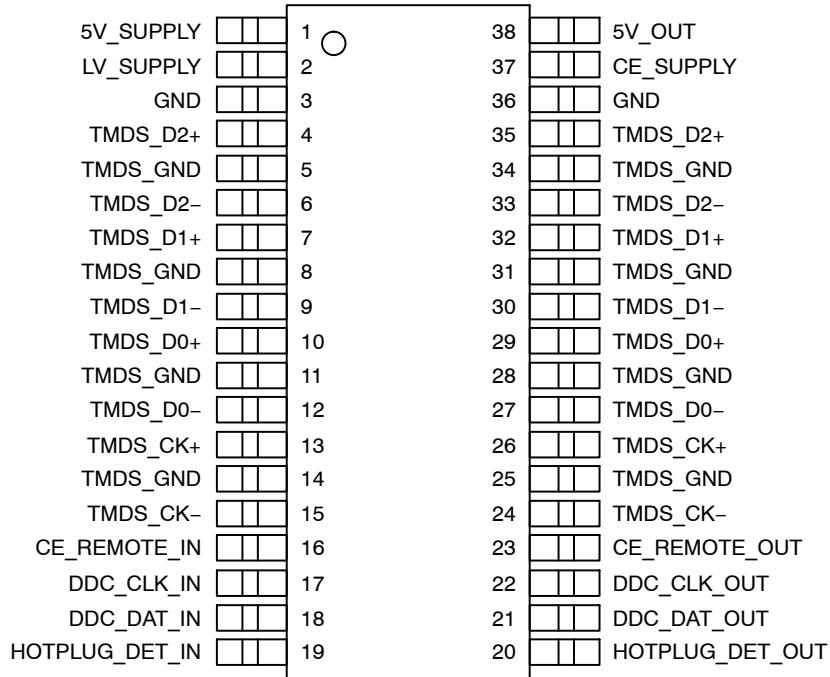
# CM2030

## ELECTRICAL SCHEMATIC



## PACKAGE / PINOUT DIAGRAM

Top View



38-Pin TSSOP Package

Table 1. PIN DESCRIPTIONS

| Pins                                | Name            | ESD Level          | Description                                                                                                                      |
|-------------------------------------|-----------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------|
| 4, 35                               | TMDS_D2+        | 8 kV (Note 3)      | TMDS 0.9 pF ESD Protection (Note 1)                                                                                              |
| 6, 33                               | TMDS_D2-        | 8 kV (Note 3)      | TMDS 0.9 pF ESD Protection (Note 1)                                                                                              |
| 7, 32                               | TMDS_D1+        | 8 kV (Note 3)      | TMDS 0.9 pF ESD Protection (Note 1)                                                                                              |
| 9, 30                               | TMDS_D1-        | 8 kV (Note 3)      | TMDS 0.9 pF ESD Protection (Note 1)                                                                                              |
| 10, 29                              | TMDS_D0+        | 8 kV (Note 3)      | TMDS 0.9 pF ESD Protection (Note 1)                                                                                              |
| 12, 27                              | TMDS_D0-        | 8 kV (Note 3)      | TMDS 0.9 pF ESD Protection (Note 1)                                                                                              |
| 13, 26                              | TMDS_CK+        | 8 kV (Note 3)      | TMDS 0.9 pF ESD Protection (Note 1)                                                                                              |
| 15, 24                              | TMDS_CK-        | 8 kV (Note 3)      | TMDS 0.9 pF ESD Protection (Note 1)                                                                                              |
| 16                                  | CE_REMOTE_IN    | 2 kV (Note 4)      | CE_SUPPLY Referenced Logic Level In                                                                                              |
| 23                                  | CE_REMOTE_OUT   | 8 kV (Note 3)      | 5V_SUPPLY Referenced Logic Level Out plus 10 pF ESD (Note 6)                                                                     |
| 17                                  | DDC_CLK_IN      | 2 kV (Note 4)      | LV_SUPPLY Referenced Logic Level In                                                                                              |
| 22                                  | DDC_CLK_OUT     | 8 kV (Note 3)      | 5V_SUPPLY Referenced Logic Level Out plus 10 pF ESD (Note 6)                                                                     |
| 18                                  | DDC_DAT_IN      | 2 kV (Note 4)      | LV_SUPPLY Referenced Logic Level In                                                                                              |
| 21                                  | DDC_DAT_OUT     | 8 kV (Note 3)      | 5V_SUPPLY Referenced Logic Level Out plus 10 pF ESD (Note 6)                                                                     |
| 19                                  | HOTPLUG_DET_IN  | 2 kV (Note 4)      | LV_SUPPLY Referenced Logic Level In                                                                                              |
| 20                                  | HOTPLUG_DET_OUT | 8 kV (Note 3)      | 5V_SUPPLY Referenced Logic Level Out plus 10 pF ESD. A 0.1 $\mu$ F Bypass Ceramic Capacitor is Recommended on this Pin (Note 2). |
| 2                                   | LV_SUPPLY       | 2 kV (Note 4)      | Bias for CE / DDC / HOTPLUG Level Shifters                                                                                       |
| 37                                  | CE_SUPPLY       | 2 kV (Notes 2 & 4) | CEC Bias Voltage. Previously CM2020 ESD_BYP Pin.                                                                                 |
| 1                                   | 5V_SUPPLY       | 2 kV (Note 4)      | Current Source for 5V_OUT, VREF for DDC I <sup>2</sup> C Voltage References, and Bias for 8 kV ESD Pins.                         |
| 38                                  | 5V_OUT          | 8 kV (Note 3)      | 55 mA Minimum Overcurrent Protected 5 V Output. This Output Must be Bypassed with a 0.1 $\mu$ F Ceramic Capacitor.               |
| 3, 5, 8, 11, 14, 25, 28, 31, 34, 36 | GND / TMDS_GND  | N/A                | GND Reference                                                                                                                    |

1. These 2 pins need to be connected together in-line on the PCB. See recommended layout diagram.
2. This output can be connected to an external 0.1  $\mu$ F ceramic capacitor/pads to maintain backward compatibility with the CM2020.
3. Standard IEC 61000-4-2, C<sub>DISCHARGE</sub> = 150 pF, R<sub>DISCHARGE</sub> = 330  $\Omega$ , 5V\_SUPPLY and LV\_SUPPLY within recommended operating conditions, GND = 0 V, 5V\_OUT (pin 38), and HOTPLUG\_DET\_OUT (pin 20) each bypassed with a 0.1  $\mu$ F ceramic capacitor connected to GND.
4. Human Body Model per MIL-STD-883, Method 3015, C<sub>DISCHARGE</sub> = 100 pF, R<sub>DISCHARGE</sub> = 1.5 k $\Omega$ , 5V\_SUPPLY and LV\_SUPPLY within recommended operating conditions, GND = 0 V, 5V\_OUT (pin 38), and HOTPLUG\_DET\_OUT (pin 20) each bypassed with a 0.1  $\mu$ F ceramic capacitor connected to GND.
5. These pins should be routed directly to the associated GND pins on the HDMI connector with single point ground vias at the connector.
6. The slew-rate control and active acceleration circuitry dynamically offsets the system capacitive load on these pins.

## BACKDRIVE PROTECTION AND ISOLATION

Backdrive current is defined as the undesirable current flow through an I/O pin when that I/O pin's voltage exceeds the related local supply voltage for that circuitry. This is a potentially common occurrence in multimedia entertainment systems with multiple components and several power plane domains in each system.

For example, if a DVD player is switched off and an HDMI connected TV is powered on, there is a possibility of reverse current flow back into the main power supply rail of the DVD player from pull-ups in the TV. As little as a few milliamps of backdrive current flowing back into the power rail can charge the DVD player's bulk bypass capacitance on the power rail to some intermediate level. If this level rises above the power-on-reset (POR) voltage level of some of the integrated circuits in the DVD player, then these devices

may not reset properly when the DVD player is turned back on.

If any SOC devices are incorporated in the design which have built-in level shifter and/or ESD protection structures, there can be a risk of permanent damage due to backdrive. In this case, backdrive current can forward bias the on-chip ESD protection structure. If the current flow is high enough, even as little as a few milliamps, it could destroy one of the SOC chip's internal DRC diodes, as they are not designed for passing DC.

To avoid either of these situations, the CM2030 was designed to block backdrive current, guaranteeing less than 5  $\mu$ A into any I/O pin when the I/O pin voltage exceeds its related operating CM2030 supply voltage.

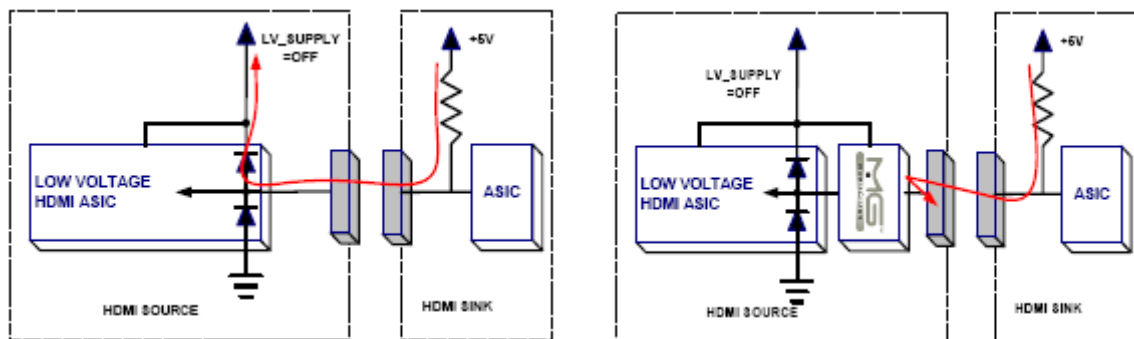


Figure 1. Backdrive Protection Diagram.

## DISPLAY DATA CHANNEL (DDC) LINES

The DDC interface is based on the I<sup>2</sup>C serial bus protocol for EDID configuration.

### Dynamic Pullups

Based on the HDMI specification, the maximum capacitance of the DDC line can approach 800 pF (50 pF from source, 50 pF from sink, and 700 pF from cable). At the upper range of capacitance values (i.e. long cables), it becomes impossible for the DDC lines to meet the I<sup>2</sup>C timing specifications with the minimum pull-up resistor of 1.5 k $\Omega$ .

For this reason, the CM2030 was designed with an internal I<sup>2</sup>C accelerator to meet the AC timing specification even with very long and non-compliant cables.

The internal accelerator increases the positive slew rate of the DDC\_CLK\_OUT and DDC\_DAT\_OUT lines whenever the sensed voltage level exceeds 0.3\*5V\_SUPPLY (approximately 1.5 V). This provides faster overall risetime in heavily loaded situations without overloading the multi-drop open drain I<sup>2</sup>C outputs elsewhere.

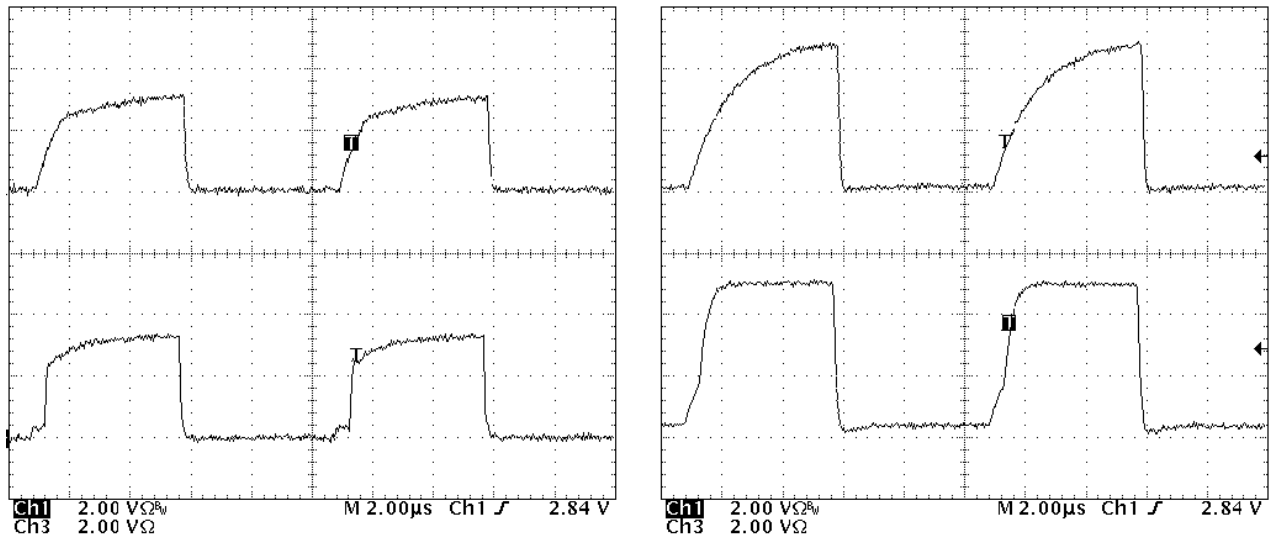
Figure 2 demonstrates the “worst case” operation of the dynamic CM2030 DDC level shifting circuitry (bottom)

against a discrete NFET common-gate level shifter circuit with a typical 1.5 kW pullup at the source (top.) Both are shown driving an off-spec, but unfortunately readily available 31 m HDMI cable which exceeds the 700 pF HDMI specification. Some widely available HDMI cables have been measured at over 4 nF.

When the standard I/OD cell releases the NFET discrete shifter, the risetime is limited by the pullup and the parasitics of the cable, source and sink. For long cables, this can extend the risetime and reduce the margin for reading a valid “high” level on the data line. In this case, an HDMI source may not be able to read uncorrupted data and will not be able to initiate a link.

With the CM2030's dynamic pullups, when the ASIC driver releases its DDC line and the “OUT” line reaches at least 0.3\*VDD (of 5V\_SUPPLY), then the “OUT” active pullups are enabled and the CM2030 takes over driving the cable until the “OUT” voltage approaches the 5V\_SUPPLY rail.

The internal pass element and the dynamic pullups also work together to damp reflections on the longer cables and keep them from glitching the local ASIC.



**Figure 2. Dynamic DDC Pullups**  
(Discrete – Top, CM2030 – Bottom; 3.3 V ASIC – Left, 5 V Cable – Right)

### I<sup>2</sup>C Low Level Shifting

In addition to the Dynamic Pullups described in the previous section, the CM2030 also incorporates improved I<sup>2</sup>C low-level shifting on the DDC\_CLK\_IN and DDC\_DAT\_IN lines for enhanced compatibility.

Typical discrete NFET level shifters can advertise specifications for low R<sub>DS(on)</sub>, but usually state relatively high V<sub>GS</sub> test parameters, requiring a ‘switch’ signal (gate voltage) as high as 10 V or more. At a sink current of 4 mA for the ASIC on DDC\_XX\_IN, the CM2030 guarantees no more than 140 mV increase to DDC\_XX\_OUT, even with a switching control of 2.5 V on LV\_SUPPLY.

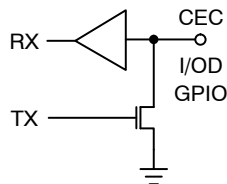
When I<sup>2</sup>C devices are driving the external cable, an internal pulldown on DDC\_XX\_IN guarantees that the VOL seen by the ASIC on DDC\_XX\_IN is equal to or lower than DDC\_XX\_OUT.

### Multiport DDC Multiplexing

By switching LV\_SUPPLY, the DDC/HPD blocks can be independently disabled by engaging their inherent “backdrive” protection. This allows N:1 multiplexing of the low-speed HDMI signals without any additional FET switches.

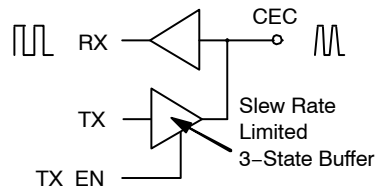
## CONSUMER ELECTRONICS CONTROL (CEC)

The Consumer Electronics Control (CEC) line is a high level command and control protocol, based on a single wire multidrop open drain communication bus running at approximately 1 kHz (See Figure 3). While the HDMI link provides only a single point-to-point connection, up to ten (10) CEC devices may reside on the bus, and they may be daisy chained out through other physical connectors including other HDMI ports or other dedicated CEC links. The high level protocol of CEC can be implemented in a simple microcontroller or other interface with any I/OD (input/open-drain) GPIO.



**Figure 3. Typical μC I/OD Driver**

To limit possible EMI and ringing in this potentially complex connection topology, the rise- and fall-time of this line are limited by the specification. However, meeting the slew-rate limiting requirements with additional discrete circuitry in this bi-directional block is not trivial without an additional RX/TX control line to limit the output slew-rate without affecting the input sensing (See Figure 4).



**Figure 4. Three-Pin External Buffer Control**

Simple CMOS buffers cannot be used in this application since the load can vary so much (total pullup of 27 kΩ to less

than 2 kW, and up to 7.3 nF total capacitance.) The CM2030 targets an output drive slew-rate of less than 100 mV/ms regardless of static load for the CEC line. Additionally, the same internal circuitry will perform active termination, thus reducing ringing and overshoot in entertainment systems connected to legacy or poorly designed CEC nodes.

The CM2030's bi-directional slew rate limiting is integrated into the CEC level-shifter functionality thus allowing the designer to directly interface a simple low voltage CMOS GPIO directly to the CEC bus and simultaneously guarantee meeting all CEC output logic levels and HDMI slew-rate and isolation specifications (See Figure 5).

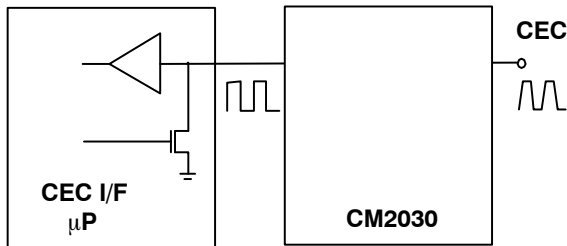


Figure 5. Integrated CM2030 Solution

The CM2030 also includes an internal backdrive protected static pullup 120  $\mu$ A current source from the CE\_SUPPLY rail in addition to the dynamic slew rate control circuitry.

Figure 6 shows a typical shaped CM2030 CEC output (bottom) against a ringing uncontrolled discrete solution (top).

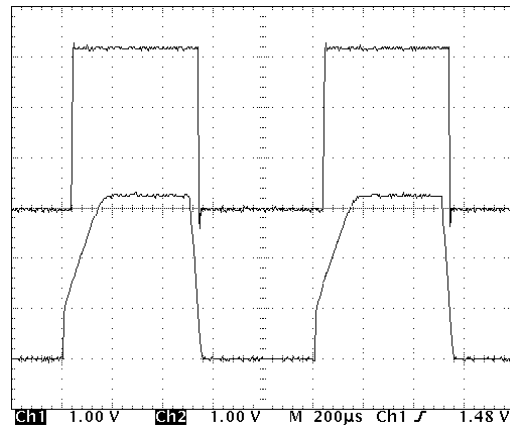


Figure 6. CM2030 CEC Output

HDMI certification requires capacitance measurement of the CEC line to be less than 150 pF per device. Due to the active circuit inside the CM2030 CEC line, CM2030 may cause false readings during the CEC capacitance measurement and not pass the test. The active circuit of the CM2030 CEC line would react with the LCR meter and cause false capacitance readings. There is no issue with the operation of the CM2030 CEC line during normal operations. In fact, CM2030 CEC has shown to improve the signal integrity of the CEC line. CM2030 can be used for applications which do not require HDMI certification or applications which do not use the CEC line.

## HOTPLUG DETECT LOGIC

The CM2030 ensures that the local ASIC will properly detect an HDMI compliant Sink. The current sink maintains a local logic “low” when no system is connected.

A valid pullup on the HDMI connector pin will overdrive the internal pulldown and deliver a logic “high” to the local ASIC.

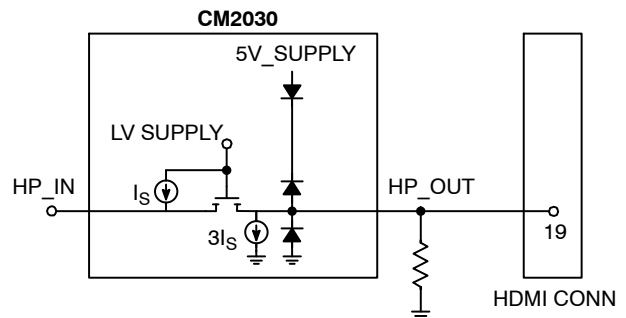


Figure 7. Hotplug Detect Circuit

A 15 K $\Omega$  pull down resistor should be connected between HP\_OUT and ground as required by HDMI specification. There should be no pull up on the HP\_IN, ASIC side of CM2030.

## SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameter                            | Rating                                 | Units |
|--------------------------------------|----------------------------------------|-------|
| V <sub>CC5</sub> , V <sub>CCLV</sub> | 6.0                                    | V     |
| DC Voltage at any Channel Input      | [GND – 0.5] to [V <sub>CC</sub> + 0.5] | V     |
| Storage Temperature Range            | –65 to +150                            | °C    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD (RECOMMENDED) OPERATING CONDITIONS

| Symbol    | Parameter                   | Min | Typ | Max | Units |
|-----------|-----------------------------|-----|-----|-----|-------|
| 5V_SUPPLY | Operating Supply Voltage    | –   | 5   | 5.5 | V     |
| LV_SUPPLY | Bias Supply Voltage         | 1.0 | 3.3 | 5.5 | V     |
| CE_SUPPLY | Bias Supply Voltage         | 3.0 | 3.3 | 3.6 | V     |
| –         | Operating Temperature Range | –40 | –   | 85  | °C    |

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 7)

| Symbol                          | Parameter                                         | Conditions                                                                                                | Min | Typ  | Max  | Units |
|---------------------------------|---------------------------------------------------|-----------------------------------------------------------------------------------------------------------|-----|------|------|-------|
| I <sub>CC5</sub>                | Operating Supply Current                          | 5V_SUPPLY = 5.0 V,<br>CEC_OUT = 3.3 V,<br>LV_SUPPLY = 3.3 V,<br>CE_SUPPLY = 3.3 V, DDC = 5 V<br>(Note 12) |     | 300  | 350  | μA    |
| I <sub>CCLV</sub>               | Bias Supply Current                               | LV_SUPPLY = 3.3 V (Note 12)                                                                               |     | 60   | 150  | μA    |
| I <sub>CCCE</sub>               | Bias Supply Current                               | CE_SUPPLY = 3.3 V, CEC_OUT = 0 V<br>(Notes 12 and 13)                                                     |     | 60   | 150  | μA    |
| I <sub>CEC</sub>                | Current Source on CEC Pin                         | CE_SUPPLY = 3.3 V,                                                                                        | 111 | 120  | 128  | mA    |
| V <sub>DROP</sub>               | 5V_OUT Overcurrent Out Put Drop                   | 5V_SUPPLY = 5.0 V, I <sub>OUT</sub> = 55 mA                                                               |     | 65   | 100  | mV    |
| I <sub>SC</sub>                 | 5V_OUT Short Circuit Current Limit                | 5V_SUPPLY = 5.0 V, 5V_OUT = GND                                                                           | 90  | 135  | 175  | mA    |
| I <sub>OFF</sub>                | OFF State Leakage Current, Level Shifting NFET    | LV_SUPPLY = 0 V                                                                                           |     | 0.1  | 5    | μA    |
| I <sub>BACKDRIVE, CEC</sub>     | Current Through CE-REMOTE_OUT when Powered Down   | CE-REMOTE_IN = CE_SUPPLY < CE_REMOTE_OUT                                                                  |     | 0.1  | 1.8  | μA    |
| I <sub>BACKDRIVE, TMDS</sub>    | Current Through TMDS Pins when Powered Down       | All Supplies = 0 V,<br>TMDS_[2:0]+/-, TMDS_CK+/- = 4 V                                                    |     | 0.1  | 5    | μA    |
| I <sub>BACKDRIVE, 5V_OUT</sub>  | Current Through 5V_OUT when Powered Down          | All Supplies = 0 V,<br>5V_OUT_PIN = 5 V                                                                   |     | 0.1  | 5    | μA    |
| I <sub>BACKDRIVE, DDC</sub>     | Current Through DDC_DAT/CLK_OUT when Powered Down | All Supplies = 0 V,<br>DDC_DAT/CLK_OUT = 5 V,<br>DDC_DAT/CLK_IN = 0 V                                     |     | 0.1  | 5    | μA    |
| I <sub>BACKDRIVE, HOTPLUG</sub> | Current Through HOTPLUG_DET_OUT when Powered Down | All Supplies = 0 V,<br>HOTPLUG_DET_OUT = 5 V,<br>HOTPLUG_IN = 0 V                                         |     | 0.1  | 5    | μA    |
| CEC <sub>SL</sub>               | CEC Slew Limit                                    | Measured from 10–90% or 90–10%                                                                            |     | 0.26 | 0.65 | V/μs  |

7. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

8. Standard IEC61000–4–2, C<sub>DISCHARGE</sub> = 150 pF, R<sub>DISCHARGE</sub> = 330 Ω, 5V\_SUPPLY = 5 V, 3.3V\_SUPPLY = 3.3 V, LV\_SUPPLY = 3.3 V, GND = 0 V.

9. Human Body Model per MIL–STD–883, Method 3015, C<sub>DISCHARGE</sub> = 100 pF, R<sub>DISCHARGE</sub> = 1.5 kΩ, 5V\_SUPPLY = 5V, 3.3V\_SUPPLY = 3.3 V, LV\_SUPPLY = 3.3 V, GND = 0 V.

10. Intra-pair matching, each TMDS pair (i.e. D+, D–)

11. These measurements performed with no external capacitor on V<sub>P</sub> (V<sub>P</sub> floating)

12. These static measurements do not include AC activity on controlled I/O lines.

13. This measurement does not include supply current for the 120 μA current source on the CEC pin.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 7)

| Symbol                    | Parameter                                                                                                              | Conditions                                                                                                | Min        | Typ          | Max          | Units |
|---------------------------|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|------------|--------------|--------------|-------|
| CEC <sub>RT</sub>         | CEC Rise Time                                                                                                          | Measured from 10–90%<br>Assumes a signal swing from 0–3.3 V                                               | 26.4       |              | 250          | μs    |
| CEC <sub>FT</sub>         | CEC Fall Time                                                                                                          | Measured from 90–10%<br>Assumes a signal swing from 0–3.3 V                                               | 4          |              | 50           | μs    |
| V <sub>ACC</sub>          | Turn On Threshold of I <sup>2</sup> C / DDC Accelerator                                                                | Voltage is 0.3 ±10% X 5 V <sub>Supply</sub><br>(Note 8)                                                   | 1.35       | 1.5          | 1.65         | V     |
| V <sub>ON</sub> (DDC_OUT) | Voltage Drop across DDC Level Shifter                                                                                  | LV_SUPPLY = 3.3 V, 3 mA Sink at<br>DDC <sub>IN</sub> , DDCOUT < V <sub>ACC</sub>                          |            | 150          | 225          | mV    |
| V <sub>OL</sub> (DDC_IN)  | Logic Level (ASIC side) when I <sup>2</sup> C / DDC Logic<br>Low Applied (I <sup>2</sup> C Pass-through Compatibility) | DDC_OUT = 0.4 V,<br>LV_SUPPLY = 3.3 V, 1.5 kΩ pullup on<br>DDC_OUT to 5.0 V (Note 8)                      |            | 0.3          | 0.4          | V     |
| tr(DDC)                   | DDC_OUT Line Risettime,<br>V <sub>ACC</sub> < V <sub>DDC_OUT</sub> < (5V <sub>Supply</sub> – 0.5 V)                    | DDC_IN floating, LV_SUPPLY = 3.3 V,<br>1.5 kΩ pullup on DDC_OUT to 5.0 V,<br>Bus Capacitance = 1500 pF    |            |              | 1            | μs    |
| V <sub>F</sub>            | Diode Forward Voltage<br>Top Diode<br>Bottom Diode                                                                     | IF = 8 mA, T <sub>A</sub> = 25°C                                                                          | 0.6<br>0.6 | 0.85<br>0.85 | 0.95<br>0.95 | V     |
| V <sub>ESD</sub>          | ESD Withstand Voltage (IEC)                                                                                            | Pins 4, 7, 10, 13, 20, 21, 22, 23, 24, 27,<br>30, 33, T <sub>A</sub> = 25°C (Note 8)                      | ±8         |              |              | kV    |
| V <sub>ESD</sub>          | ESD Withstand Voltage (HBM)                                                                                            | Pins 1, 2, 16, 17, 18, 19, 37, 38,<br>T <sub>A</sub> = 25°C                                               | ±2         |              |              | kV    |
| V <sub>CL</sub>           | Channel Clamp Voltage<br>Positive Transients<br>Negative Transients                                                    | T <sub>A</sub> = 25°C, I <sub>PP</sub> = 1 A, t <sub>P</sub> = 8/20 μS<br>(Note 11)                       |            | 11.0<br>2.0  |              | V     |
| R <sub>DYN</sub>          | Dynamic Resistance<br>Positive Transients<br>Negative Transients                                                       | T <sub>A</sub> = 25°C, I <sub>PP</sub> = 1 A, t <sub>P</sub> = 8/20 μS<br>Any I/O pin to Ground (Note 11) |            | 1.4<br>0.9   |              | Ω     |
| I <sub>LEAK</sub>         | TMDS Channel Leakage Current                                                                                           | T <sub>A</sub> = 25°C                                                                                     |            | 0.01         | 1            | μA    |
| C <sub>IN</sub> , TMDS    | TMDS Channel Input Capacitance                                                                                         | 5V_SUPPLY = 5.0 V, Measured at<br>1 MHz, V <sub>BIAS</sub> = 2.5 V                                        |            | 0.9          | 1.2          | pF    |
| ΔC <sub>IN</sub> , TMDS   | TMDS Channel Input Capacitance Matching                                                                                | 5V_SUPPLY = 5.0 V, Measured at<br>1 MHz, V <sub>BIAS</sub> = 2.5 V (Note 10)                              |            | 0.05         |              | pF    |
| C <sub>MUTUAL</sub>       | Mutual Capacitance between Signal Pin and<br>Adja Cent Signal Pin                                                      | 5V_SUPPLY = 0 V,<br>Measured at 1 MHz, V <sub>BIAS</sub> = 2.5 V                                          |            | 0.07         |              | pF    |
| C <sub>IN</sub> , DDCOUT  | Level Shifting Input Capacitance, Capacitance<br>to GND                                                                | 5V_SUPPLY = 0 V,<br>Measured at 100 kHz, V <sub>BIAS</sub> = 2.5 V                                        |            | 10           |              | pF    |
| C <sub>IN</sub> , CECOUT  | Level Shifting Input Capacitance, Capacitance<br>to GND                                                                | 5V_SUPPLY = 0 V,<br>Measured at 100 kHz, V <sub>BIAS</sub> = 1.65 V                                       |            | 10           |              | pF    |
| C <sub>IN</sub> , HPOUT   | Level Shifting Input Capacitance, Capacitance<br>to GND                                                                | 5V_SUPPLY = 0 V,<br>Measured at 100 kHz, V <sub>BIAS</sub> = 2.5 V                                        |            | 10           |              | pF    |

7. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

8. Standard IEC61000-4-2, C<sub>DISCHARGE</sub> = 150 pF, R<sub>DISCHARGE</sub> = 330 Ω, 5V\_SUPPLY = 5 V, 3.3V\_SUPPLY = 3.3 V, LV\_SUPPLY = 3.3 V, GND = 0 V.

9. Human Body Model per MIL-STD-883, Method 3015, C<sub>DISCHARGE</sub> = 100 pF, R<sub>DISCHARGE</sub> = 1.5 kΩ, 5V\_SUPPLY = 5V, 3.3V\_SUPPLY = 3.3 V, LV\_SUPPLY = 3.3 V, GND = 0 V.

10. Intra-pair matching, each TMDS pair (i.e. D+, D-)

11. These measurements performed with no external capacitor on V<sub>P</sub> (V<sub>P</sub> floating)

12. These static measurements do not include AC activity on controlled I/O lines.

13. This measurement does not include supply current for the 120 μA current source on the CEC pin.

## PERFORMANCE INFORMATION

Typical Filter Performance ( $T_A = 25^\circ\text{C}$ , DC Bias = 0 V, 50  $\Omega$  Environment)

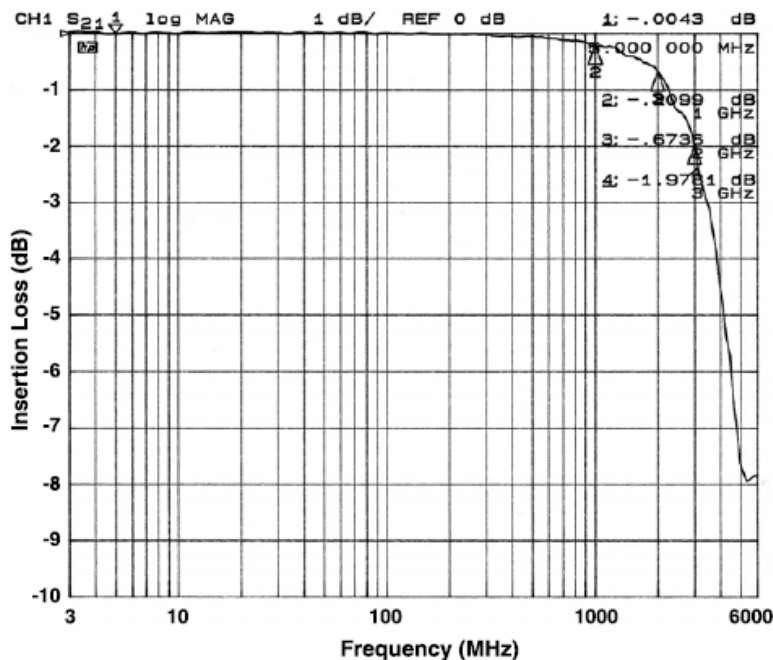


Figure 8. Insertion Loss vs. Frequency (TMDS\_D1- to GND)

## APPLICATION INFORMATION

## Design Considerations

## 5V\_OUT (pin 38)

Maximum overcurrent protection output drop at 55 mA on 5V\_OUT is 100 mV. To meet HDMI output requirements of 4.8–5.3 V, an input of greater than 4.9 V should be used (i.e.  $5.1\text{ V} \pm 4\%$ )

## DUT On vs. DUT Off

Many HDMI CTS tests require a power off condition on the System Under Test. Many discrete ESD diode configurations can be forward biased when their VDD rail is lower than the I/O pin bias, thereby exhibiting extremely high apparent capacitance measurements, for example. The *MediaGuard*™ backdrive isolation circuitry limits this current to less than 5 mA, and will help ensure HDMI compliance.

## APPLICATION INFORMATION (Cont'd)



### Figure 9. Typical Application for CM2030

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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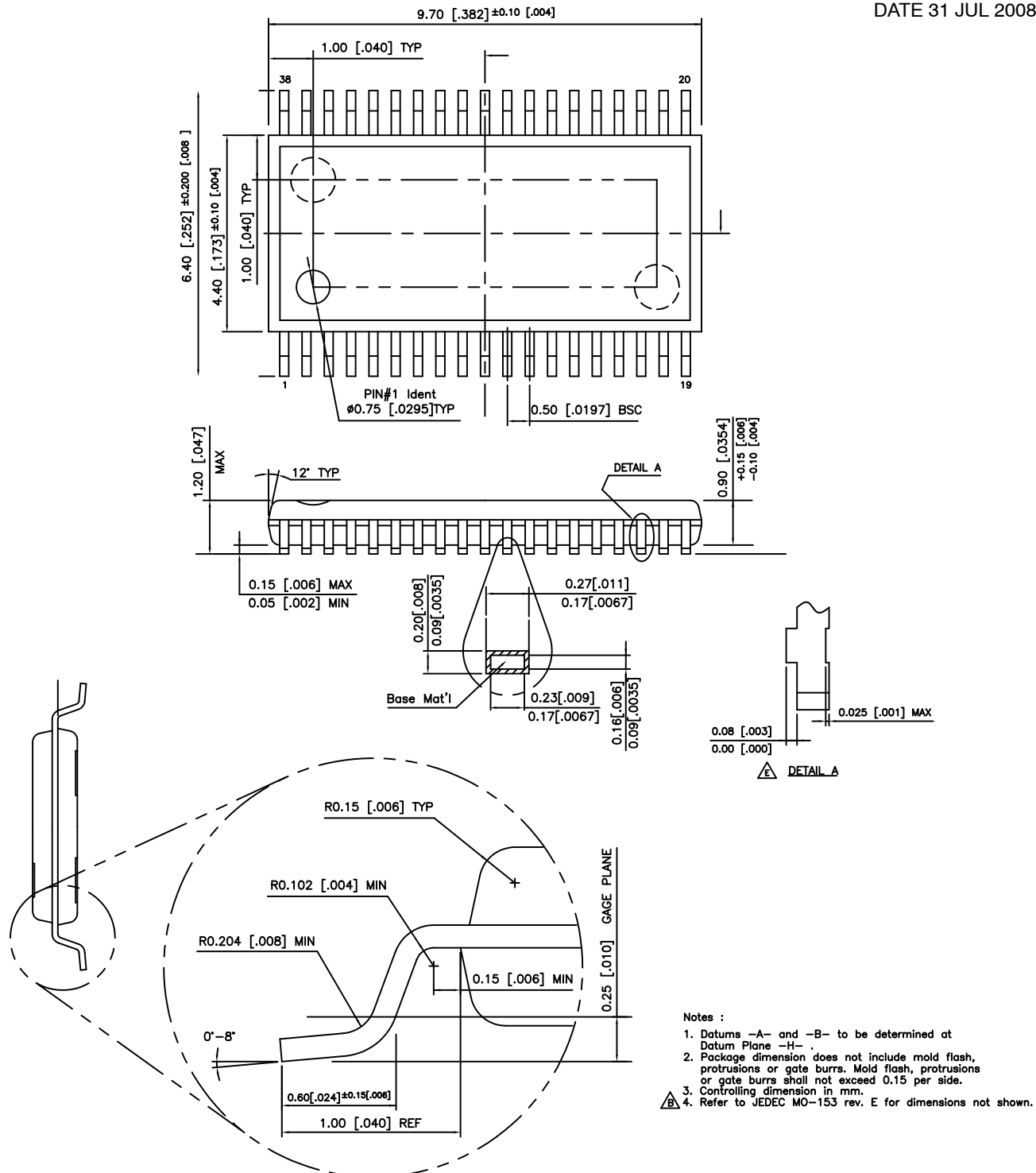
ON

### TSSOP 38

#### CASE 948AG-01

#### ISSUE O

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