

FEATURES

- 25Ω cutoff bus output
- Extended 100E VEE range of -4.2V to -5.5V
- 50Ω receiver output
- Transmit and receive registers
- 1500ps max. clock to bus
- 1000ps max. clock to Q
- Internal edge slow-down capacitors on bus outputs
- Additional package ground pins
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E336
- Available in 28-pin PLCC package

DESCRIPTION

The SY10/100E336 offer three bus transceivers with both transmit and receive registers and are designed for use in new, high-performance ECL systems. The bus outputs (BUS₀ - BUS₂) are designed to drive a 25Ω bus. The receive outputs (Q₀ - Q₂) are specified for 50Ω. The bus outputs feature a normal logic HIGH level (V_{OH}) and a cutoff LOW level when at a logic LOW. At cutoff, the outputs go to -2.0V and the output emitter-follower is "off", presenting a high impedance to the bus. The bus outputs have edge slow-down capacitors.

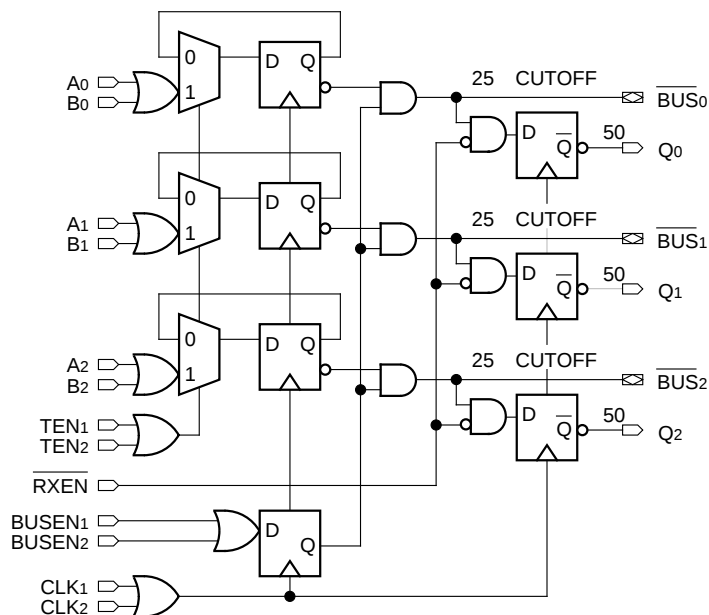
The Transmit Enable pins (TEN) determine whether current data is held in the transmit register or new data is loaded from the A/B inputs. A logic LOW on both of the bus enable inputs (BUSEN), when clocked through the register, disables the bus outputs to -2.0V.

The receiver section clocks bus data into the receive registers after gating with the Receive Enable (RXEN) input.

All registers are clocked by rising edge of CLK₁ or CLK₂ (or both).

Additional grounding is provided through the ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

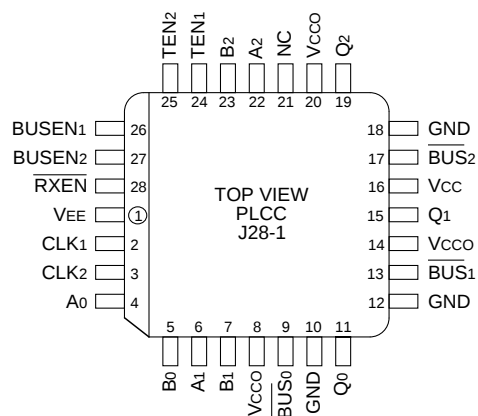
BLOCK DIAGRAM



PIN NAMES

Pin	Function
A ₀ -A ₂	Data Inputs A
B ₀ -B ₂	Data Inputs B
TEN _{1, 2}	Transmit Enable Inputs
RXEN	Receive Enable Input
BUSEN _{1, 2}	Bus Enable Inputs
CLK _{1, 2}	Clock Inputs
BUS ₀ -BUS ₂	25Ω Cutoff Bus Outputs
Q ₀ -Q ₂	Receive Data Outputs
Vcco	Vcc to Output

PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾

28-Pin PLCC (J28-1)

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E336JC	J28-1	Commercial	SY10E336JC	Sn-Pb
SY10E336JCTR ⁽²⁾	J28-1	Commercial	SY10E336JC	Sn-Pb
SY100E336JC	J28-1	Commercial	SY100E336JC	Sn-Pb
SY100E336JCTR ⁽²⁾	J28-1	Commercial	SY100E336JC	Sn-Pb
SY10E336JZ ⁽³⁾	J28-1	Commercial	SY10E336JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E336JZTR ^(2, 3)	J28-1	Commercial	SY10E336JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E336JZ ⁽³⁾	J28-1	Commercial	SY100E336JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E336JZTR ^(2, 3)	J28-1	Commercial	SY100E336JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

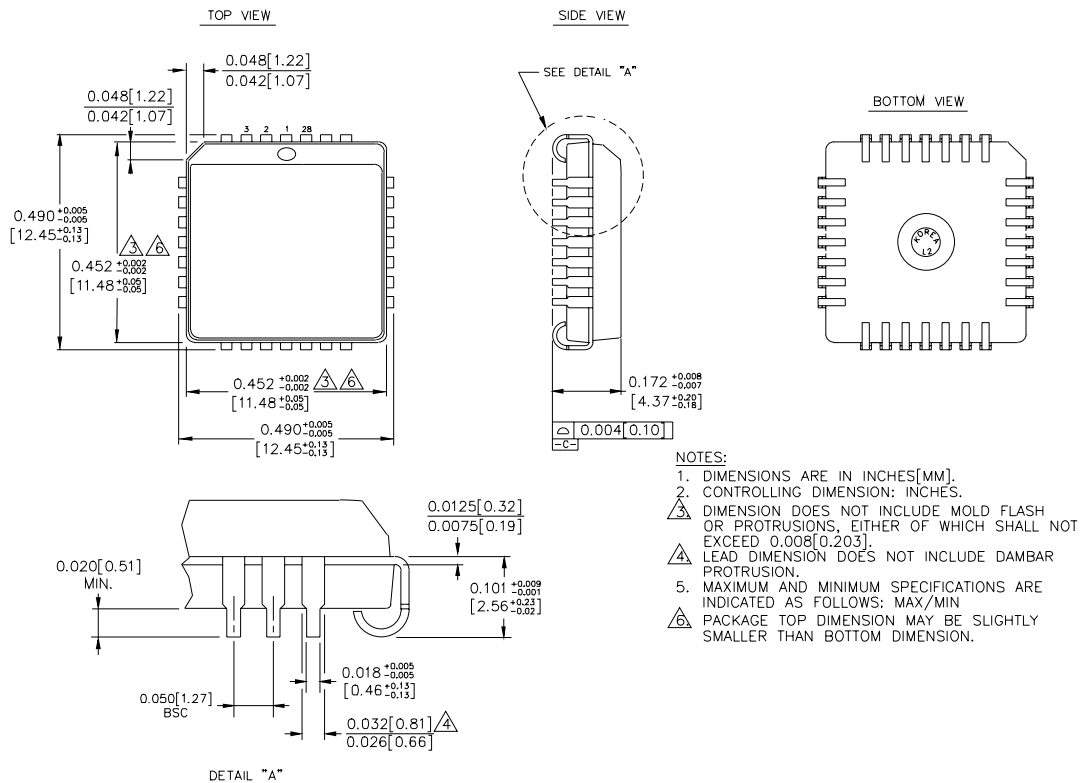
1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V _{CUT}	Cut-off Output Voltage	-2.10	—	-2.03	-2.10	—	-2.03	-2.10	—	-2.03	V	1
I _{IH}	Input HIGH Current RXEN All Other Inputs	— —	— —	225 150	— —	— —	225 150	— —	— —	225 150	μA	—
I _{EE}	Power Supply Current 10E 100E	— —	125 125	150 150	— —	125 125	150 150	— —	125 144	150 173	mA	—

Note:1. Measured with V_{TT} = -2.10V.**AC ELECTRICAL CHARACTERISTICS**V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PD}	Propagation Delay to Output CLK to Q CLK to $\overline{\text{BUS}}$	500 825	700 1250	1000 1800	500 825	700 1250	1000 1800	500 825	700 1250	1000 1800	ps	—
t _S	Set-up Time BUS, RXEN BUSEN A, B Data TEN	150 100 300 450	-150 -200 -50 150	— — — —	150 100 300 450	-150 -200 -50 150	— — — —	150 100 300 450	-150 -200 -50 150	— — — —	ps	—
t _H	Hold Time BUS, RXEN BUSEN A, B Data TEN	450 500 350 200	150 200 50 -150	— — — —	450 500 350 200	150 200 50 -150	— — — —	450 500 350 200	150 200 50 -150	— — — —	ps	—
t _{PW}	Minimum Pulse Width, CLK	400	—	—	400	—	—	400	—	—	ps	—
t _r t _f	Rise/Fall Time 20% to 80% (Q _n) 20% to 80% (BUS _n Rise) 20% to 80% (BUS _n Fall)	300 500 300	450 800 500	700 1000 800	300 500 300	450 800 500	700 1000 800	300 500 300	450 800 500	700 1000 800	ps	—

28-PIN PLCC (J28-1)

Rev. 03

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