



T-46-09-05

54F/74F164

Serial-In, Parallel-Out Shift Register

General Description

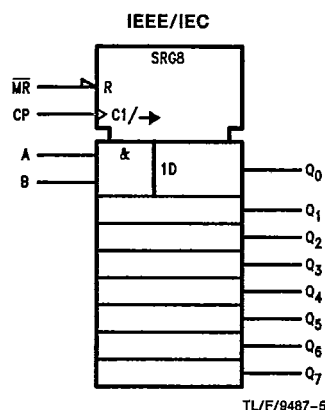
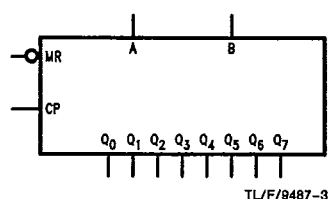
The 'F164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

Features

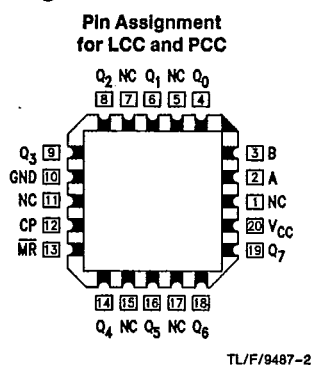
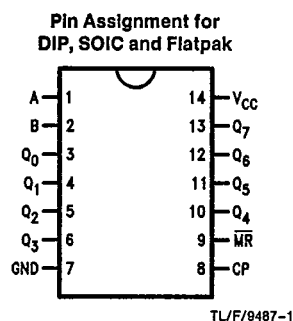
- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers

Ordering Code: See Section 5

Logic Symbols



Connection Diagrams



Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A, B	Data Inputs	1.0/1.0	20 μ A / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A / -0.6 mA
MR	Master Reset Input (Active LOW)	1.0/1.0	20 μ A / -0.6 mA
Q0-Q7	Outputs	50/33.3	-1 mA / 20 mA

Functional Description

The 'F164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

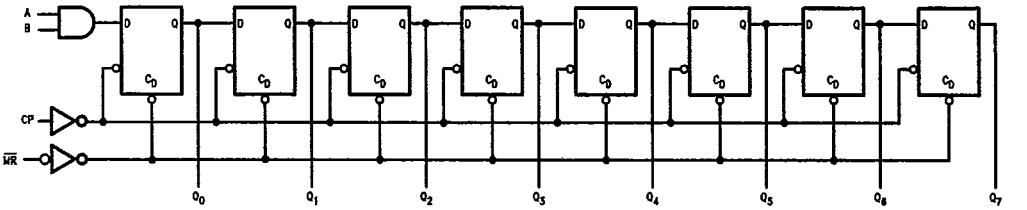
Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q₀ the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q ₀	Q ₁ -Q ₇
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q ₀ -q ₈
	H	l	h	L	q ₀ -q ₈
	H	h	l	L	q ₀ -q ₈
	H	h	h	H	q ₀ -q ₈

H(h) = HIGH Voltage Levels
L(l) = LOW Voltage Levels
X = Immaterial
q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

T-46-09-05

164

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C

V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
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Input Voltage (Note 2)	-0.5V to +7.0V
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Input Current (Note 2)	-30 mA to +5.0 mA
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Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	-0.5V to V _{CC}
Standard Output	-0.5V to +5.5V
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
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Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	-55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.5 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
I _{IH}	Input HIGH Current			20	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			100	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CEX}	Output HIGH Leakage Current			250	μA	Max	V _{OUT} = V _{CC}
I _{CC}	Power Supply Current		35	55	mA	Max	CP = HIGH MR = GND, A, B = GND

T-46-09-05

164

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	90		50		80		MHz	2-1
t_{PLH}	Propagation Delay CP to Q_n	3.5	6.0	8.0	3.5	11.0	4.5	9.0	ns	2-3
t_{PHL}	Propagation Delay CP to Q_n	5.0	7.5	10.0	4.0	13.0	5.0	11.0		
t_{PHL}	Propagation Delay $\overline{\text{MR}}$ to Q_n	5.5	10.5	13.0	5.5	16.0	5.5	14.0	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{MII}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	7.0		7.0		7.0		ns	2-6
$t_s(\text{L})$	A or B to CP	7.0		7.0		7.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	1.0		1.0		1.0		ns	2-6
$t_h(\text{L})$	A or B to CP	1.0		1.0		1.0			
$t_w(\text{H})$	CP Pulse Width	4.0		4.0		4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	7.0		7.0		7.0			
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	7.0		7.0		7.0		ns	2-4
t_{rec}	Recovery Time $\overline{\text{MR}}$ to CP	7.0		7.0		7.0		ns	2-6