

CBTD3861

10-bit level shifting bus switch with output enable

Rev. 2 — 21 November 2011

Product data sheet

1. General description

The CBTD3861 provides ten bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBTD3861 device is organized as one 10-bit bus switches with one output enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the switch is on and port A is connected to the B port. When $\overline{OE}$ is HIGH, each switch is disabled.

The CBTD3861 is characterized for operation from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

2. Features and benefits

- Designed to be used in 5 V to 3.3 V level shifting applications with internal diode
- $5\text{ }\Omega$ switch connection between two ports
- TTL-compatible control input levels
- Multiple package options
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ CDM JESD22-C101C exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBTD3861PW	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
CBTD3861DK	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP24 ^[1]	plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT556-1
CBTD3861BQ	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body $3.5 \times 5.5 \times 0.85\text{ mm}$	SOT815-1

[1] Also known as QSOP24 package



4. Functional diagram

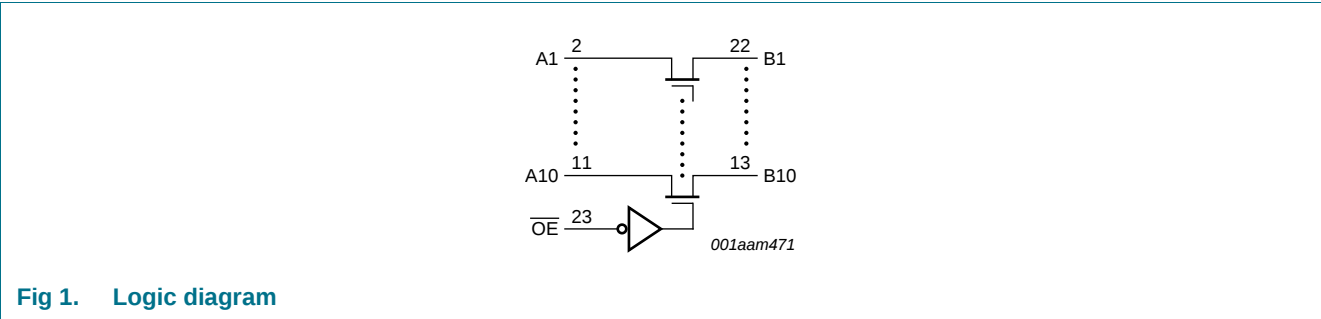


Fig 1. Logic diagram

5. Pinning information

5.1 Pinning

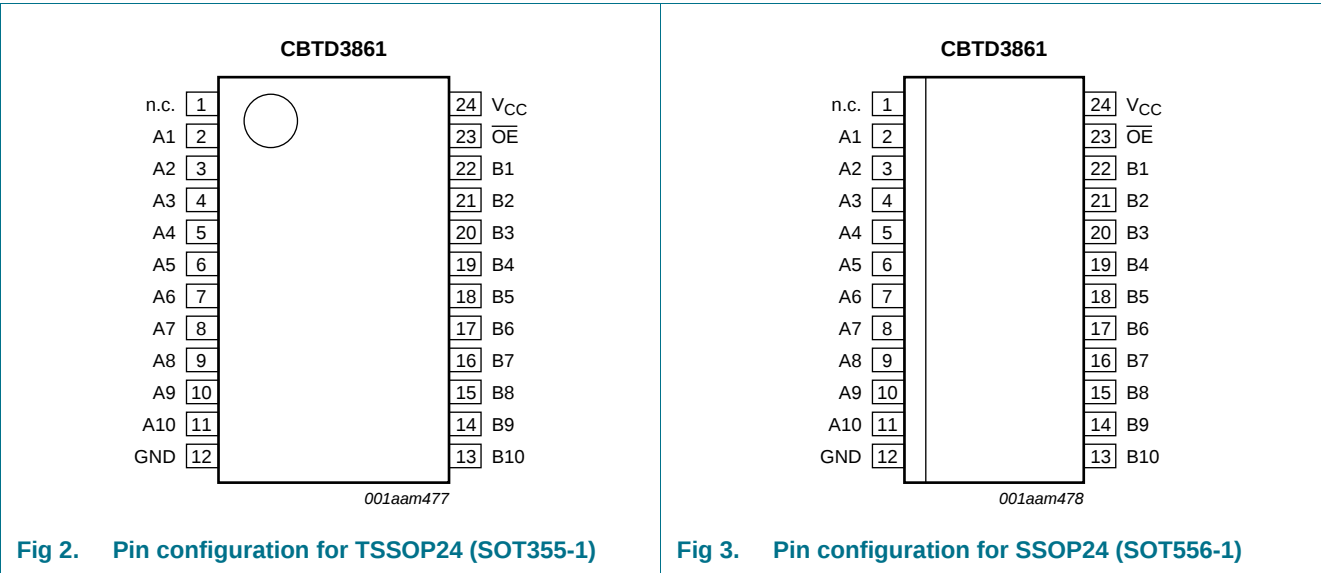
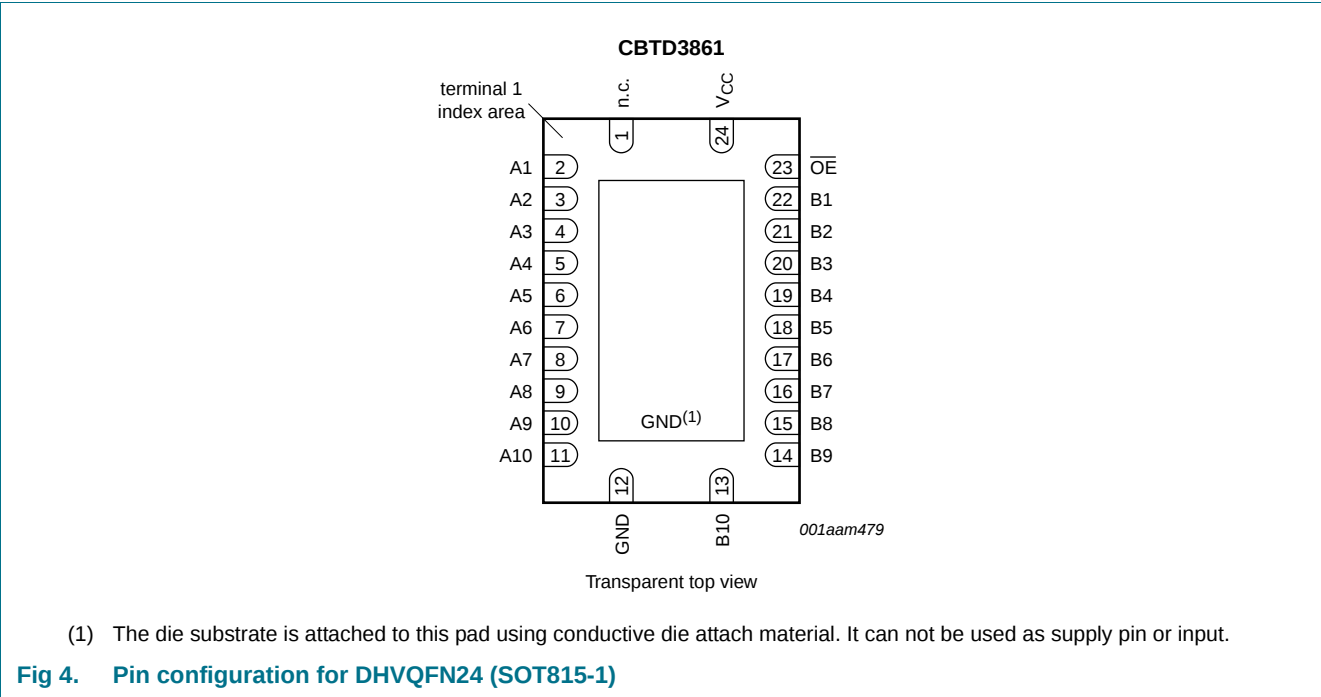


Fig 2. Pin configuration for TSSOP24 (SOT355-1)

Fig 3. Pin configuration for SSOP24 (SOT556-1)



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A1 to A10	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	data input/output (A port)
GND	12	ground (0 V)
B1 to B10	22, 21, 20, 19, 18, 17, 16, 15, 14, 13	data input/output (B port)
OE	23	output enable input (active LOW)
VCC	24	positive supply voltage

6. Functional description

Table 3. Function selection^[1]

Input	Input/output
OE	An, Bn
L	An = Bn
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		^[2] -0.5	+7.0	V
I_O	output current	$V_O < 0\text{ V}$	-	± 128	mA
I_{IK}	input clamping current	$V_{I/O} = 0\text{ V}$	-50	-	mA
T_{stg}	storage temperature		-65	+150	$^{\circ}\text{C}$

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 8](#), is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free air	-40	-	+85	$^{\circ}\text{C}$

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

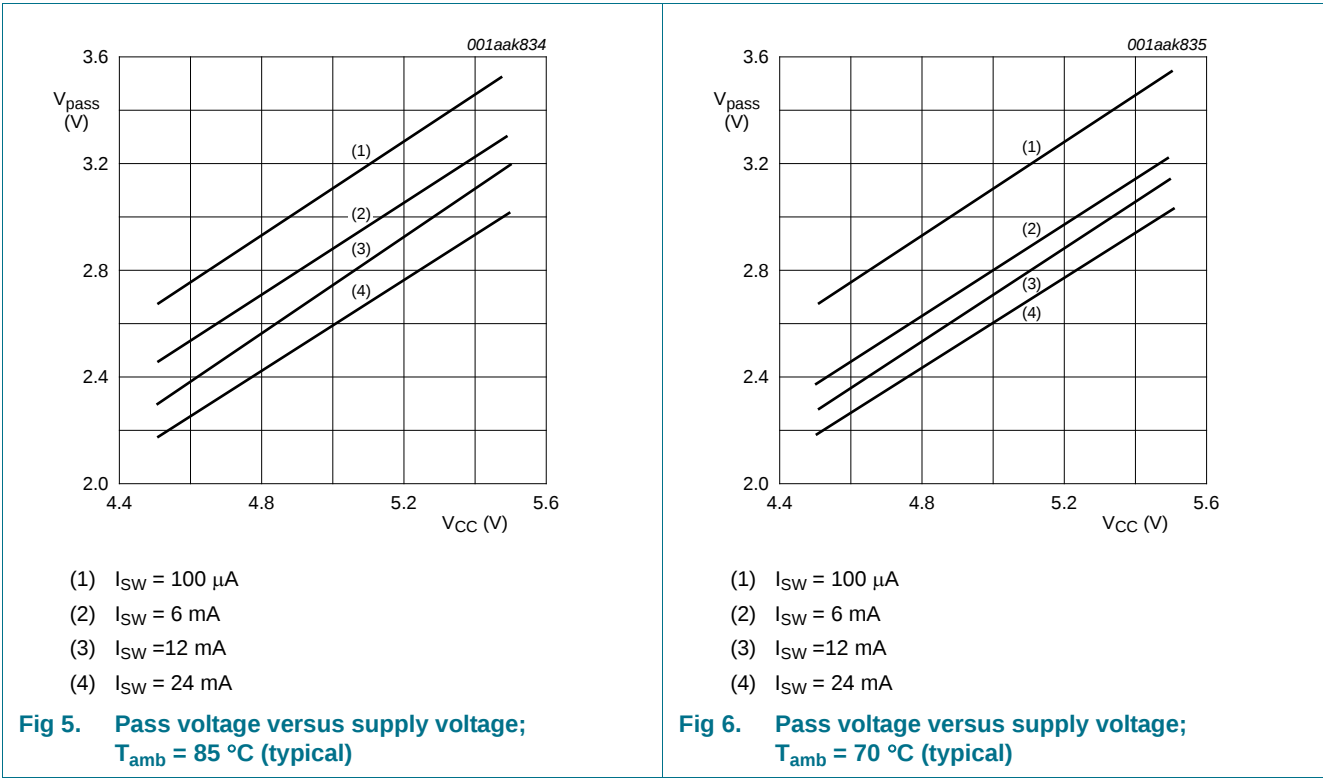
Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$			Unit
			Min	Typ ^[1]	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5\text{ V}$; $I_I = -18\text{ mA}$	-	-	-1.2	V
I_I	input leakage current	$V_{CC} = 5.5\text{ V}$; $V_I = \text{GND}$ or 5.5 V	-	-	± 1	μA
I_{CC}	supply current	$V_{CC} = 5.5\text{ V}$; $I_O = 0\text{ mA}$; $V_I = V_{CC}$ or GND	-	-	1.5	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 5.5\text{ V}$; one input at 3.4 V, other inputs at V_{CC} or GND ^[2]	-	-	2.5	mA
V_{pass}	pass voltage	see Figure 5 to Figure 9	-	-	-	V
C_I	input capacitance	control pins; $V_I = 3\text{ V}$ or 0 V	-	2.5	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; $V_I = 3\text{ V}$ or 0 V ; $\overline{OE} = V_{CC}$	-	4.0	-	pF

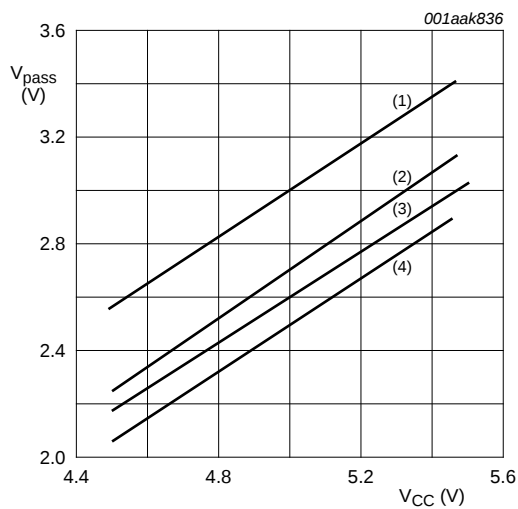
Table 6. Static characteristics ...continued
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
R _{ON}	ON resistance	V _{CC} = 4.5 V; V _I = 0 V; I _I = 64 mA ^[3]	-	5	7	Ω
		V _{CC} = 4.5 V; V _I = 0 V; I _I = 30 mA ^[3]	-	5	7	Ω
		V _{CC} = 4.5 V; V _I = 2.4 V; I _I = -15 mA ^[3]	-	17	50	Ω

- [1] All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
- [2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
- [3] Measured by the voltage drop between the nAn and the nBn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nAn or nBn) terminals.

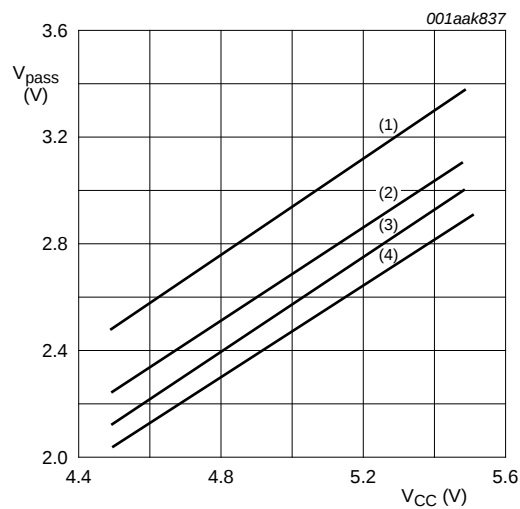
9.1 Typical pass voltage graphs





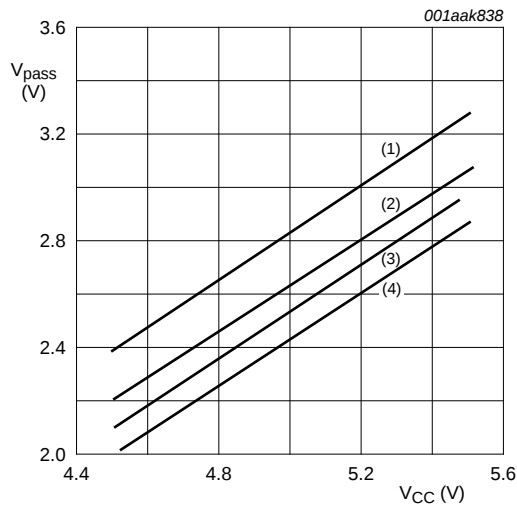
- (1) $I_{SW} = 100 \mu A$
- (2) $I_{SW} = 6 \text{ mA}$
- (3) $I_{SW} = 12 \text{ mA}$
- (4) $I_{SW} = 24 \text{ mA}$

Fig 7. Pass voltage versus supply voltage; $T_{amb} = 25 \text{ }^{\circ}\text{C}$ (typical)



- (1) $I_{SW} = 100 \mu A$
- (2) $I_{SW} = 6 \text{ mA}$
- (3) $I_{SW} = 12 \text{ mA}$
- (4) $I_{SW} = 24 \text{ mA}$

Fig 8. Pass voltage versus supply voltage; $T_{amb} = 0 \text{ }^{\circ}\text{C}$ (typical)



- (1) $I_{SW} = 100 \mu A$
- (2) $I_{SW} = 6 \text{ mA}$
- (3) $I_{SW} = 12 \text{ mA}$
- (4) $I_{SW} = 24 \text{ mA}$

Fig 9. Pass voltage versus supply voltage; $T_{amb} = -40 \text{ }^{\circ}\text{C}$ (typical)

10. Dynamic characteristics

Table 7. Dynamic characteristics

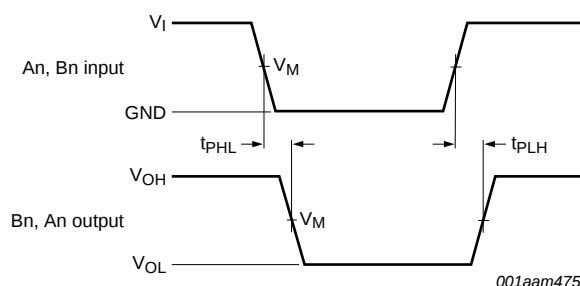
Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$			Unit
			Min	Typ	Max	
t_{pd}	propagation delay	An, Bn to Bn, An; see Figure 10 [1][2] $V_{\text{CC}} = 5.0\text{ V} \pm 0.5\text{ V}$	-	-	0.25	ns
t_{en}	enable time	$\overline{\text{OE}}$ to An or Bn; see Figure 11 [2] $V_{\text{CC}} = 5.0\text{ V} \pm 0.5\text{ V}$	1.8	4.3	10.0	ns
t_{dis}	disable time	$\overline{\text{OE}}$ to An or Bn; see Figure 11 [2] $V_{\text{CC}} = 5.0\text{ V} \pm 0.5\text{ V}$	1.0	3.0	6.0	ns

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .
 t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{dis} is the same as t_{PLZ} and t_{PHZ} .

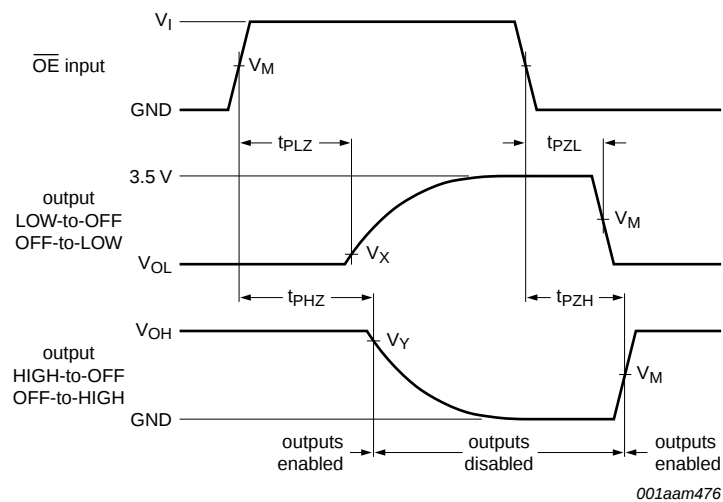
11. Waveforms



Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. The data input (An, Bn) to output (Bn, An) propagation delay times



Measurement points are given in [Table 8](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

12. Test information

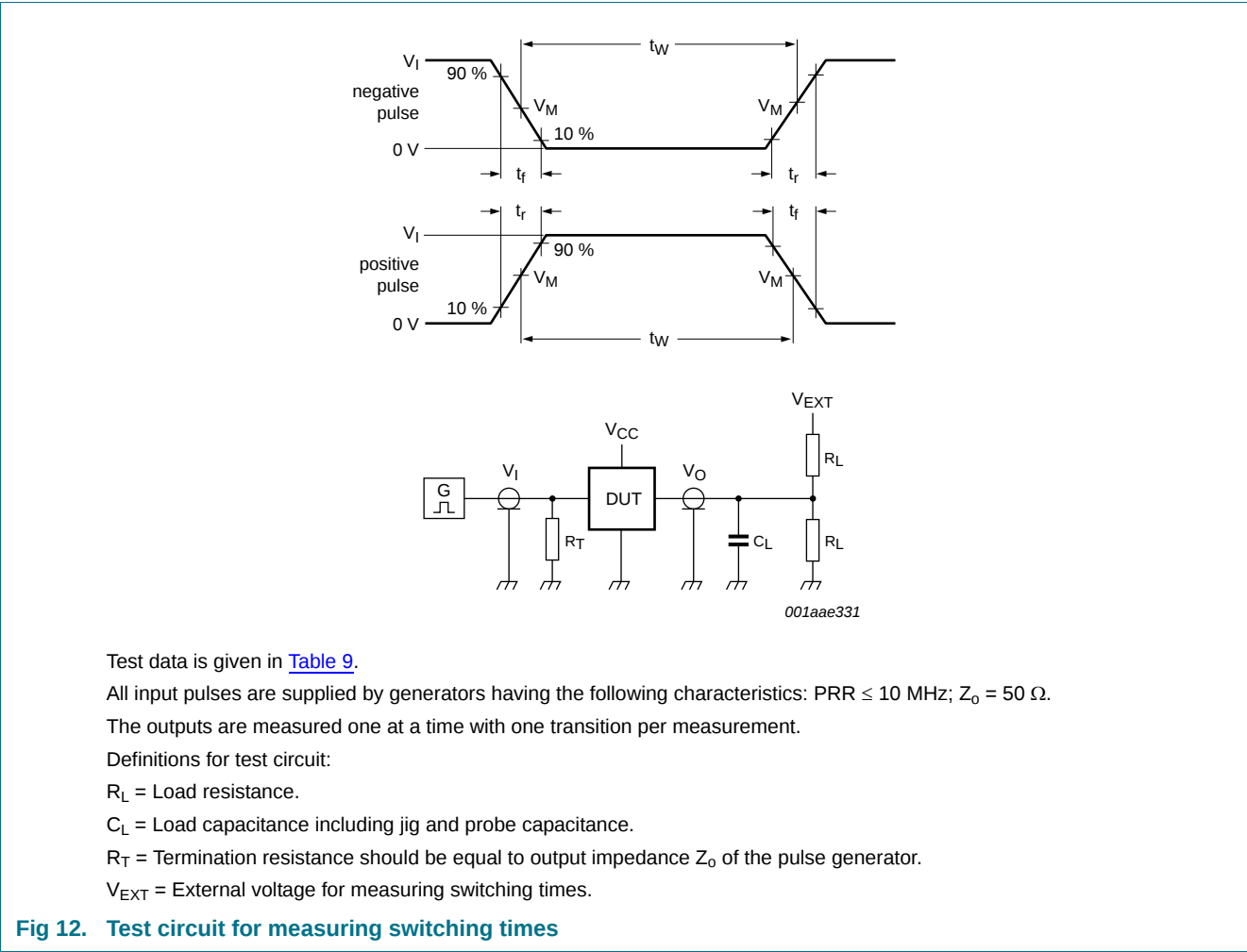


Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
V _{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

13. Package outline

SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm SOT556-1

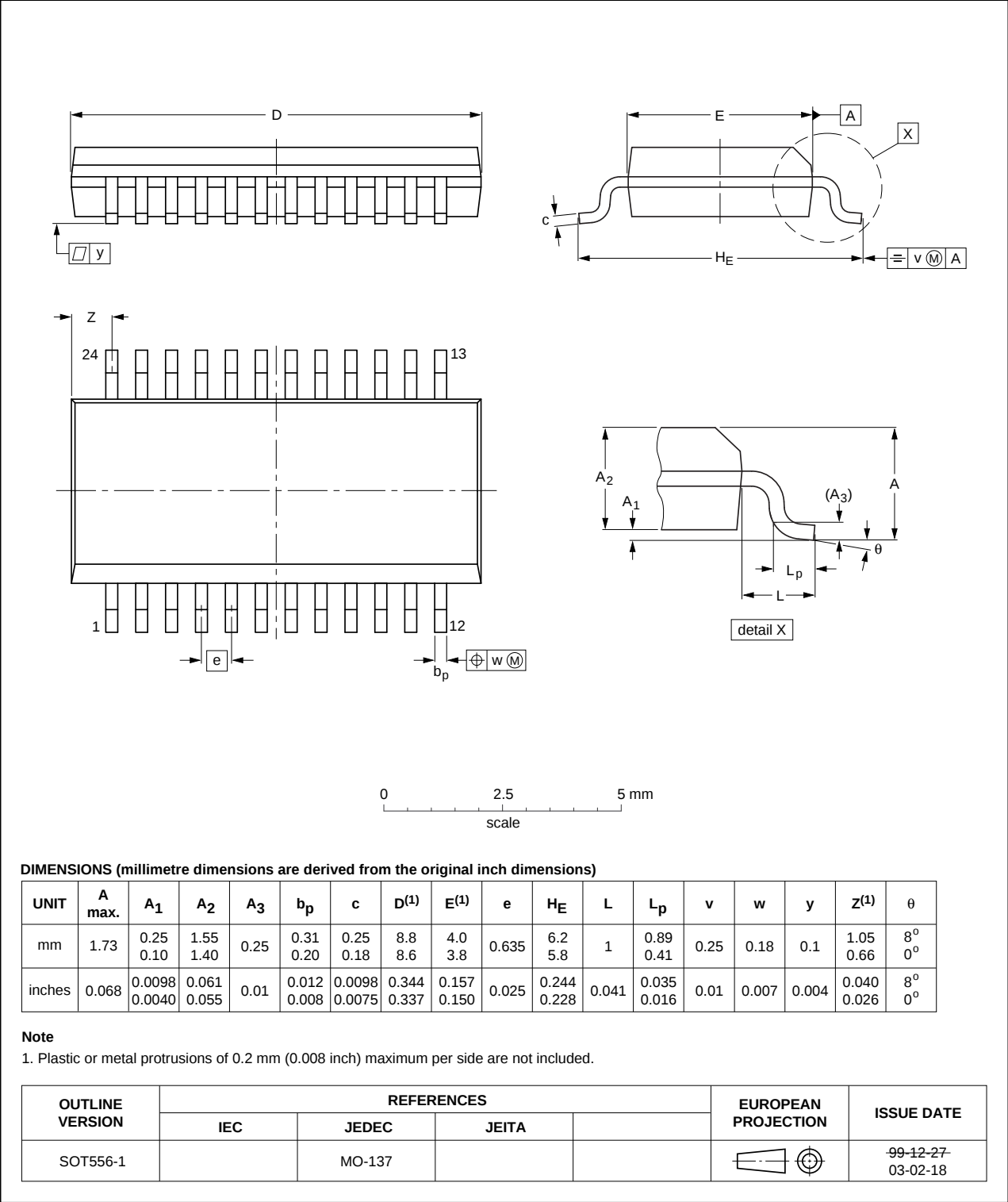


Fig 13. Package outline SOT556-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

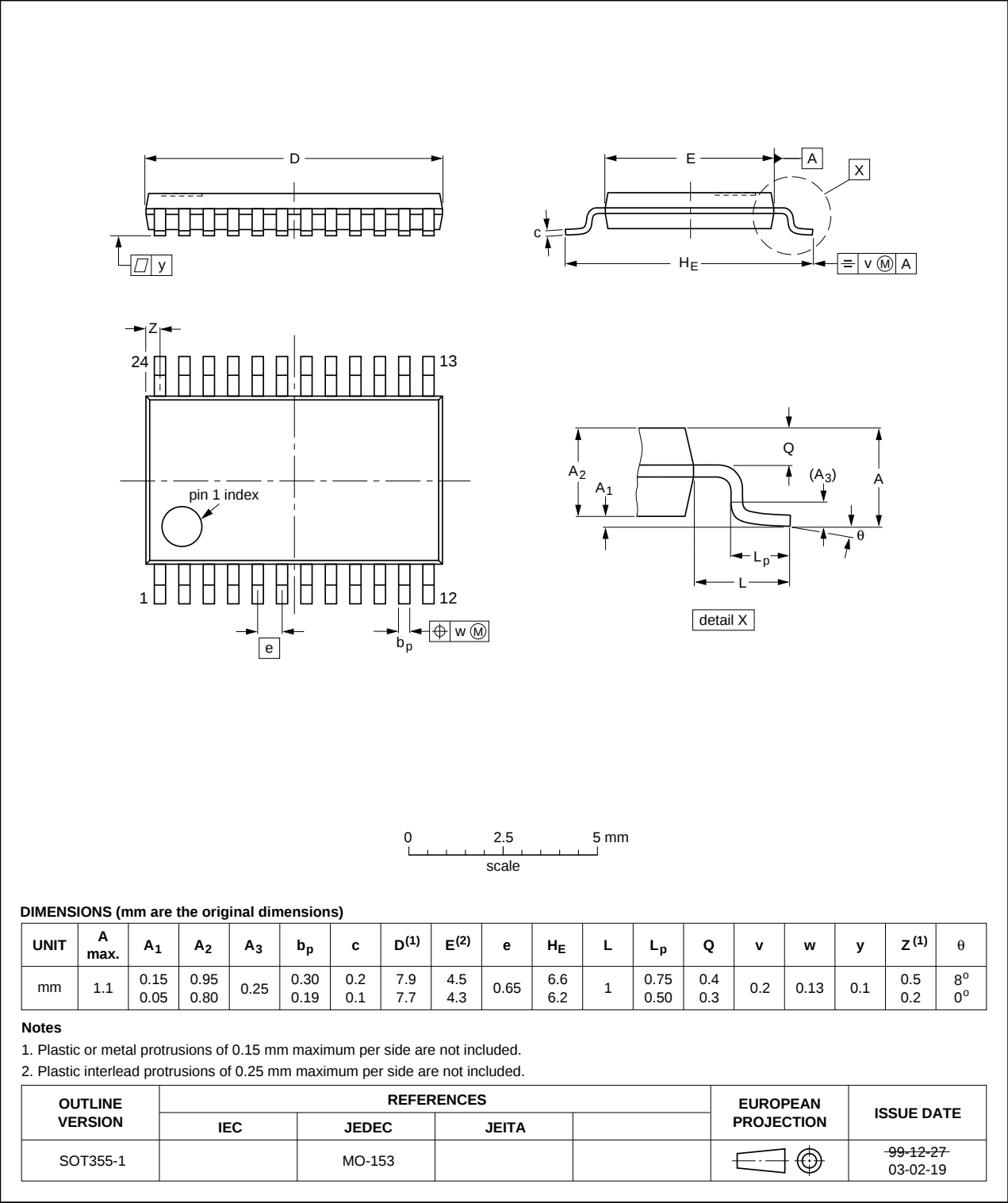


Fig 14. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;
 no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

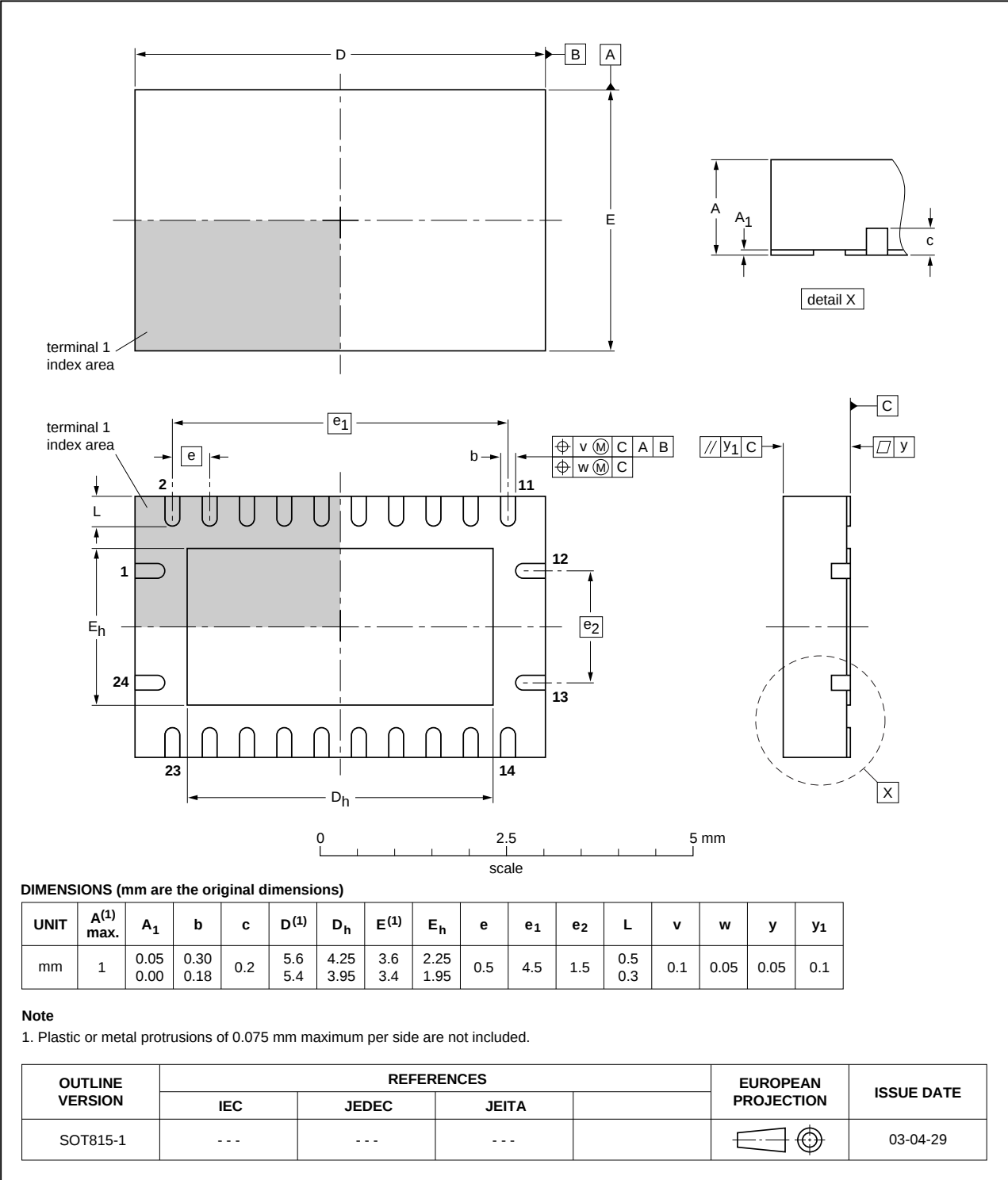


Fig 15. Package outline SOT815-1 (DHVQFN24)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTD3861 v.2	20111121	Product data sheet	-	CBTD3861 v.1
Modifications:	• Legal pages updated.			
CBTD3861 v.1	20100819	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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