

# SN74LS257B, SN74LS258B

## Quad 2-Input Multiplexer with 3-State Outputs

The LSTTL/MSI SN74LS257B and the SN74LS258B are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (EO) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process For High Speed
- Multiplexer Expansion By Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

### GUARANTEED OPERATING RANGES

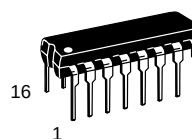
| Symbol          | Parameter                           | Min  | Typ | Max  | Unit |
|-----------------|-------------------------------------|------|-----|------|------|
| V <sub>CC</sub> | Supply Voltage                      | 4.75 | 5.0 | 5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 0    | 25  | 70   | °C   |
| I <sub>OH</sub> | Output Current – High               |      |     | –2.6 | mA   |
| I <sub>OL</sub> | Output Current – Low                |      |     | 24   | mA   |



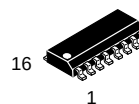
ON Semiconductor™

<http://onsemi.com>

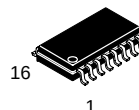
**LOW  
POWER  
SCHOTTKY**



PLASTIC  
N SUFFIX  
CASE 648



SOIC  
D SUFFIX  
CASE 751B



SOEIAJ  
M SUFFIX  
CASE 966

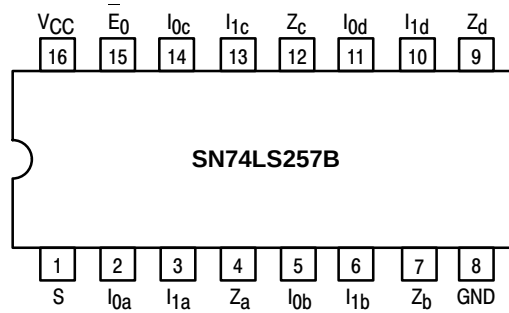
### ORDERING INFORMATION

| Device        | Package    | Shipping         |
|---------------|------------|------------------|
| SN74LS257BN   | 16 Pin DIP | 2000 Units/Box   |
| SN74LS257BD   | SOIC–16    | 38 Units/Rail    |
| SN74LS257BDR2 | SOIC–16    | 2500/Tape & Reel |
| SN74LS257BM   | SOEIAJ–16  | See Note 1       |
| SN74LS257BMEL | SOEIAJ–16  | See Note 1       |
| SN74LS258BN   | 16 Pin DIP | 2000 Units/Box   |
| SN74LS258BD   | SOIC–16    | 38 Units/Rail    |
| SN74LS258BDR2 | SOIC–16    | 2500/Tape & Reel |
| SN74LS258BM   | SOEIAJ–16  | See Note 1       |
| SN74LS258BMEL | SOEIAJ–16  | See Note 1       |

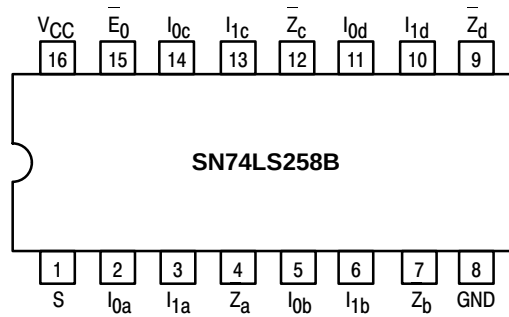
1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

## SN74LS257B, SN74LS258B

### CONNECTION DIAGRAM DIP (TOP VIEW)



$V_{CC}$  = PIN 16  
GND = PIN 8

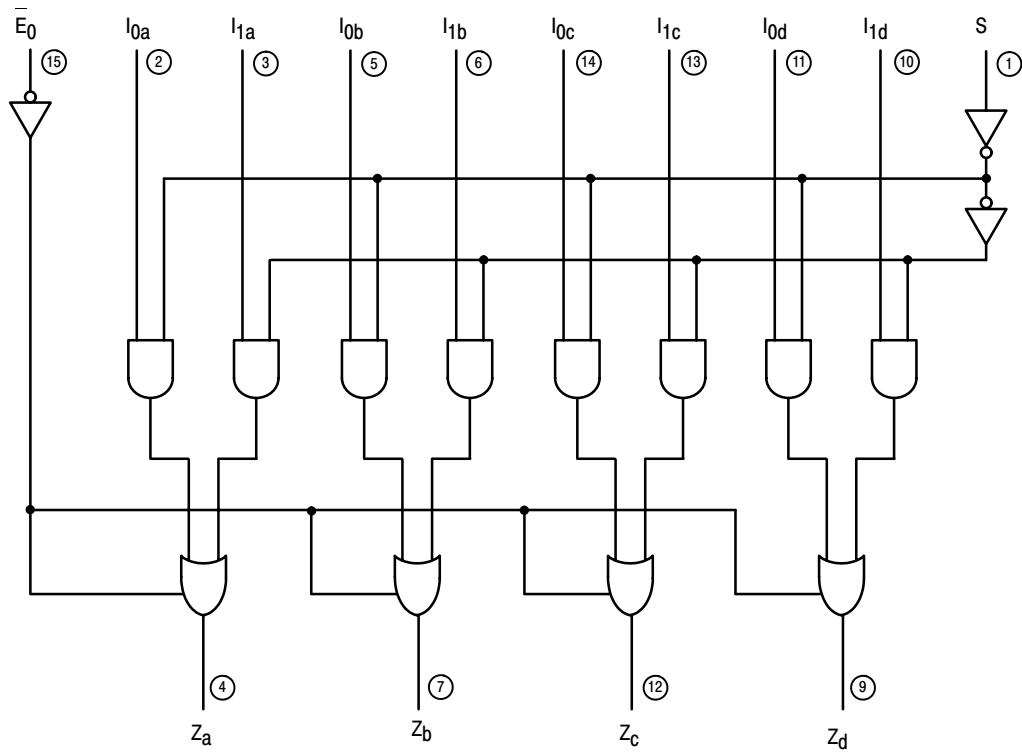


NOTE:  
The Flatpak version has the same  
pinouts (Connection Diagram) as  
the Dual In-Line Package.

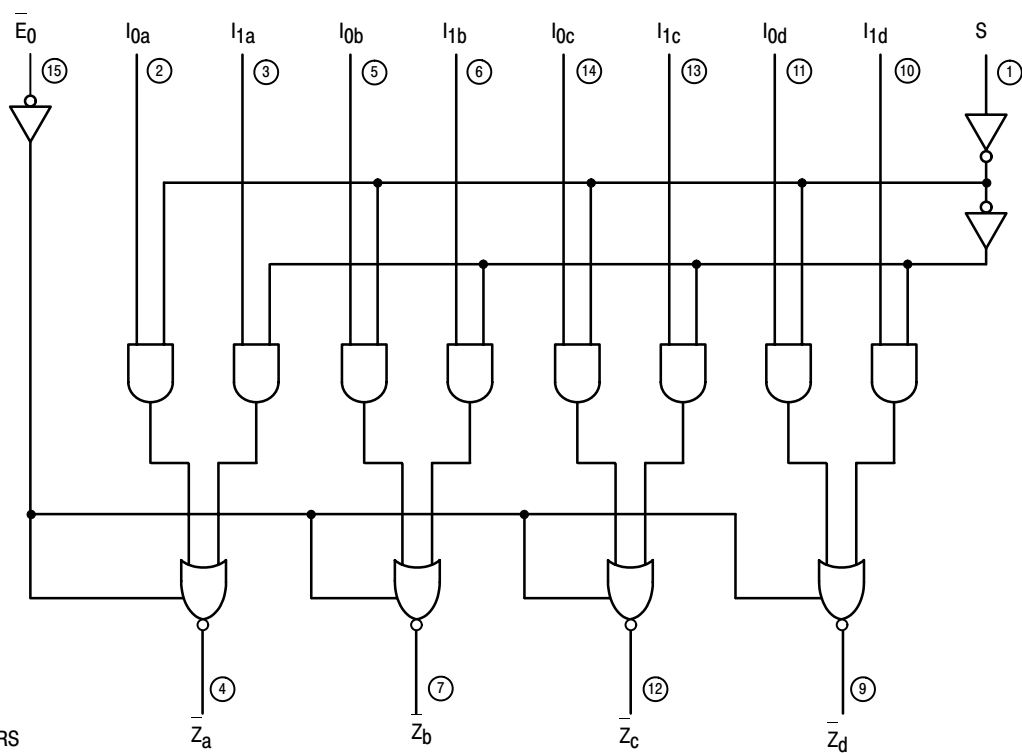
# SN74LS257B, SN74LS258B

## LOGIC DIAGRAMS

SN74LS257B



SN74LS258B



$V_{CC}$  = PIN 16  
GND = PIN 8

○ = PIN NUMBERS

## SN74LS257B, SN74LS258B

### FUNCTIONAL DESCRIPTION

The LS257B and LS258B are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the  $I_0$  inputs are selected and when Select is HIGH, the  $I_1$  inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257B and in the inverted form for the LS258B.

The LS257B and LS258B are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

#### LS257B

$$\begin{aligned} Z_a &= \bar{E}_0 \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ Z_b &= \bar{E}_0 \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ Z_c &= E_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ Z_d &= E_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

When the Output Enable Input ( $\bar{E}_0$ ) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

#### LS258B

$$\begin{aligned} Z_a &= \bar{E}_0 \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ Z_b &= \bar{E}_0 \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ Z_c &= E_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ Z_d &= E_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

TRUTH TABLE

| OUTPUT<br>ENABLE | SELECT<br>INPUT | DATA<br>INPUTS |       | OUTPUTS<br>LS257B | OUTPUTS<br>LS258B |
|------------------|-----------------|----------------|-------|-------------------|-------------------|
| $\bar{E}_0$      | S               | $I_0$          | $I_1$ | Z                 | $\bar{Z}$         |
| H                | X               | X              | X     | (Z)               | (Z)               |
| L                | H               | X              | L     | L                 | H                 |
| L                | H               | X              | H     | H                 | L                 |
| L                | L               | L              | X     | L                 | H                 |
| L                | L               | H              | X     | H                 | L                 |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

(Z) = High Impedance (off)

# SN74LS257B, SN74LS258B

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol    | Parameter                                      | Limits           |       |            | Unit          | Test Conditions                                                                               |
|-----------|------------------------------------------------|------------------|-------|------------|---------------|-----------------------------------------------------------------------------------------------|
|           |                                                | Min              | Typ   | Max        |               |                                                                                               |
| $V_{IH}$  | Input HIGH Voltage                             | 2.0              |       |            | V             | Guaranteed Input HIGH Voltage for All Inputs                                                  |
| $V_{IL}$  | Input LOW Voltage                              |                  |       | 0.8        | V             | Guaranteed Input LOW Voltage for All Inputs                                                   |
| $V_{IK}$  | Input Clamp Diode Voltage                      |                  | -0.65 | -1.5       | V             | $V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$                                             |
| $V_{OH}$  | Output HIGH Voltage                            | 2.4              | 3.1   |            | V             | $V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table |
| $V_{OL}$  | Output LOW Voltage                             |                  | 0.25  | 0.4        | V             | $I_{OL} = 12 \text{ mA}$                                                                      |
|           |                                                |                  | 0.35  | 0.5        | V             | $I_{OL} = 24 \text{ mA}$                                                                      |
| $I_{OZH}$ | Output Off Current — HIGH                      |                  |       | 20         | $\mu\text{A}$ | $V_{CC} = \text{MAX}$ , $V_{OUT} = 2.7 \text{ V}$                                             |
| $I_{OZL}$ | Output Off Current — LOW                       |                  |       | -20        | $\mu\text{A}$ | $V_{CC} = \text{MAX}$ , $V_{OUT} = 0.4 \text{ V}$                                             |
| $I_{IH}$  | Input HIGH Current<br>Other Inputs<br>S Inputs |                  |       | 20<br>40   | $\mu\text{A}$ | $V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$                                              |
|           | Other Inputs<br>S Inputs                       |                  |       | 0.1<br>0.2 | mA            | $V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$                                              |
| $I_{IL}$  | Input LOW Current<br>All Inputs                |                  |       | -0.4       | mA            | $V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$                                              |
| $I_{OS}$  | Short Circuit Current (Note 2)                 | -30              |       | -130       | mA            | $V_{CC} = \text{MAX}$                                                                         |
| $I_{CC}$  | Power Supply Current<br>Total, Output HIGH     | LS257B<br>LS258B |       | 10<br>9.0  | mA            | $V_{CC} = \text{MAX}$                                                                         |
|           | Total, Output LOW                              | LS257B<br>LS258B |       | 16<br>14   | mA            |                                                                                               |
|           | Total, Output 3-State                          | LS257B<br>LS258B |       | 19<br>16   | mA            |                                                                                               |

2. Not more than one output should be shorted at a time, nor for more than 1 second.

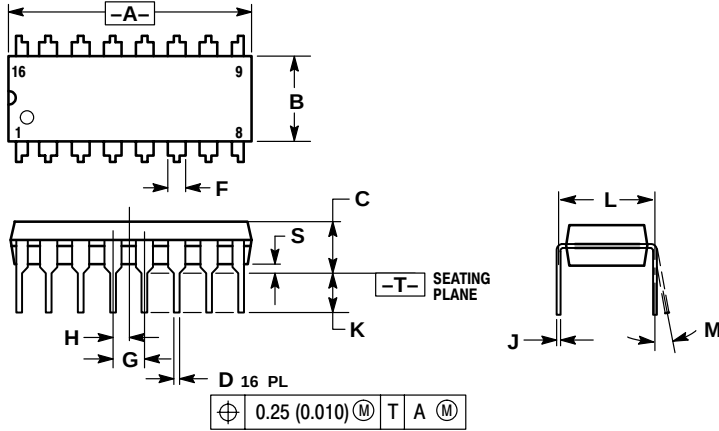
## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ ) See SN74LS251 for Waveforms

| Symbol                 | Parameter                           | Limits |          |          | Unit | Test Conditions |
|------------------------|-------------------------------------|--------|----------|----------|------|-----------------|
|                        |                                     | Min    | Typ      | Max      |      |                 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Data to Output   |        | 10<br>12 | 13<br>15 | ns   | Figures 1 & 2   |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Select to Output |        | 14<br>14 | 21<br>21 | ns   | Figures 1 & 2   |
| $t_{PZH}$              | Output Enable Time to HIGH Level    |        | 20       | 25       | ns   | Figures 4 & 5   |
| $t_{PZL}$              | Output Enable Time to LOW Level     |        | 20       | 25       | ns   | Figures 3 & 5   |
| $t_{PLZ}$              | Output Disable Time to LOW Level    |        | 16       | 25       | ns   | Figures 3 & 5   |
| $t_{PHZ}$              | Output Disable Time from HIGH Level |        | 18       | 25       | ns   | Figures 4 & 5   |

# SN74LS257B, SN74LS258B

## PACKAGE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**



### NOTES:

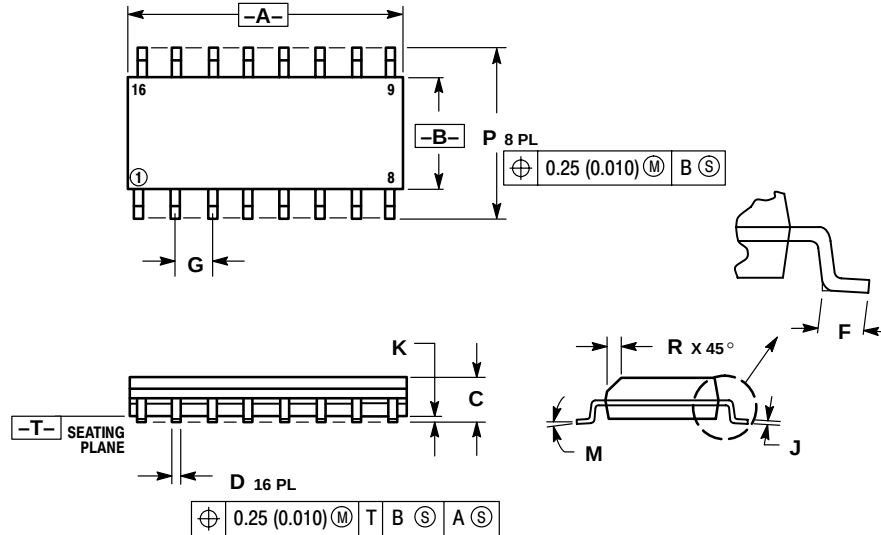
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

# SN74LS257B, SN74LS258B

## PACKAGE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



#### NOTES:

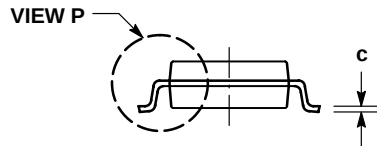
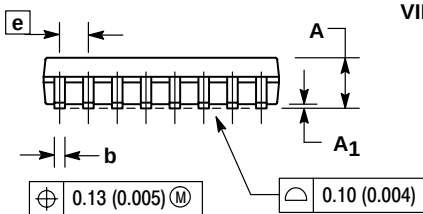
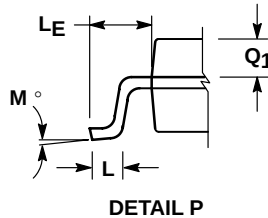
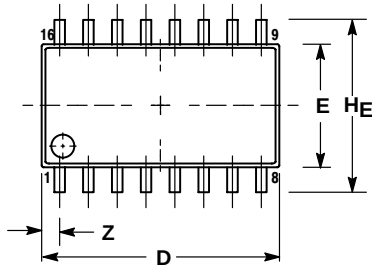
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| E   | 0.40        | 1.25  | 0.016     | 0.049 |
| F   | 1.27 BSC    |       | 0.050 BSC |       |
| G   | 0.19        | 0.25  | 0.008     | 0.009 |
| H   | 0.10        | 0.25  | 0.004     | 0.009 |
| J   | 0°          | 7°    | 0°        | 7°    |
| K   | 5.80        | 6.20  | 0.229     | 0.244 |
| M   | 0.25        | 0.50  | 0.010     | 0.019 |

# SN74LS257B, SN74LS258B

## PACKAGE DIMENSIONS

**M SUFFIX**  
SOEIAJ PACKAGE  
CASE 966-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.18        | 0.27  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| HE             | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| LE             | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.78  | ---       | 0.031 |

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