

MC74LVXT8053

Analog Multiplexer / Demultiplexer High-Performance Silicon-Gate CMOS

The MC74LVXT8053 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to GND).

The LVXT8053 is similar in pinout to the high-speed HC4053A, and the metal-gate MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected by means of an analog switch to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with TTL-type input thresholds. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the higher-voltage power supply.

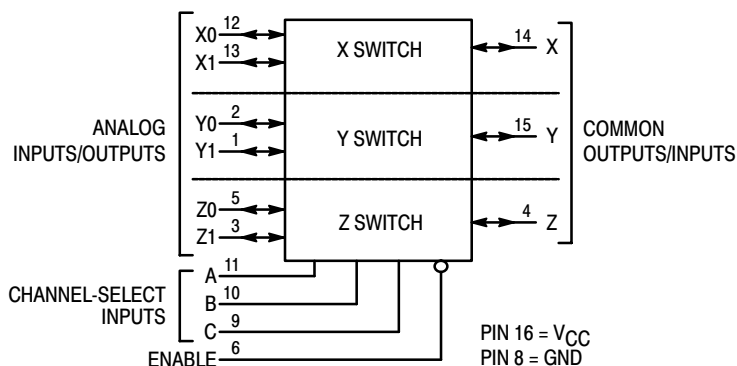
The MC74LVXT8053 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74LVXT8053 to be used to interface 5 V circuits to 3 V circuits.

This device has been designed so that the ON resistance (R_{ON}) is more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} - GND$) = 2.0 V to 6.0 V
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.0 V to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A

LOGIC DIAGRAM

Triple Single-Pole, Double-Position Plus Common Off

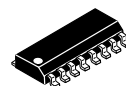


NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

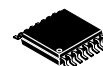


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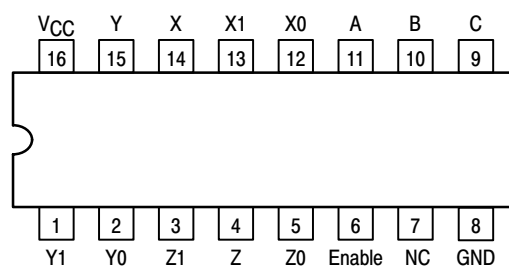


16-LEAD SOIC
D SUFFIX
CASE 751B



16-LEAD TSSOP
DT SUFFIX
CASE 948F

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 192 of this data sheet.

FUNCTION TABLE - MC74LVXT8053

Control Inputs						
Enable	Select					
	C	B	A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping
MC74LVXT8053DR2	SOIC	2500 Units/Reel
MC74LVXT8053DT	TSSOP	96 Units/Rail
MC74LVXT8053DTR2	TSSOP	2500 Units/Reel

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage (Referenced to GND)	−0.5 to + 7.0	V
V _{IS}	Analog Input Voltage	−0.5 to V _{CC} + 0.5	V
V _{in}	Digital Input Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	−20	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature Range	−65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating − SOIC Package: − 7 mW/°C from 65°C to 125°C

TSSOP Package: − 6.1 mW/°C from 65°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IS}	Analog Input Voltage	0.0	V _{CC}	V
V _{in}	Digital Input Voltage (Referenced to GND)	GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch		1.2	V
T _A	Operating Temperature Range, All Package Types	−55	+ 85	°C
t _r , t _f	Input Rise/Fall Time (Channel Select or Enable Inputs) V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R _{on} = Per Spec	3.0 4.5 5.5	1.2 2.0 2.0	1.2 2.0 2.0	1.2 2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R _{on} = Per Spec	3.0 4.5 5.5	0.53 0.8 0.8	0.53 0.8 0.8	0.53 0.8 0.8	V
I _{in}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V _{in} = V _{CC} or GND,	5.5	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V _{IS} = V _{CC} or GND; V _{IO} = 0 V	5.5	4	40	160	μA

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DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
R _{ON}	Maximum "ON" Resistance	V _{in} = V _{IL} or V _{IH}	3.0	40	45	50	Ω
		V _{IS} = V _{CC} to GND	4.5	30	32	37	
		I _S ≤ 10.0 mA (Figures 1, 2)	5.5	25	28	30	
		V _{in} = V _{IL} or V _{IH}	3.0	30	35	40	
ΔR _{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V _{IS} = V _{CC} or GND (Endpoints)	4.5	25	28	35	Ω
		I _S ≤ 10.0 mA (Figures 1, 2)	5.5	20	25	30	
		V _{in} = V _{IL} or V _{IH}	3.0	15	20	25	
		V _{IS} = 1/2 (V _{CC} - GND)	4.5	8.0	12	15	
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	I _S ≤ 10.0 mA	5.5	8.0	12	15	μA
		V _{in} = V _{IL} or V _{IH} ;	5.5	0.1	0.5	1.0	
		V _{IO} = V _{CC} or GND;	5.5	0.1	1.0	2.0	
		Switch Off (Figure 3)	5.5	0.1	1.0	2.0	
I _{on}	Maximum On-Channel Leakage Current, Channel-to-Channel	V _{in} = V _{IL} or V _{IH} ;	5.5	0.1	1.0	2.0	μA
		V _{IO} = V _{CC} or GND;	5.5	0.1	1.0	2.0	
		Switch-to-Switch =	5.5	0.1	1.0	2.0	
		V _{CC} or GND; (Figure 5)	5.5	0.1	1.0	2.0	

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 3 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0	30	35	40	ns
		3.0	20	25	30	
		4.5	15	18	22	
		5.5	15	18	20	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	4.0	6.0	8.0	ns
		3.0	3.0	5.0	6.0	
		4.5	1.0	2.0	2.0	
		5.5	1.0	2.0	2.0	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	30	35	40	ns
		3.0	20	25	30	
		4.5	15	18	22	
		5.5	15	18	20	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	20	25	30	ns
		3.0	12	14	15	
		4.5	8.0	10	12	
		5.5	8.0	10	12	
C _{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
C _{I/O}	Maximum Capacitance Analog I/O		35	35	35	pF
	(All Switches Off) Common O/I		50	50	50	
	Feedthrough		1.0	1.0	1.0	
C _{PD}	Power Dissipation Capacitance (Figure 13)*	Typical @ 25°C, V _{CC} = 5.0 V				pF
		45				

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

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ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V _{CC} V	Limit*	Unit
				25°C	
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	f _{IN} = 1MHz Sine Wave; Adjust f _{IN} Voltage to Obtain 0dBm at V _{OS} ; Increase f _{IN} Frequency Until dB Meter Reads -3 dB; R _L = 50 Ω, C _L = 10 pF	3.0 4.5 5.5	120 120 120	MHz
-	Off-Channel Feedthrough Isolation (Figure 7)	f _{IN} = Sine Wave; Adjust f _{IN} Voltage to Obtain 0 dBm at V _{IS} f _{IN} = 10kHz, R _L = 600 Ω, C _L = 50 pF	3.0 4.5 5.5	-50 -50 -50	dB
		f _{IN} = 1.0MHz, R _L = 50Ω, C _L = 10pF	3.0 4.5 5.5	-37 -37 -37	
-	Feedthrough Noise. Channel-Select Input to Common I/O (Figure 8)	V _{IN} ≤ 1MHz Square Wave (t _r = t _f = 3 ns); Adjust R _L at Setup so that I _S = 0A; Enable = GND R _L = 600 Ω, C _L = 50pF	3.0 4.5 5.5	25 105 135	mV PP
		R _L = 10 kΩ, C _L = 10pF	3.0 4.5 5.5	35 145 190	
-	Crosstalk Between Any Two Switches (Figure 12)	f _{IN} = Sine Wave; Adjust f _{IN} Voltage to Obtain 0dBm at V _{IS} f _{IN} = 10 kHz, R _L = 600Ω, C _L = 50pF	3.0 4.5 5.5	-50 -50 -50	dB
		f _{IN} = 1.0MHz, R _L = 50Ω, C _L = 10pF	3.0 4.5 5.5	-60 -60 -60	
THD	Total Harmonic Distortion (Figure 14)	f _{IN} = 1kHz, R _L = 10 kΩ, C _L = 50pF THD = THD _{measured} - THD _{source} V _{IS} = 2.0V _{PP} sine wave V _{IS} = 4.0V _{PP} sine wave V _{IS} = 5.0V _{PP} sine wave	3.0 4.5 5.5	0.10 0.08 0.05	%

*Limits not tested. Determined by design and verified by qualification.

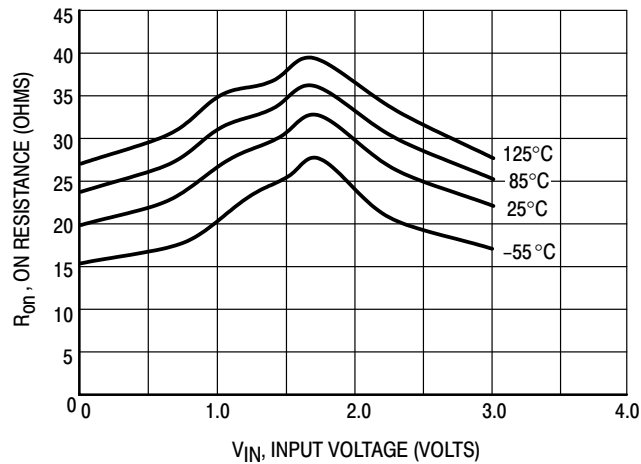


Figure 1a. Typical On Resistance, V_{CC} = 3.0 V

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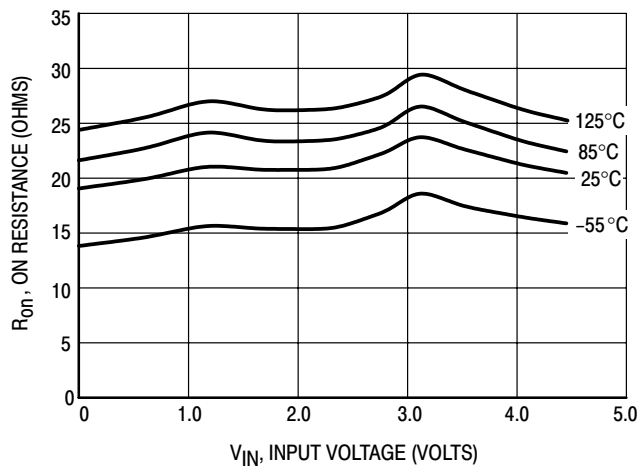


Figure 1b. Typical On Resistance, $V_{CC} = 4.5\text{ V}$

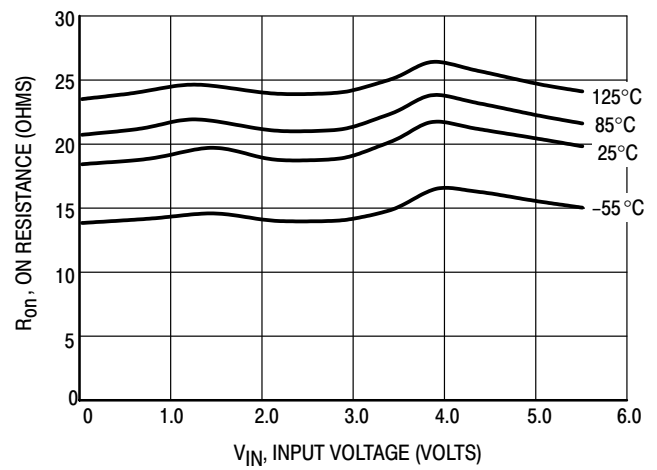


Figure 1c. Typical On Resistance, $V_{CC} = 5.5\text{ V}$

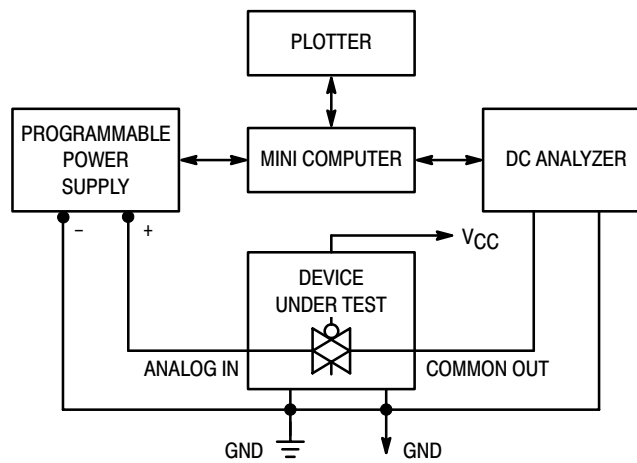


Figure 1. On Resistance Test Set-Up

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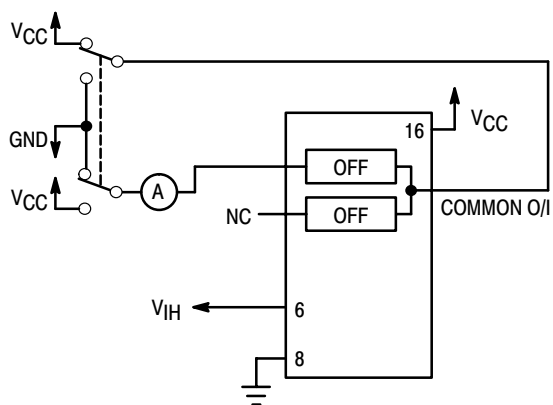


Figure 2. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

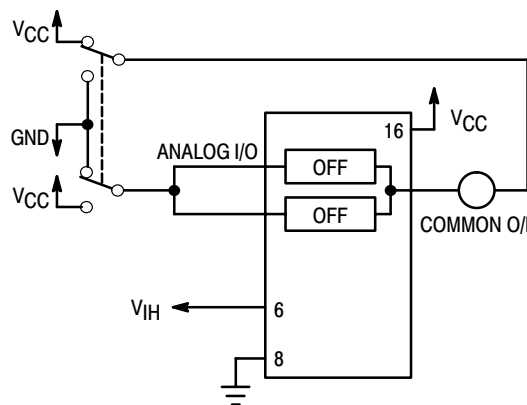


Figure 3. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

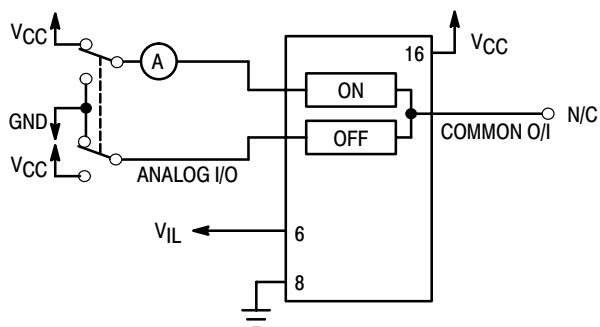
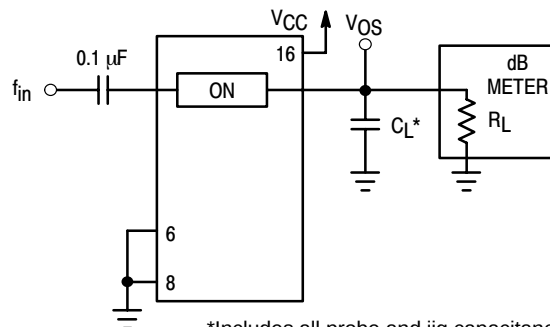
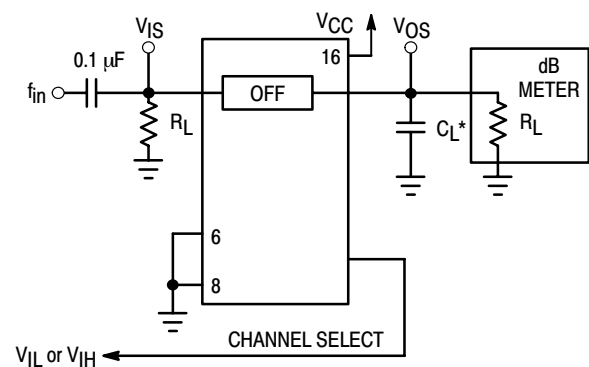


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



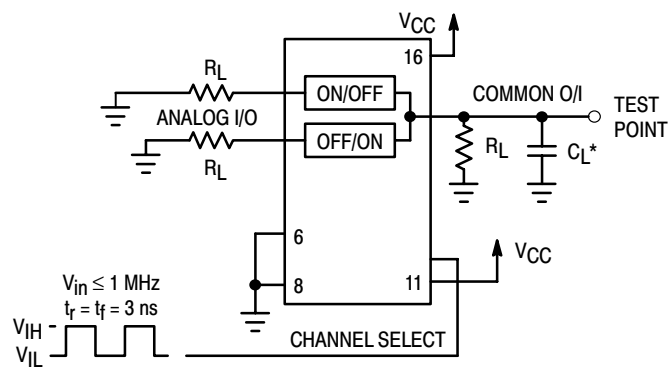
*Includes all probe and jig capacitance

Figure 5. Maximum On Channel Bandwidth, Test Set-Up



*Includes all probe and jig capacitance

Figure 6. Off Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance

Figure 7. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

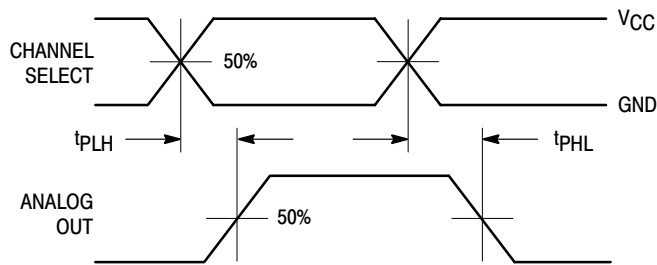
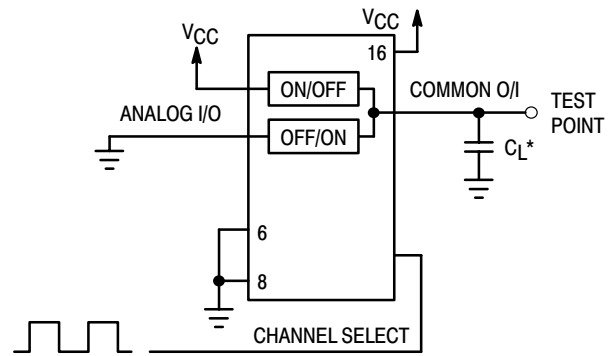


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

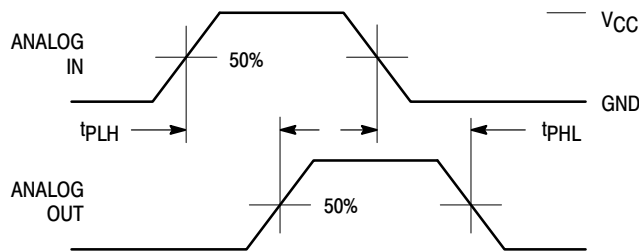
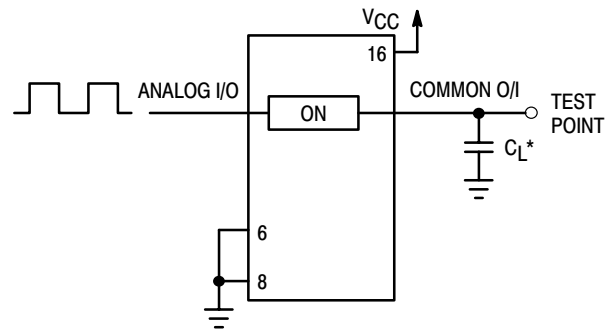


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

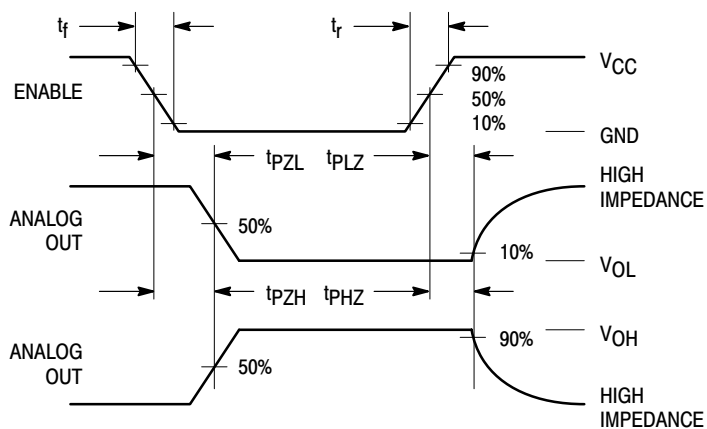


Figure 11a. Propagation Delays, Enable to Analog Out

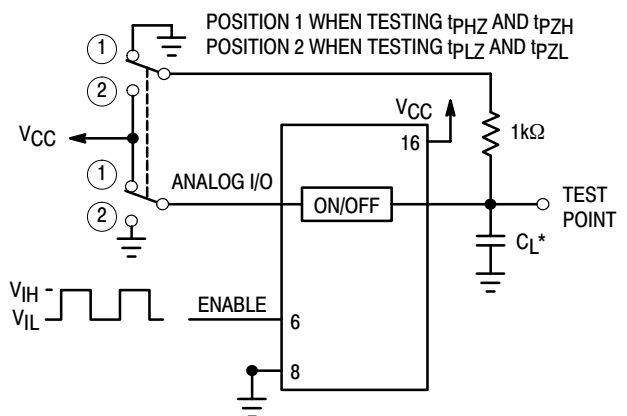
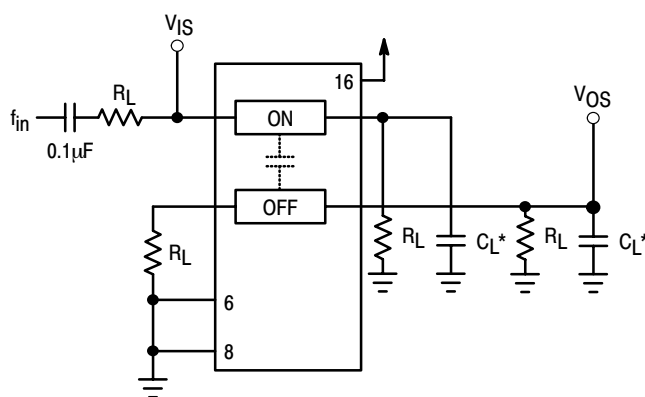


Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out



*Includes all probe and jig capacitance

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

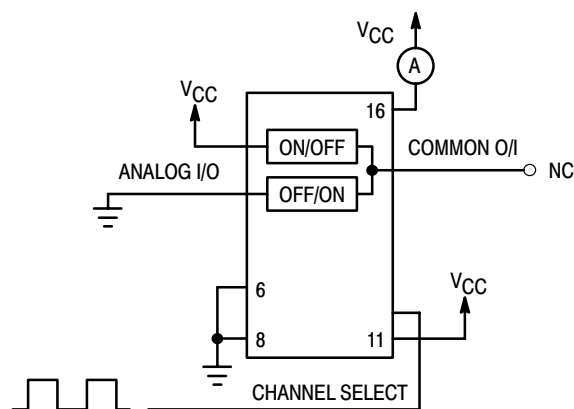
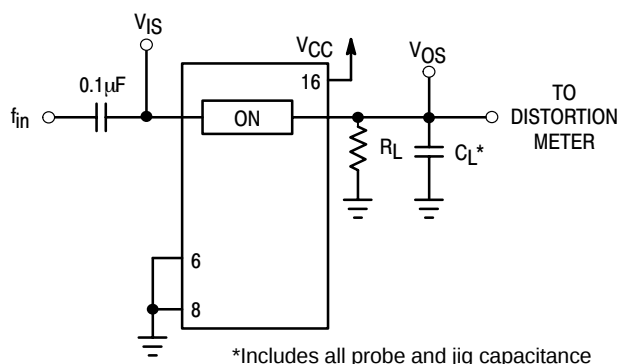


Figure 13. Power Dissipation Capacitance, Test Set-Up



*Includes all probe and jig capacitance

Figure 14a. Total Harmonic Distortion, Test Set-Up

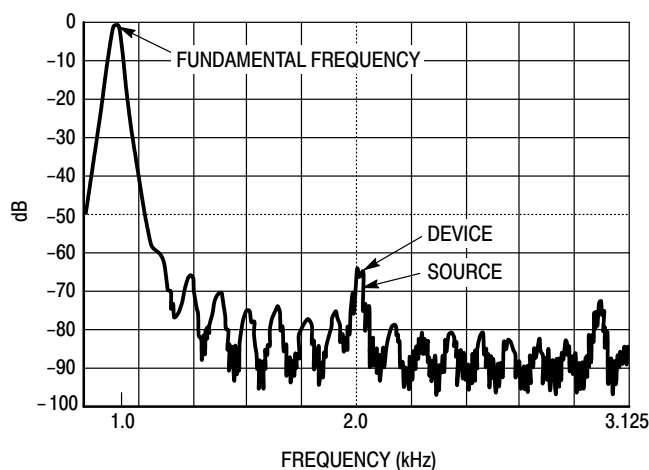


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5V = \text{logic high} \\ GND &= 0V = \text{logic low} \end{aligned}$$

The maximum analog voltage swing is determined by the supply voltages V_{CC} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below GND. In this example, the difference between V_{CC} and GND is five volts. Therefore, using the configuration of Figure 15, a maximum analog signal of five volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not

connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{CC} - GND = 2 \text{ to } 6 \text{ volts}$$

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

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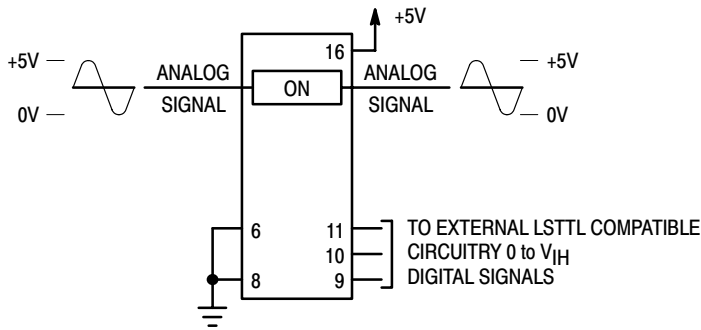


Figure 15. Application Example

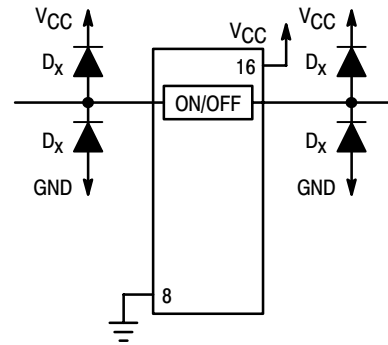
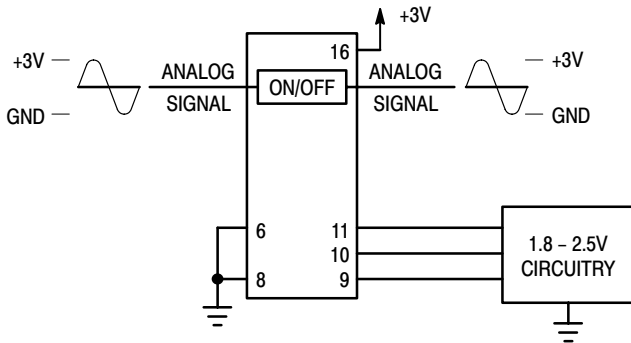
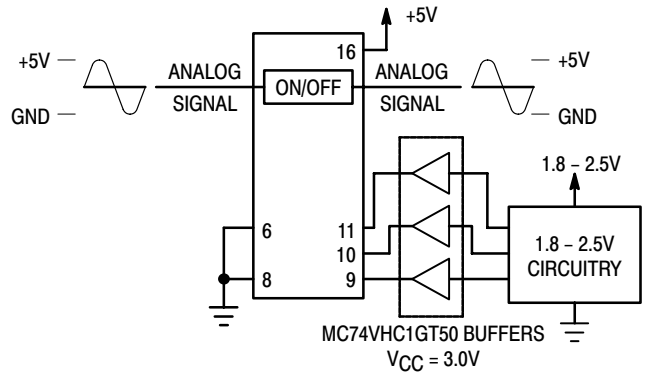


Figure 16. External Germanium or Schottky Clipping Diodes



a. Low Voltage Logic Level Shifting Control



b. 2-Stage Logic Level Shifting Control

Figure 17. Interfacing Low Voltage CMOS Inputs

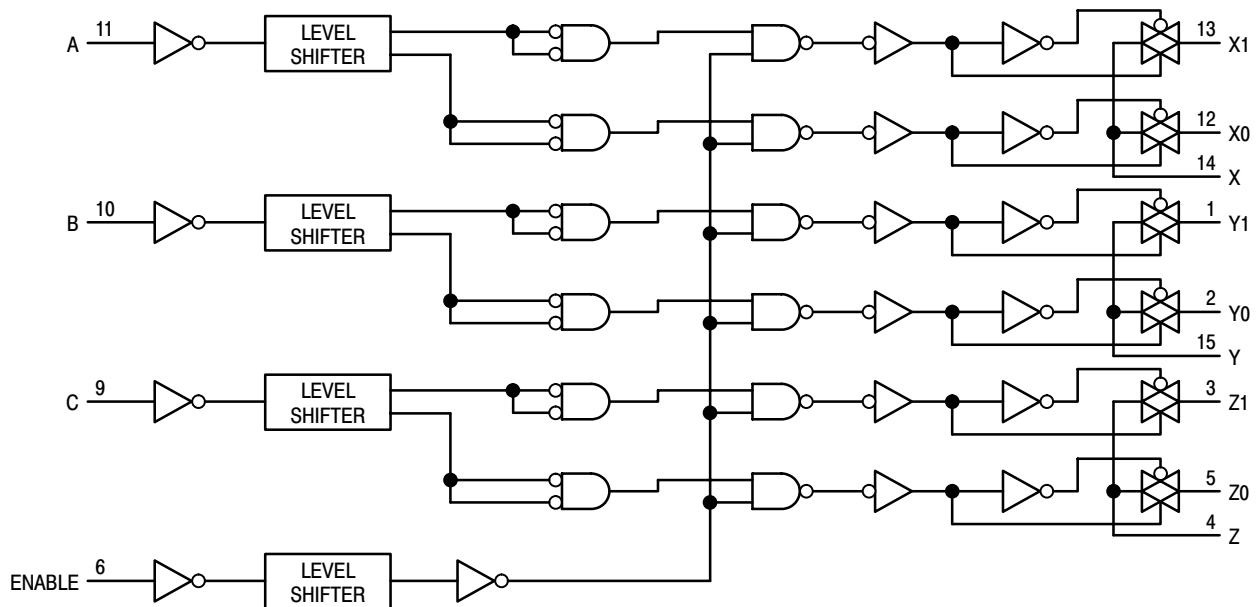
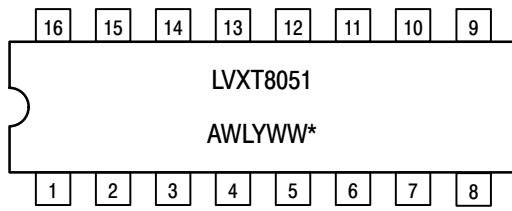


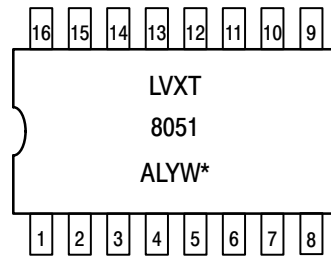
Figure 18. Function Diagram, LVXT8053

MC74LVXT8053

MARKING DIAGRAMS (Top View)



16-LEAD SOIC
D SUFFIX
CASE 751B



16-LEAD TSSOP
DT SUFFIX
CASE 948F

*See Applications Note #AND8004/D for date code and traceability information.