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NTE4008B

Integrated Circuit

CMOS, 4-Bit Full Adder w/Parallel Carry Out

Description:

The NTE4008B is a 4-bit full adder in a 16-Lead DIP type package constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

Features:

- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS} , Note 1)

DC Supply Voltage, V_{DD}		-0.5 to +18.0V
Input Voltage (DC or Transient), V_{in}		-0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out}		-0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in}		$\pm 10\text{mA}$
Output Current (DC or Transient, Per Pin), I_{out}		$\pm 10\text{mA}$
Power Dissipation (Per Package), P_D		500mW
Temperature Derating (from +65° to +125°C)		-7.0mW/°C
Storage Temperature Range, T_{stg}		-65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L		+260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS} , Note 2)

Parameter	Symbol	V_{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0 "1" Level $V_{in} = 0$ or V_{DD}	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level ($V_O = 4.5$ or $0.5V_{dc}$) ($V_O = 9.0$ or $1.0V_{dc}$) ($V_O = 13.5$ or $1.5V_{dc}$) "1" Level ($V_O = 0.5$ or $4.5V_{dc}$) ($V_O = 1.0$ or $9.0V_{dc}$) ($V_O = 1.5$ or $13.5V_{dc}$)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source ($V_{OH} = 2.5V_{dc}$) ($V_{OH} = 4.6V_{dc}$) ($V_{OH} = 9.5V_{dc}$) ($V_{OH} = 13.5V_{dc}$) Sink ($V_{OL} = 0.4V_{dc}$) ($V_{OL} = 0.5V_{dc}$) ($V_{OL} = 1.5V_{dc}$)	I_{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	± 0.1	–	± 0.00001	± 0.1	–	± 0.1	μ Adc
Input Capacitance ($V_{IN} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μ Adc
		10	–	10	–	0.010	10	–	300	μ Adc
		15	–	20	–	0.015	20	–	600	μ Adc
Total Supply Current (Dynamic plus Quiescent, Per Package, $C_L = 50pF$ on all outputs, all buffers switching, Note 3, Note 4)	I_T	5.0	$I_T = (1.7\mu A/kHz) f + I_{DD}$							μ Adc
		10	$I_T = (3.4\mu A/kHz) f + I_{DD}$							μ Adc
		15	$I_T = (5.0\mu A/kHz) f + I_{DD}$							μ Adc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.005$.

Switching Characteristics: ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5\text{ns/pf}) C_L + 25\text{ns}$ $T_{TLH}, t_{THL} = (0.75\text{ns/pf}) C_L + 12.5\text{ns}$ $T_{TLH}, t_{THL} = (0.55\text{ns/pf}) C_L + 9.5\text{ns}$	$t_{TLH},$ t_{THL}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Propagation Delay Time Sum In to Sum Out $t_{PLH}, t_{PHL} = (1.7\text{ns/pf}) C_L + 315\text{ns}$ $t_{PLH}, t_{PHL} = (0.66\text{ns/pf}) C_L + 127\text{ns}$ $t_{PLH}, t_{PHL} = (0.5\text{ns/pf}) C_L + 90\text{ns}$ Sum In to Carry Out $t_{PLH}, t_{PHL} = (1.7\text{ns/pf}) C_L + 220\text{ns}$ $t_{PLH}, t_{PHL} = (0.66\text{ns/pf}) C_L + 112\text{ns}$ $t_{PLH}, t_{PHL} = (0.5\text{ns/pf}) C_L + 85\text{ns}$ Carry In to Sum Out $t_{PLH}, t_{PHL} = (1.7\text{ns/pf}) C_L + 290\text{ns}$ $t_{PLH}, t_{PHL} = (0.66\text{ns/pf}) C_L + 122\text{ns}$ $t_{PLH}, t_{PHL} = (0.5\text{ns/pf}) C_L + 90\text{ns}$ Carry In to Carry Out $t_{PLH}, t_{PHL} = (1.7\text{ns/pf}) C_L + 85\text{ns}$ $t_{PLH}, t_{PHL} = (0.66\text{ns/pf}) C_L + 42\text{ns}$ $t_{PLH}, t_{PHL} = (0.5\text{ns/pf}) C_L + 30\text{ns}$	$t_{PLH},$ t_{PHL}	5.0	–	400	800	ns
		10	–	160	320	ns
		15	–	115	230	ns
		5.0	–	305	610	ns
		10	–	145	290	ns
		15	–	110	220	ns
		5.0	–	375	750	ns
		10	–	155	310	ns
		15	–	115	230	ns
		5.0	–	170	340	ns
		10	–	75	150	ns
		15	–	55	110	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at $+25^\circ\text{C}$.

Truth Table (Single Stage):

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Pin Connection Diagram

