FAIRCHILD SEMICONDUCTOR®

April 2008

NC7SBU3157, FSAU3157
Low-Voltage SPDT Analog Switch or 2:1 Multiplexer / De-multiplexer Bus Switch

Features

- Analog and digital applications
- Space-saving, SC70 6-lead, surface-mount package
- Low on resistance: <10Ω on typical at 3.3V V_{CC}
- Broad V_{CC} operating range: 1.65V to 5.5V
- Rail-to-rail signal handling
- Power-down, high-impedance control input
- Over-voltage tolerance of control input to 7.0V
- Break-before-make enable circuitry
- 250 MHz, 3dB bandwidth

General Description

The NC7SBU3157 / FSAU3157 is a high-performance, single-pole / double-throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-before-make select circuitry prevents disruption of signals on the B port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V V_{CC} operating range. The control input tolerates voltages up to 5.5V, independent of the V_{CC} operating range.

Fairchild's integrated Undershoot Hardened Circuit (UHC®) senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning the switch on.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package Description	Packing Method
NC7SBU3157P6X	B7A	-40 to +85°C	6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package	3000 Units Tape and Reel
FSAU3157P6X	B7A	-40 to +85°C	6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package	3000 Units Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

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UHC® is a registered trademark of Fairchild Semiconductor Corporation.

Logic Symbol

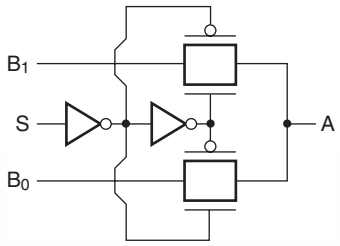


Figure 1. Logic Symbol

Analog Symbol

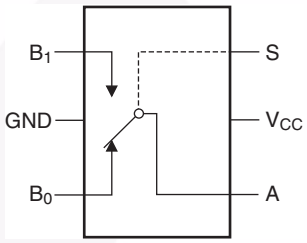


Figure 3. Analog Symbol

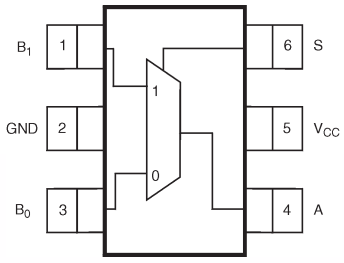
Function Table

Input (S)	Function
Logic Level Low	B_0 Connected to A
Logic Level High	B_1 Connected to A

Pin Descriptions

Pin Names	Description
A, B_0, B_1	Data Ports
S	Control Input

Connection Diagrams



2. Pin Assignments SC70

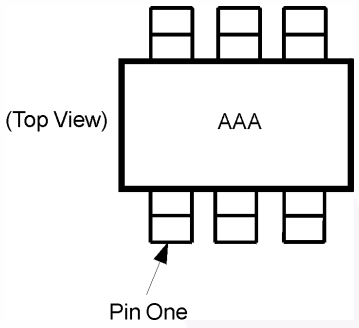


Figure 4. Pin One Orientation

Note:

Orientation of top mark determines pin one location. Read the top mark left to right and pin one is the lower left pin *(see Figure 4)*.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	–0.5	+7.0	V
V_S	DC Switch Voltage(1)	–0.5	V_{CC} +0.5	V
V_{IN}	DC Input Voltage(1)	–0.5	+7.0	V
I_{IK}	DC Input Diode Current at V_{IN} < 0V		–50	mA
I_{OUT}	DC Output Current		128	mA
I_{CC}/I_{GND}	DC V_{CC} or Ground Current		±100	mA
T_{STG}	Storage Temperature Range	–65	+150	°C
T_J	Junction Temperature Under Bias		+150	°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)		+260	°C
P_D	Power Dissipation at +85°C		180	mW

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Max	Units
V_{CC}	Supply Voltage Operating		1.65	5.50	V
V_{IN}	Control Input Voltage(2)		0	V_{CC}	V
V_{IN}	Switch Input Voltage(2)		0	V_{CC}	V
V_{OUT}	Output Voltage(2)		0	V_{CC}	V
T_A	Operating Temperature		–40	+85	°C
t_r, t_f	Input Rise and Fall Time	Control Input V_{CC}=2.3V–3.6V	0	10	ns/V
		Control Input V_{CC}=4.5V–5.5V	0	5	ns/V
θ_{JA}	Thermal Resistance			350	°C/W

Note:

2. Control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage		1.65 to 1.95	0.75 V_{CC}			0.75 V_{CC}		V
			2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}		
V_{IL}	Low Level Input Voltage		1.65 to 1.95			0.25 V_{CC}		0.25 V_{CC}	V
			2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}	
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5V$	0 to 5.5		±0.05	±0.1		±1	µA
I_{OFF}	Off State Leakage Current	$0 \le A, B \le V_{CC}$	1.65 to 5.5		±0.05	±0.1		±1	µA
R_{ON}	Switch On Resistance(3)	V_{IN}=0V, I_O=30mA	4.5		3.0	15.0		15.0	Ω
		V_{IN}=2.4V, I_O=–30mA			5.0	15.0		15.0	
		V_{IN}=4.5V, I_O=–30mA			7.0	15.0		15.0	
		V_{IN}=0V, I_O=24mA	3.0		4.0	20.0		20.0	
		V_{IN}=3V, I_O=–24mA			10.0	20.0		20.0	
		V_{IN}=0V, I_O=8mA	2.3		5.0	30.0		30.0	
		V_{IN}=2.3V, I_O=–8mA			13.0	30.0		30.0	
		V_{IN}=0V, I_O=4mA	1.65		6.5	50.0		50.0	
		V_{IN}=1.65V, I_O=–4mA			17.0	50.0		50.0	
I_{CC}	Quiescent Supply Current; All Channels On or Off	V_{IN}=V_{CC} or GND I_{OUT}=0	5.5			1		10	µA
	Analog Signal Range		V_{CC}	0		V_{CC}	0	V_{CC}	V
R_{RANGE}	On Resistance Over Signal Range (3, 7)	I_A=–30mA, $0 \le V_{Bn} \le V_{CC}$	4.5					25.0	Ω
		I_A=–24mA, $0 \le V_{Bn} \le V_{CC}$	3.0					50.0	
		I_A=–8mA, $0 \le V_{Bn} \le V_{CC}$	2.3					100	
		I_A=–4mA, $0 \le V_{Bn} \le V_{CC}$	1.65					300	
ΔR_{ON}	On Resistance Match Between-Channels(3, 4, 5)	I_A=–30mA, V_{Bn}=3.15	4.5		0.15				Ω
		I_A=–24mA, V_{Bn} 2.1	3.0		0.2				
		I_A=–8mA, V_{Bn}=1.6	2.3		0.5				
		I_A=–4mA, V_{Bn}=1.15	1.65		0.5				
V_{IKU}	Voltage Under-shoot	$0.0mA \le I_{IN} \le$–50, $\overline{OE}$ 5.5v	5.5					–2	V
R_{flat}	On Resistance Flatness(3, 4, 6)	I_A=–30mA, $0 \le V_{Bn} \le V_{CC}$	5.0		6.0				Ω
		I_A=–24mA, $0 \le V_{Bn} \le V_{CC}$	3.3		12.0				
		I_A=–8mA, $0 \le V_{Bn} \le V_{CC}$	2.5		28.0				
		I_A=–4mA, $0 \le V_{Bn} \le V_{CC}$	1.8		125				

Notes:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized, but not tested in production.
5. $\Delta R_{ON} = R_{ON}$ max – R_{ON} minimum measured at identical V_{CC}, temperature, and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
7. Guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A = –40°C to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PHL}, t_{PLH}	Propagation Delay Bus-to-Bus[8]	V_I = OPEN	1.65 to 1.95						ns	Figure 7 Figure 8
			2.3 to 2.7			1.2		1.2		
			3.0 to 3.6			0.8		0.8		
			4.5 to 5.5			0.3		0.3		
t_{PZL}, t_{PZH}	Output Enable Time Turn-On Time (A to B_n)	V_I = 2 x V_{CC} for t_{PZL} V_I = 0V for t_{PZH}	1.65 to 1.95	7.0		23.0	7.0	24.0	ns	Figure 7 Figure 8
			2.3 to 2.7	3.5		13.0	3.5	14.0		
			3.0 to 3.6	2.5		6.9	2.5	7.6		
			4.5 to 5.5	1.7		5.2	1.7	5.7		
t_{PLZ}, t_{PHZ}	Output Disable Time Turn-Off Time (A Port to B Port)	V_I = 2 x V_{CC} for t_{PLZ} V_I = 0V for t_{PHZ}	1.65 to 1.95	3.0		12.5	3.0	13.0	ns	Figure 7 Figure 8
			2.3 to 2.7	2.0		7.0	2.0	7.5		
			3.0 to 3.6	1.5		5.0	1.5	5.3		
			4.5 to 5.5	0.8		3.5	0.8	3.8		
t_{BBM}	Break-Before-Make Time[9]		1.65 to 1.95	0.5			0.5		ns	Figure 9
			2.3 to 2.7	0.5			0.5			
			3.0 to 3.6	0.5			0.5			
			4.5 to 5.5	0.5			0.5			
Q	Charge Injection[9]	C_L = 0.1nF, V_{GEN} = 0V,	5.0		7.0				pC	Figure 10
		R_{GEN} = 0Ω	3.3		3.0					
OIRR	Off Isolation[10]	R_L = 50Ω, f = 10MHz	1.65 to 5.5		–57.0				dB	Figure 11
Xtalk	Crosstalk	R_L = 50Ω, f = 10MHz	1.65 to 5.5		–54.0				dB	Figure 12
BW	–3dB Bandwidth	R_L = 50Ω	1.65 to 5.5		250				MHz	Figure 15
THD	Total Harmonic Distortion[9]	R_L = 600Ω, 0.5V_{PP}, f = 20Hz to 20KHz	5.0		.011				%	

Notes:

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).
9. Guaranteed by design.
10. Off Isolation = 20 $\log_{10}$ [V_A / V_{Bn}].

Capacitance

T_A = +25°C, f = 1MHz. Capacitance is characterized, but not tested in production.

Symbol	Parameter	Conditions	Typ.	Max.	Units	Figure
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0V	2.3		pF	
C_{IO-B}	B Port Off Capacitance	V_{CC} = 5.0V	6.5		pF	Figure 13
C_{IOA-ON}	A Port Capacitance When Switch Is Enabled	V_{CC} = 5.0V	18.5		pF	Figure 14

Undershoot Characteristic

Symbol	Parameter	Min.	Typ.	Units	Figure
V_{OUTU}	Output Voltage During Undershoot	2.5	V_{OH} - 0.3	V	Figure 5

Note:

11. This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

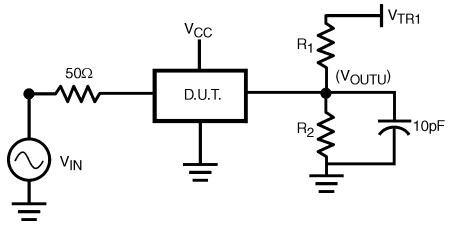


Figure 5. Output Voltage During Undershoot

Device Test Conditions

Parameter	Value	Units
V_{IN}	*see Figure 6*	V
$R_1 = R_2$	100	KΩ
V_{TRI}	7.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform

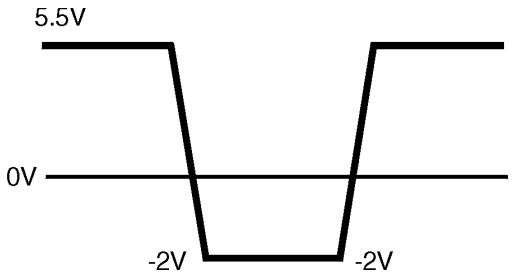
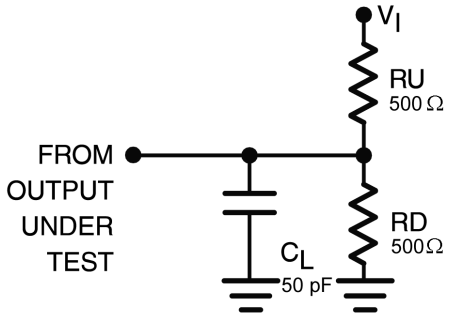


Figure 6. Transient Input Voltage Waveform

AC Loading and Waveforms



Notes:
Input driven by 50Ω source terminated in 50Ω.
C_L includes load and stray capacitance.
Input PRR=1.0MHz; tw = 500ns.

Figure 7. AC Test Circuit

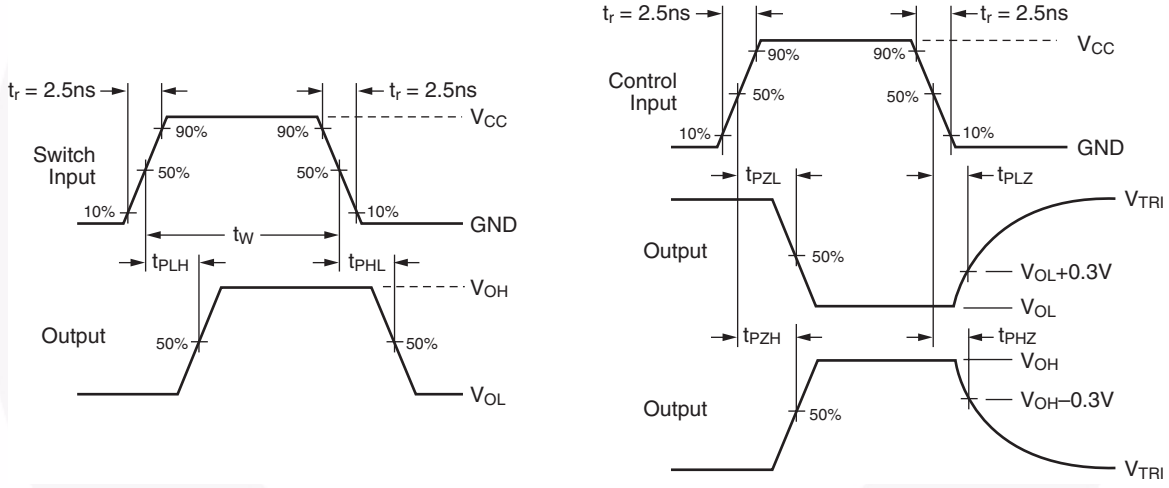


Figure 8. AC Waveforms

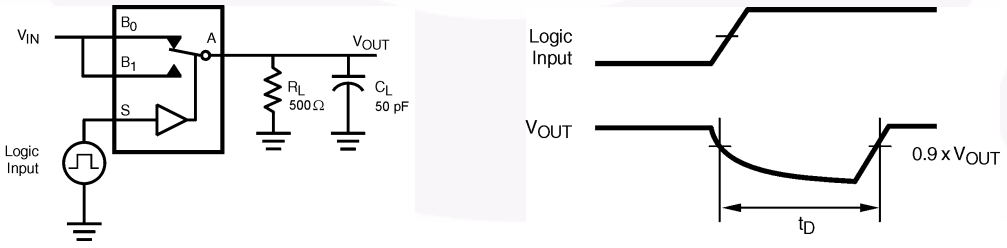
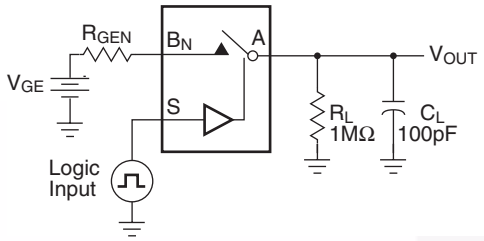


Figure 9. Break-Before-Make Interval Timing

AC Loading and Waveforms (continued)



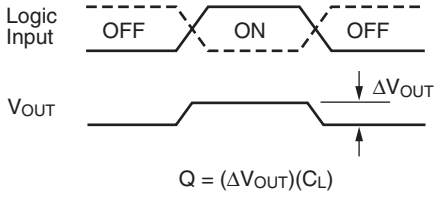


Figure 10. Charge Injection Test

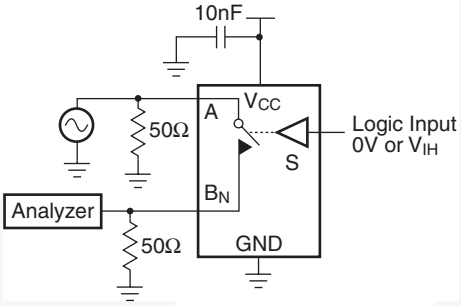


Figure 11. Off Isolation

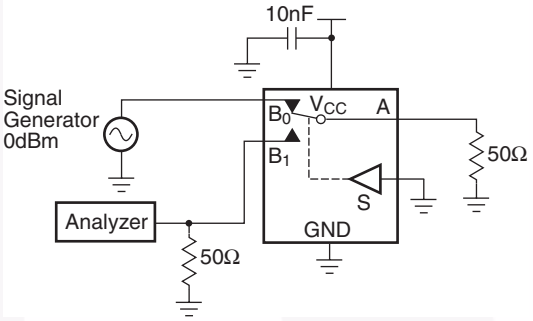


Figure 12. Crosstalk

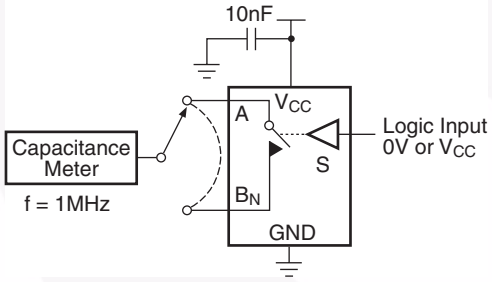


Figure 13. Channel Off Capacitance

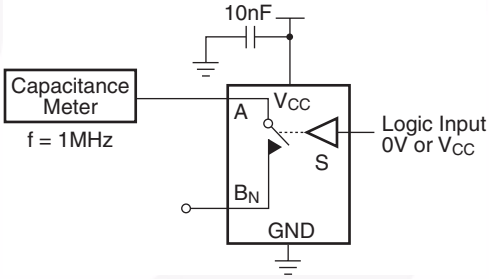


Figure 14. Channel On Capacitance

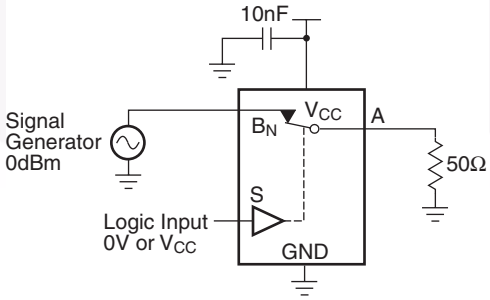


Figure 15. Bandwidth

Physical Dimensions

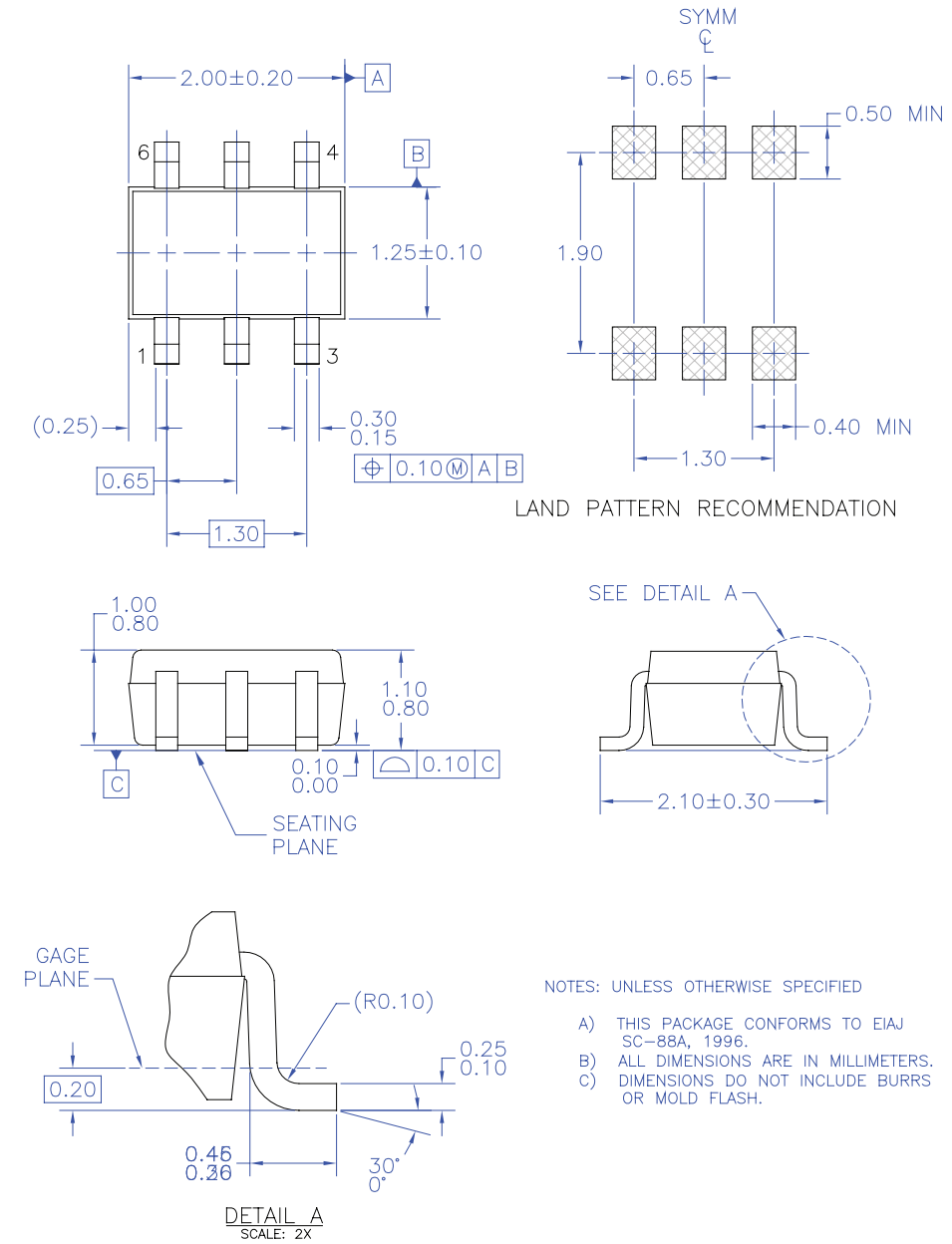


Figure 16. 6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package

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Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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