

# T-51-19

## CD4047A Types

### CMOS Low-Power Monostable/Astable Multivibrator

The RCA-CD4047A consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, -TRIGGER, ASTABLE, ASTABLE, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q,  $\bar{Q}$ , and OSCILLATOR. In all modes of operation an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and  $\bar{Q}$  Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the  $\bar{ASTABLE}$  input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the -TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the -TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the RETRIGGER input is high, with or without transitions.

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the ASTABLE input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever  $V_{DD}$  is applied.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

#### Features:

- Low power consumption: special COS/MOS oscillator configuration
- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required
- Quiescent current specified to 15 V
- Maximum input leakage current of 1  $\mu$ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

#### Monostable Multivibrator Features:

- Positive- or negative-edge trigger
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse width expansion
- Long pulse widths possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

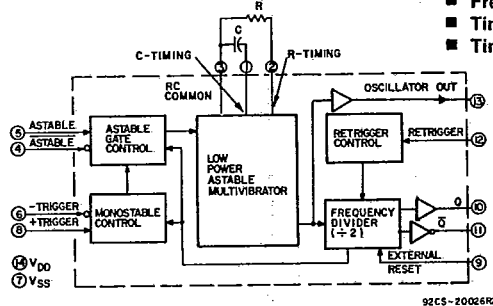
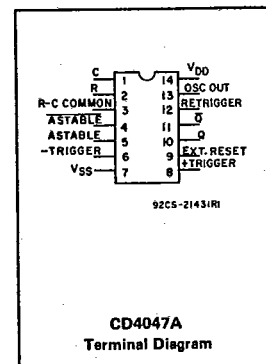


Fig. 1 - CD4047A logic block diagram.

#### MAXIMUM RATINGS, Absolute-Maximum Values:

|                                                                               |                                       |
|-------------------------------------------------------------------------------|---------------------------------------|
| STORAGE-TEMPERATURE RANGE ( $T_{stg}$ )                                       | -65 to +150°C                         |
| OPERATING-TEMPERATURE RANGE ( $T_A$ ):                                        |                                       |
| PACKAGE TYPES D, F, K, H                                                      | -55 to +125°C                         |
| PACKAGE TYPE E                                                                | -40 to +85°C                          |
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )                                         |                                       |
| (Voltages referenced to $V_{SS}$ Terminal):                                   | -0.5 to +15 V                         |
| POWER DISSIPATION PER PACKAGE ( $P_D$ )                                       |                                       |
| FOR $T_A = -40$ to +60°C (PACKAGE TYPE E)                                     | 500 mW                                |
| FOR $T_A = +60$ to +85°C (PACKAGE TYPE E)                                     | Derate Linearly at 12 mW/°C to 200 mW |
| FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)                             | 500 mW                                |
| FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)                            | Derate Linearly at 12 mW/°C to 200 mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                                      |                                       |
| FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)                | 100 mW                                |
| INPUT VOLTAGE RANGE, ALL INPUTS                                               | -0.5 to $V_{DD} + 0.5$ V              |
| LEAD TEMPERATURE (DURING SOLDERING):                                          |                                       |
| At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79 mm) from case for 10 s max. | +265°C                                |



#### Astable Multivibrator Features:

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available
- Good astable frequency stability:

#### Frequency deviation:

$$= \pm 2\% + 0.03\%/^{\circ}\text{C} @ 100 \text{ kHz}$$

$$= \pm 0.5\% + 0.015\%/^{\circ}\text{C} @ 10 \text{ kHz}$$

(circuits "trimmed" to frequency  $V_{DD} = 10 \text{ V} \pm 10\%$ )

#### Applications:

- Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:
- Envelope detection
  - Frequency multiplication
  - Frequency division
  - Frequency discriminators
  - Timing circuits
  - Time-delay applications

## CD4047A Types

RECOMMENDED OPERATING CONDITIONS at  $T_A = 25^\circ\text{C}$ , Except as Noted.  
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC                                                            | V <sub>DD</sub> | LIMITS              |         |             |         | UNITS |
|---------------------------------------------------------------------------|-----------------|---------------------|---------|-------------|---------|-------|
|                                                                           |                 | D, F, K, H Packages |         | E Package   |         |       |
|                                                                           |                 | Min.                | Max.    | Min.        | Max.    |       |
| Supply-Voltage Range (For T <sub>A</sub> =Full Package Temperature Range) |                 | 3                   | 12      | 3           | 12      | V     |
| Input Pulse Width, t <sub>W</sub><br>(Any Input)                          | 5<br>10         | 1000<br>400         | —<br>—  | 1300<br>600 | —<br>—  | ns    |
| Trigger, Retrigger<br>Rise or Fall Time, t <sub>r</sub> , t <sub>f</sub>  | 5<br>10         | —<br>—              | 15<br>5 | —<br>—      | 15<br>5 | μs    |

## STATIC ELECTRICAL CHARACTERISTICS

| Characteristics                                                             | Conditions            |                        |                        | Limits at Indicated Temperatures (°C) |                   |      |       |           |                   |       |       | Units |    |
|-----------------------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------------------|------|-------|-----------|-------------------|-------|-------|-------|----|
|                                                                             |                       |                        |                        | D, F, K, H Packages                   |                   |      |       | E Package |                   |       |       |       |    |
|                                                                             | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | -55                                   | +25<br>Typ. Limit |      | +125  | -40       | +25<br>Typ. Limit |       | +85   |       |    |
| Quiescent Device Current I <sub>L</sub> Max.                                | —                     | —                      | 5                      | 5                                     | 0.03              | 5    | 300   | 50        | 0.1               | 50    | 700   | μA    |    |
|                                                                             | —                     | —                      | 10                     | 10                                    | 0.05              | 10   | 600   | 100       | 0.2               | 100   | 1400  |       |    |
|                                                                             | —                     | —                      | 15                     | 50                                    | 1                 | 50   | 2000  | 500       | 5                 | 500   | 5000  |       |    |
| Output Voltage: Low-Level, V <sub>OL</sub>                                  | —                     | 5                      | 5                      | 0 Typ.; 0.05 Max.                     |                   |      |       |           |                   |       |       |       | V  |
|                                                                             | —                     | 10                     | 10                     | 0 Typ.; 0.05 Max.                     |                   |      |       |           |                   |       |       |       |    |
| High Level V <sub>OH</sub>                                                  | —                     | 0                      | 5                      | 4.95 Min.; 5 Typ.                     |                   |      |       |           |                   |       |       |       | V  |
|                                                                             | —                     | 0                      | 10                     | 9.95 Min., 10 Typ.                    |                   |      |       |           |                   |       |       |       |    |
| Noise Immunity: Inputs Low, V <sub>NL</sub>                                 | 4.2                   | —                      | 5                      | 1.5 Min.; 2.25 Typ.                   |                   |      |       |           |                   |       |       |       | V  |
|                                                                             | 9                     | —                      | 10                     | 3 Min.; 4.5 Typ.                      |                   |      |       |           |                   |       |       |       |    |
| Inputs High V <sub>NH</sub>                                                 | 0.8                   | —                      | 5                      | 1.5 Min.; 2.25 Typ.                   |                   |      |       |           |                   |       |       |       | V  |
|                                                                             | 1                     | —                      | 10                     | 3 Min.; 4.5 Typ.                      |                   |      |       |           |                   |       |       |       |    |
| Noise Margin: Inputs Low, V <sub>NML</sub>                                  | 4.5                   |                        | 5                      | 1 Min.                                |                   |      |       |           |                   |       |       |       | V  |
|                                                                             | 9                     |                        | 10                     | 1 Min.                                |                   |      |       |           |                   |       |       |       |    |
| Inputs High, V <sub>NMH</sub>                                               | 0.5                   |                        | 5                      | 1 Min.                                |                   |      |       |           |                   |       |       |       | V  |
|                                                                             | 1                     |                        | 10                     | 1 Min.                                |                   |      |       |           |                   |       |       |       |    |
| Output Drive Current: (Q, Q Outputs) n-channel (Sink), I <sub>DN</sub> Min. | 0.5                   | —                      | 5                      | 0.5                                   | 0.8               | 0.4  | 0.28  | 0.34      | 0.8               | 0.28  | 0.23  | mA    |    |
|                                                                             | 0.5                   | —                      | 10                     | 1.25                                  | 2                 | 1    | 0.7   | 0.85      | 2                 | 0.7   | 0.6   |       |    |
| p-Channel (Source): I <sub>DP</sub> Min.                                    | 4.5                   | —                      | 5                      | -0.5                                  | -0.8              | -0.4 | -0.28 | -0.34     | -0.8              | -0.28 | -0.23 | mA    |    |
|                                                                             | 9.5                   | —                      | 10                     | -1.25                                 | -2                | -1   | -0.7  | -0.85     | -2                | -0.7  | -0.6  |       |    |
| Input Leakage Current, I <sub>IL</sub> , I <sub>IH</sub>                    | Any Input             |                        | 15                     | ±10 <sup>-5</sup> Typ., ±1 Max.       |                   |      |       |           |                   |       |       |       | μA |

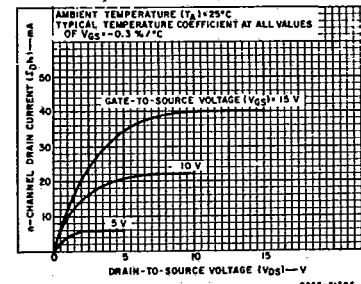


Fig. 2 — Typical output n-channel drain characteristics for  $Q$  and  $\bar{Q}$  buffers.

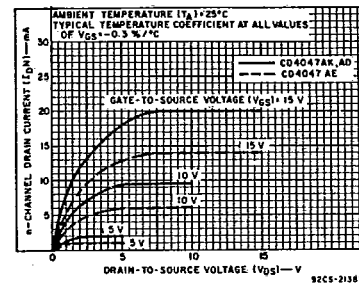


Fig. 3 — Minimum output n-channel drain characteristics for  $Q$  and  $\bar{Q}$  buffers.

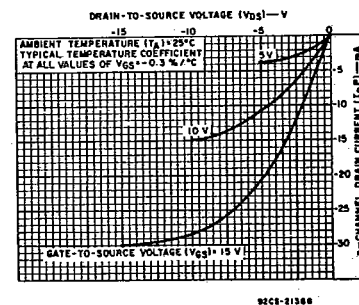


Fig. 4 — Typical output p-channel drain characteristics for  $Q$  and  $\bar{Q}$  buffers.

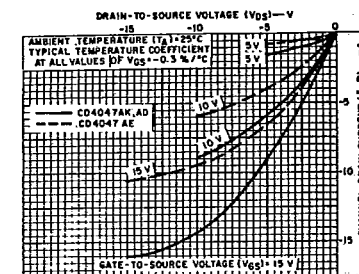


Fig. 5 — Minimum output p-channel drain characteristics for  $Q$  and  $\bar{Q}$  buffers.

## CD4047A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 15\text{ pF}$ ,  
 $R_L = 200\text{ k}\Omega$

| CHARACTERISTICS                                                                     | TEST<br>CONDITIONS | LIMITS         |                        |      |      |              |      | UNITS |         |
|-------------------------------------------------------------------------------------|--------------------|----------------|------------------------|------|------|--------------|------|-------|---------|
|                                                                                     |                    | VDD<br>(Volts) | D, F, K, H<br>Packages |      |      | E<br>Package |      |       |         |
|                                                                                     |                    |                | Min.                   | TYP. | MAX. | Min.         | TYP. |       | MAX.    |
| Propagation Delay Time:<br>$t_{PHL}$ , $t_{PLH}$<br>Astable, Astable<br>to Osc. Out |                    | 5              | —                      | 200  | 400  | —            | 200  | 550   | ns      |
|                                                                                     |                    | 10             | —                      | 100  | 200  | —            | 100  | 275   |         |
| Astable, Astable<br>to Q, $\bar{Q}$                                                 |                    | 5              | —                      | 550  | 900  | —            | 550  | 1200  |         |
|                                                                                     |                    | 10             | —                      | 250  | 500  | —            | 250  | 650   |         |
| +Trigger, —Trigger<br>to Q, $\bar{Q}$                                               |                    | 5              | —                      | 700  | 1200 | —            | 700  | 1600  |         |
|                                                                                     |                    | 10             | —                      | 300  | 600  | —            | 300  | 800   |         |
| +Trigger, Retrigger<br>to Q, $\bar{Q}$                                              |                    | 5              | —                      | 300  | 600  | —            | 300  | 800   |         |
|                                                                                     |                    | 10             | —                      | 175  | 300  | —            | 175  | 400   |         |
| External Reset<br>to Q, $\bar{Q}$                                                   |                    | 5              | —                      | 300  | 600  | —            | 300  | 800   |         |
|                                                                                     |                    | 10             | —                      | 125  | 250  | —            | 125  | 350   |         |
| Transition Time:<br>$t_{THL}$ , $t_{TLH}$<br>Q, $\bar{Q}$                           |                    | 5              | —                      | 75   | 125  | —            | 75   | 150   | ns      |
|                                                                                     |                    | 10             | —                      | 45   | 75   | —            | 45   | 100   |         |
| Osc. Out                                                                            |                    | 5              | —                      | 75   | 150  | —            | 75   | 180   | ns      |
|                                                                                     |                    | 10             | —                      | 45   | 100  | —            | 45   | 130   |         |
| Minimum Input Pulse<br>Width (any input), $t_W^*$                                   |                    | 5              | —                      | 500  | 1000 | —            | 500  | 1300  | ns      |
|                                                                                     |                    | 10             | —                      | 200  | 400  | —            | 200  | 600   |         |
| +Trigger, Retrigger<br>Rise & Fall Time, $t_r$ , $t_f$                              |                    | 5              | —                      | —    | 15   | —            | —    | 15    | $\mu$ s |
|                                                                                     |                    | 10             | —                      | —    | 5    | —            | —    | 5     |         |
| Average Input<br>Capacitance, $C_i$                                                 | Any<br>Input       | —              | —                      | 5    | —    | —            | 5    | —     | pF      |

\* Input pulse widths below the minimum specified may cause malfunction of the unit.  
 See Application Note ICAN - 6230

## CD4047A FUNCTIONAL TERMINAL CONNECTIONS

NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲  
 EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

| FUNCTION                  | TERMINAL CONNECTIONS  |            |                | OUTPUT PULSE FROM | OUTPUT PERIOD OR PULSE WIDTH |
|---------------------------|-----------------------|------------|----------------|-------------------|------------------------------|
|                           | TO VDD                | TO VSS     | INPUT PULSE TO |                   |                              |
| Astable Multivibrator:    |                       |            |                |                   |                              |
|                           | Free Running          | 4,5,6,14   | 7,8,9,12       | —                 | $t_A(10,11)=4.40\text{ RC}$  |
|                           | True Gating           | 4,6,14     | 7,8,9,12       | 5                 | $t_A(13)=2.20\text{ RC}$     |
| Complement Gating         | 6,14                  | 5,7,8,9,12 | 4              | 10,11,13          |                              |
| Monostable Multivibrator: |                       |            |                |                   |                              |
|                           | Positive-Edge Trigger | 4,14       | 5,6,7,9,12     | 8                 | $t_M(10,11)=2.48\text{ RC}$  |
|                           | Negative-Edge Trigger | 4,8,14     | 5,7,9,12       | 6                 |                              |
|                           | Retriggerable         | 4,14       | 5,6,7,9        | 8,12              |                              |
|                           | External Countdown*   | 14         | 5,6,7,8,9,12   | —                 |                              |
|                           |                       |            |                | 10,11             |                              |

\* Input Pulse to Reset of External Counting Chip External Counting Chip Output To Terminal 4 ▲ See Text.

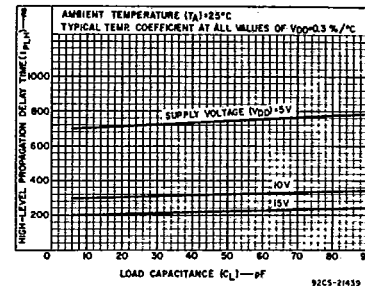


Fig. 6 — Typical low-to-high level propagation delay time vs load capacitance for Q and  $\bar{Q}$  buffers.

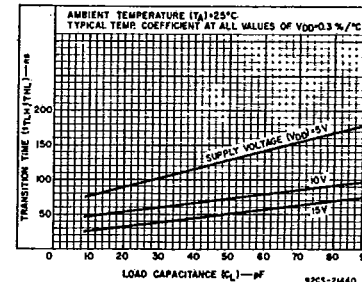


Fig. 7 — Typical transition time vs load capacitance for Q and  $\bar{Q}$  buffers.

## 1. Astable Mode Design Information

## A. Unit-to-Unit Transfer-Voltage Variations.

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage ( $V_{TR}$ ) shift (33%–67%  $V_{DD}$ ) for free-running (astable) operation.

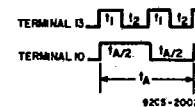


Fig. 8 — Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2)$$

$$= -2RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

$$\text{Typ: } V_{TR} = 0.5 V_{DD} \quad t_A = 4.40\text{ RC}$$

$$\text{Min: } V_{TR} = 0.33 V_{DD} \quad t_A = 4.62\text{ RC}$$

$$\text{Max: } V_{TR} = 0.67 V_{DD} \quad t_A = 4.62\text{ RC}$$

thus if  $t_A = 4.40\text{ RC}$  is used, the maximum variation will be (+5.0%, -0.0%).

## CD4047A Types

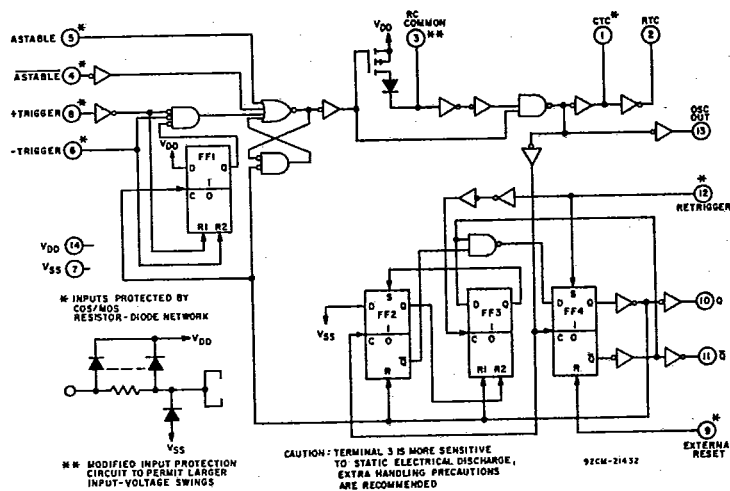


Fig. 9 - CD4047A logic diagram.

B. Variations Due to  $V_{DD}$  and Temperature Changes

In addition to variations from unit to unit, the astable period may vary as a function of frequency with respect to

$V_{DD}$  and temperature. Typical variations are presented in graphical form in Figs. 10 to 20 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

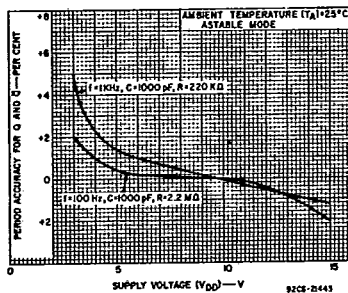
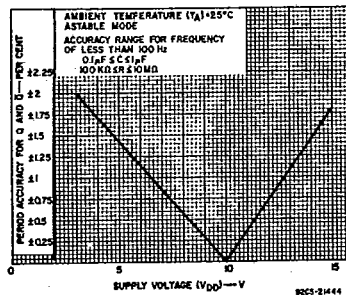
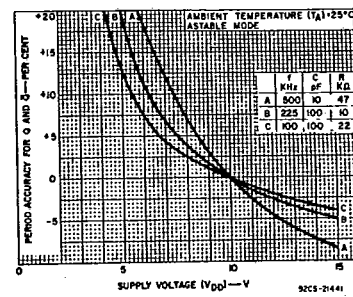
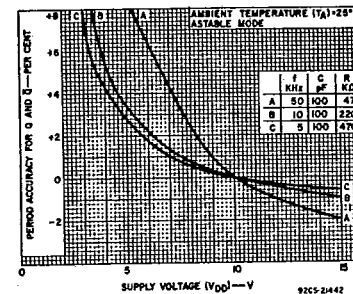
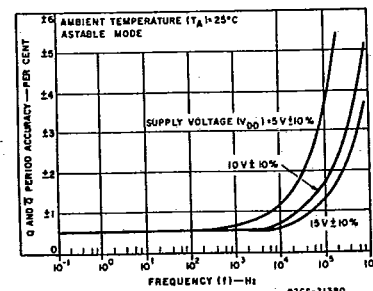
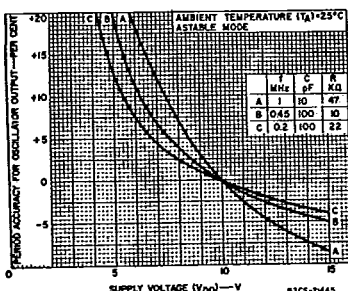
Fig. 12 - Typical Q and  $\bar{Q}$  period accuracy vs supply voltage (low frequency).Fig. 13 - Typical Q and  $\bar{Q}$  period accuracy vs supply voltage (very low frequency).Fig. 10 - Typical Q and  $\bar{Q}$  period accuracy vs supply voltage (high frequency).Fig. 11 - Typical Q and  $\bar{Q}$  period accuracy vs supply voltage (medium frequency).Fig. 14 - Typical Q and  $\bar{Q}$  period accuracy vs frequency for  $V_{DD}$  variation of  $\pm 10\%$  from value indicated.

Fig. 15 - Typical oscillator-output-period accuracy vs supply voltage (high frequency).

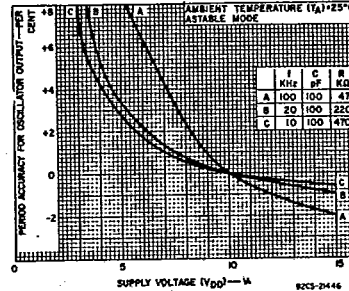
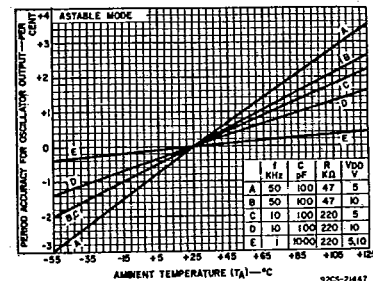


Fig. 16 - Typical oscillator-output-period accuracy vs supply voltage (medium frequency).

Fig. 17 - Typical Q and  $\bar{Q}$  period accuracy vs temperature (medium frequency).

## CD4047A Types

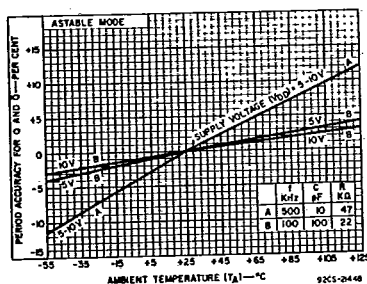


Fig. 18 - Typical Q and Q-bar period accuracy vs temperature (high frequency).

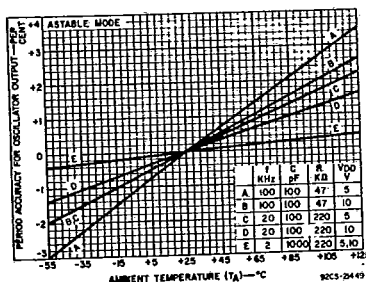


Fig. 19 - Typical oscillator-period accuracy vs temperature (medium frequency).

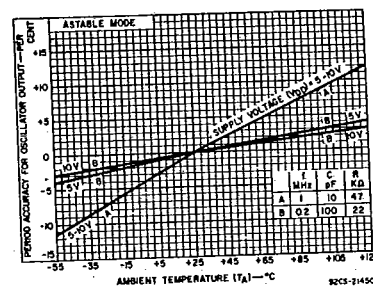


Fig. 20 - Typical oscillator-period accuracy vs temperature (high frequency).

## II. Monostable Mode Design Information

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage ( $V_{TR}$ ) shift (33% - 67%  $V_{DD}$ ) for one-shot (monostable) operation.

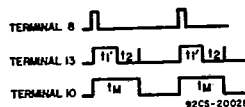


Fig. 21 - Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where  $t_M$  = Monostable mode pulse width.  
Values for  $t_M$  are as follows:

Typ:  $V_{TR} = 0.5 V_{DD}$   $t_M = 2.48 RC$   
Min:  $V_{TR} = 0.33 V_{DD}$   $t_M = 2.71 RC$   
Max:  $V_{TR} = 0.67 V_{DD}$   $t_M = 2.48 RC$

Thus if  $t_M = 2.48 RC$  is used, the maximum variation will be (+9.3%, -0.0%).

### Note:

In the astable mode, the first positive half cycle has a duration of  $T_M$ ; succeeding durations are  $T_A/2$ .

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to  $V_{DD}$  and temperature. These variations are presented in graphical form in Fig. 22 to 27 with 10 V as reference for voltage-variation curves and 25°C as reference for temperature-variation curves.

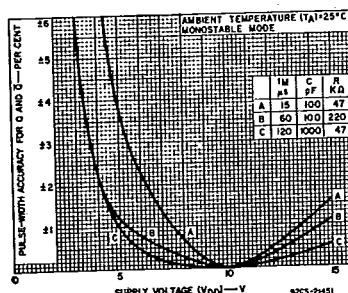


Fig. 22 - Typical Q and Q-bar pulse-width accuracy vs supply voltage ( $t_M = 15, 60, 120 \mu s$ ).

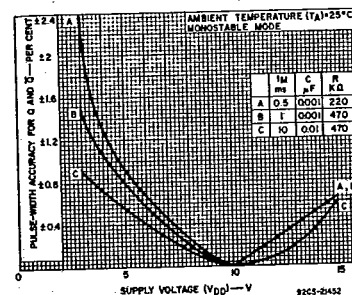


Fig. 23 - Typical Q and Q-bar pulse-width accuracy vs supply voltage ( $t_M = 0.5, 1, 10 ms$ ).

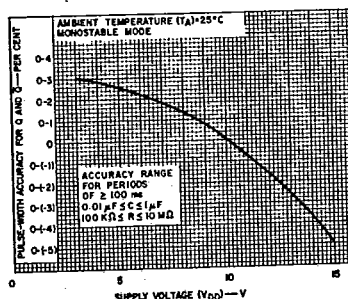


Fig. 24 - Typical Q and Q-bar pulse-width accuracy vs supply voltage ( $t_M \geq 100 \mu s$ ).

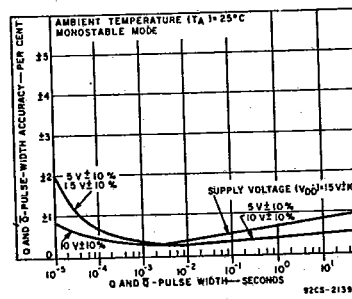


Fig. 25 - Typical Q and Q-bar pulse-width accuracy vs Q and Q-bar pulse width for a variation of  $\pm 10\%$  from value indicated.

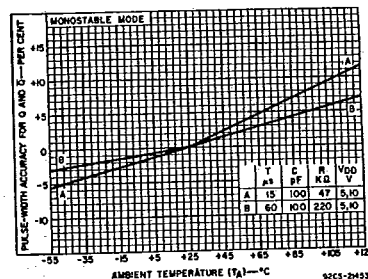


Fig. 26 - Typical Q and Q-bar pulse-width accuracy range vs temperature (high frequency).

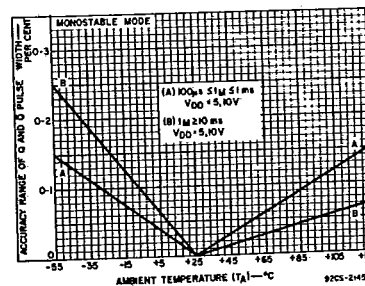


Fig. 27 - Typical Q and Q-bar pulse-width accuracy range vs temperature.

## CD4047A Types

### III. Retrigger Mode Operation

The CD4047A can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. 28, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input-pulses,  $t_{RE} = t_1' + t_1 + 2t_2$ . For more than two pulses,  $t_{RE}$  (Q OUTPUT), terminates at some variable time,  $t_D$ , after the termination of the last retrigger pulse,  $t_D$  is variable because  $t_{RE}$  (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig. 8).

### IV. External Counter Option

Time  $t_M$  can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 29. The pulse duration at the output is  $t_{ext} = (N-1)(t_A) + (t_M + t_A/2)$  where  $t_{ext}$  = pulse duration of the circuitry, and  $N$  is the number of counts used.

### V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either  $R$  or  $C$  value to maintain oscillation. However, in consideration of accuracy,  $C$  must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account).  $R$  must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of  $R$ , some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geq 100$  pF, up to any practical value, for astable modes;  
 $C \geq 1000$  pF, up to any practical value for monostable modes.

$$10 \text{ k}\Omega \leq R \leq 1 \text{ M}\Omega$$

### VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor  $C$  is given by the following formulae:

Astable Mode:  $P = 2CV^2f$ , (Output at terminal No. 13)  
 $P = 4CV^2f$ , (Output at terminal Nos. 10 and 11)

Monostable Mode:

$$P = \frac{(2.9CV^2) (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on  $R$ , a design for minimum power dissipation would be a small value of  $C$ . The value of  $R$  would depend on the desired period (within the limitations discussed above). See Figs. 30-32 for typical power consumption in astable mode.

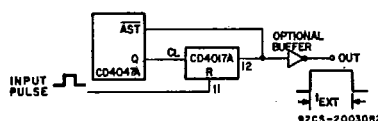


Fig. 28 - Implementation of external counter option.

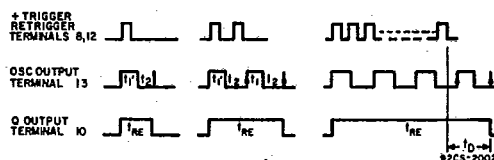


Fig. 29 - Retrigger-mode waveforms.

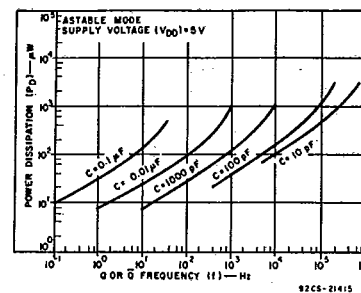


Fig. 30 - Power dissipation vs output frequency ( $V_{DD} = 5 \text{ V}$ ).

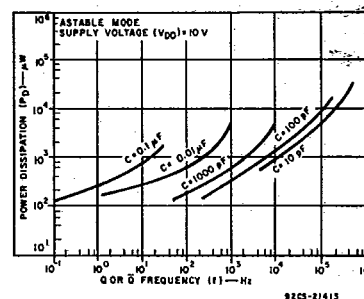


Fig. 31 - Power dissipation vs output frequency ( $V_{DD} = 10 \text{ V}$ ).

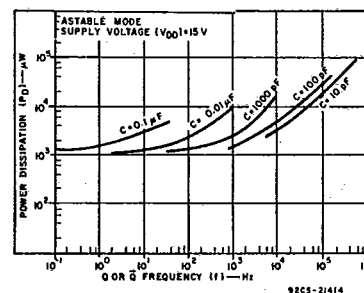


Fig. 32 - Power dissipation vs output frequency ( $V_{DD} = 15 \text{ V}$ ).