



MC33664

Isolated network high-speed transceiver

Rev. 1.0 — 23 May 2018

Short data sheet: technical data

1 General description

The MC33664 is a SMARTMOS transceiver physical layer transformer driver designed to interface a microcontroller conveniently to a high speed isolated communication network. MCU serial peripheral interface (SPI) data bits are directly converted to pulse bit information and transferred to the bus network.

Slave response messages use the same structure to send pulse bit information to the MC33664, which is converted and sent back to the MCU as a SPI bit stream.

2 Features and benefits

- 2.0 Mbit/s isolated network communication rate
- Dual SPI architecture for message confirmation
- Robust conducted and radiated immunity with wake-up
- 3.3 V and 5.0 V compatible logic thresholds
- Low sleep mode current with automatic bus wake-up
- Ultra-low radiated emissions

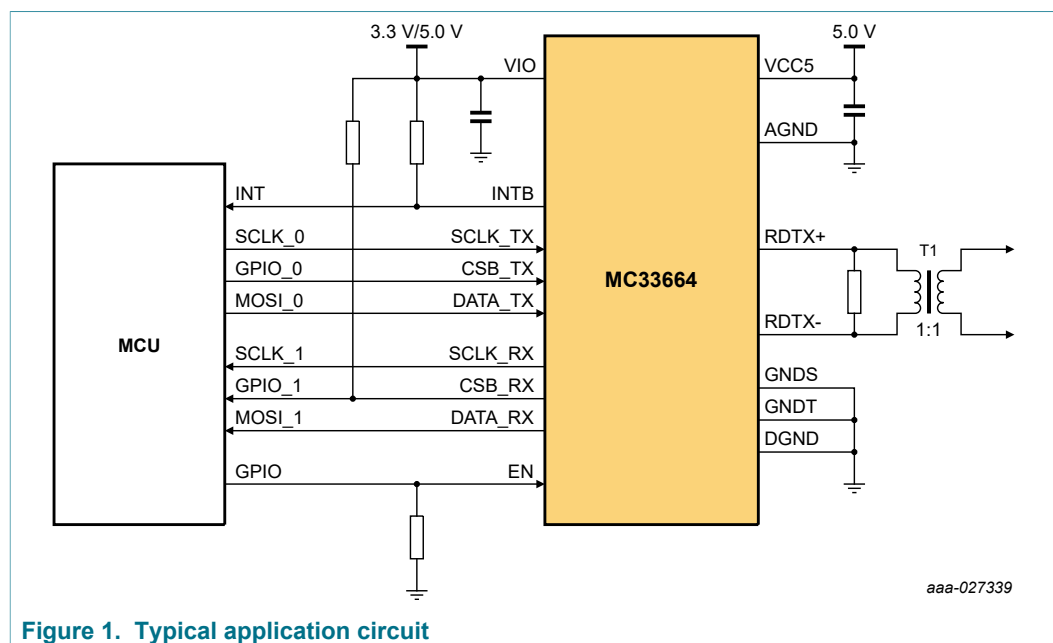


Figure 1. Typical application circuit

3 Applications

- Automotive communication network
- Industrial communication network
- Utility vehicle battery systems
- Forklift/mining battery systems
- Battery backup systems

4 Ordering information

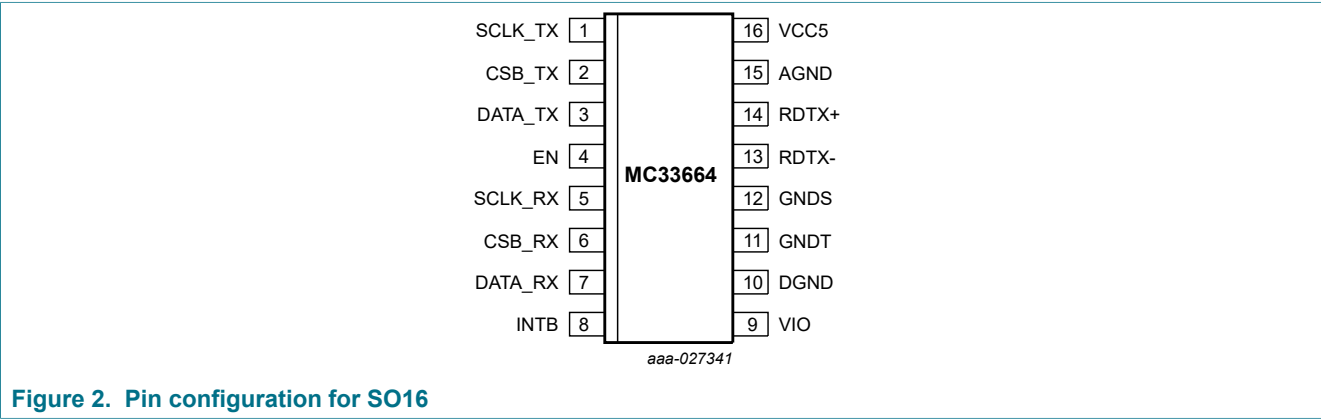
Table 1. Ordering information

Type number	Package			
	Name	Description	T _{amb} [°C]	Version
MC33664ATL1EG ^[1]	SO16	plastic small outline package; 16 leads; 1.27 mm pitch; body 9.9 mm × 3.9 mm × 1.75 mm	–40 to +125	SOT109-5

[1] To order parts in tape and reel, add R2 suffix to the part number.

5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
SCLK_TX	1	input	SPI transmit clock from the microcontroller to the MC33664
CSB_TX	2	input	SPI transmit chip select from the microcontroller to the MC33664
DATA_TX	3	input	SPI transmit data from the microcontroller to the MC33664
EN	4	input	enable control pin for the MCU to control the MC33664 to Sleep mode or Normal mode
SCLK_RX	5	output	message receive SPI clock output to the microcontroller
CSB_RX	6	output	message receive SPI chip select output to the microcontroller
DATA_RX	7	output	message receive SPI data output to the microcontroller
INTB	8	output	digital interrupt pin used to trigger MCU wake-ups
VIO	9	power	digital 3.3 V/5.0 V power to the IC
DGND	10	ground	digital ground
GNDT	11	ground	terminate to ground
GNDS	12	ground	substrate ground; terminate to ground
RDTX-	13	I/O	transformer communication bi-directional bus
RDTX+	14	I/O	transformer communication bi-directional bus
AGND	15	ground	analog ground
VCC5	16	input	5.0 V input supply

6 Ratings and operating requirements relationship

The operating voltage range pertains to the VCC5 and VIO pins referenced to the AGND and DGND pins.

Table 3. Ratings versus operating requirements

Fatal range	Lower limited operating range	Normal operating range	Upper limited operating range	Fatal range
V _{PWR} < -0.3 V Permanent failure may occur	4.5 V ≤ V _{CC5} ≤ 4.75 V no permanent failure, but IC functionality is not guaranteed	4.75 V ≤ V _{CC5} ≤ 5.5 V 3.1 V ≤ V _{IO} ≤ 5.5 V 100 % functional	5.5 V ≤ V _{CC5} ≤ 7.0 V 5.5 V ≤ V _{IO} ≤ 7.0 V	7.0 V ≤ V _{CC5} 7.0 V ≤ V _{IO} permanent failure may occur
	0 V ≤ V _{CC5} ≤ 4.5 V 0 V ≤ V _{IO} ≤ 3.1 V reset			
	handling range; no permanent failure			

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

All voltages are respect to reference ground (AGND and DGND) unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IO}	supply input voltage		-0.3	+7.0	V
V_{CC5}	supply input voltage		-0.3	+7.0	V
EN	digital enable pin for Sleep or Normal mode		-0.3	$V_{IO} + 0.3$	V
RDTX+, RDTX-	communication bus		-10	+10	V
INTB	interrupt pin		-0.3	$V_{IO} + 0.3$	V
SCLK_TX, SCLK_RX, CSB_TX, CSB_RX, DATA_TX, DATA_RX	serial peripheral interface communication ports		-0.3	$V_{IO} + 0.3$	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM) ^[1]	±2000	-	V
		charge device model (CDM)	±500	-	V
		CDM corner pins	±750	-	V
		machine model (MM)	±200	-	V
		RDTX+, RDTX-; HBM	±4000	-	V
		RDTX+, RDTX-; MM	±200	-	V

[1] Electrostatic discharge (ESD) testing is performed in accordance with the HBM ($C_{ZAP} = 100\text{ pF}$, $R_{ZAP} = 1500\text{ }\Omega$).

8 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		-40	+125	°C
T_j	junction temperature	[1]	-40	+150	°C
T_{stg}	storage temperature		-55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	[2] [3]	-	260	°C
$R_{th(j-a)}$	thermal resistance from junction to ambient	single layer (1s) [4]	-	125	°C/W
$R_{th(j-pcb)}$	thermal resistance from junction to printed-circuit board	multi layer (2s2p) [5]	-	62	°C/W

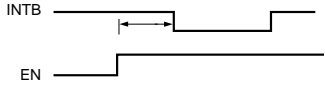
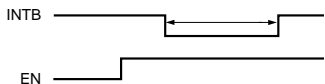
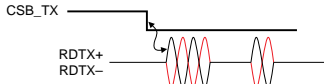
- [1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- [2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- [3] Package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to <http://www.nxp.com>, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxx enter 33xxx)], and review parametric.
- [4] Per SEMI G38-87 and JEDEC standard JESD51-2 with the single-layer board horizontal.
- [5] Indicates the maximum thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

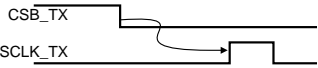
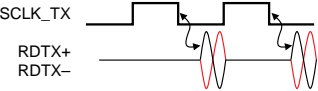
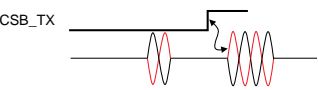
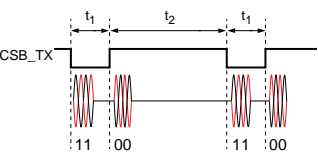
9 Characteristics

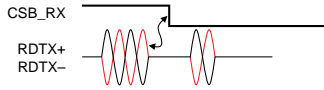
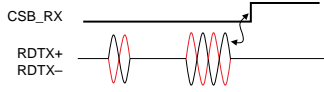
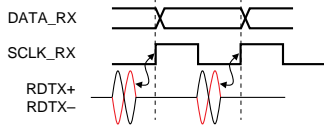
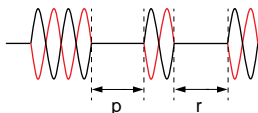
Table 6. Characteristics

Characteristic noted under conditions $4.75\text{ V} \leq V_{CC5} \leq 5.5\text{ V}$, $3.1\text{ V} \leq V_{IO} \leq 5.5\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_{amb} \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $V_{CC5} = 5.0\text{ V}$, $V_{IO} = 3.3\text{ V}/5.0\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ and device operating under nominal conditions unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply VCC5						
V_{CC5}	supply voltage	fully operational	4.75	—	5.5	V
		limited operation	4.5	—	4.75	V
$I_{VCC5(NORMAL)}$	supply current	Normal mode; EN = 1; continuous transmit; 50 Ω load		40		mA
		Normal mode; EN = 1; continuous receive		3.0		mA
$I_{VCC5(SLEEP)}$	supply current	Sleep mode; EN = 0; INTB = 5.0 V		30		μA
$V_{CC5_{UV}}$	VCC5 undervoltage POR threshold		4.0	—	4.5	V
$V_{CC5_{UV_FLT}}$	VCC5 undervoltage POR filter			2.5		μs
$V_{CC5_{UVHYS}}$	VCC5 undervoltage POR hysteresis			100		mV
Power supply VIO						
V_{IO}	supply voltage		3.1	—	5.5	V
$V_{IO_{UV}}$	VIO undervoltage POR threshold		2.2	—	3.1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IO_UV_FLT}	VIO undervoltage POR filter			2.5		μs
V _{IO_UVHYS}	VIO undervoltage POR hysteresis			100		mV
I _{VIO(SLEEP)}	VIO sleep current	EN = 0; INTB = 1	0.1	—	4.5	μA
I _{VIO(NORMAL)}	VIO Normal mode current	EN = 1; continuous communication; SPI_1 open		1.0		mA
Logic transmit EN, CSB_TX, SCLK_TX, DATA_TX						
V _{IH}	HIGH-level input voltage		1.7	—	V _{IO} + 0.3	V
V _{IL}	LOW-level input voltage		—	—	0.95	V
V _{hys}	hysteresis voltage			150		mV
R _{pd}	pull-down resistance	EN, SCLK_TX, DATA_TX		100		kΩ
R _{pu}	pull-up resistance	CSB_TX		100		kΩ
t _{READY}	Sleep mode to Normal mode	EN LOW to HIGH transition to device ready to transmit	—	—	100	μs
t _{INTB_PULSE_DELAY}	EN LOW to HIGH transition to INTB verification pulse		—	—	100	μs
						
t _{INTB_PULSE}	INTB verification pulse duration		—	100	—	μs
						
f _{SCLK_TX}	SPI_0 frequency	SCLK_TX		2.0		MHz
a	SCLK_TX HIGH	see Figure 3		250		ns
b	SCLK_TX LOW	see Figure 3		250		ns
e	SCLK_TX to CSB_TX	see Figure 3	—	250	—	ns
L	CSB_TX to start of message		—	—	1.1	μs
						

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f	falling edge of CSB_TX to rising edge SCLK_TX 	see Figure 3	1.75	—	—	μs
t _{RDTX_DLY}	propagation delay 	SCLK_TX LOW to sine out ^[1]	—	80	150	ns
g	SCLK_TX LOW to CSB_TX HIGH	see Figure 3	600	—	—	ns
c	DATA_TX to SCLK_TX setup	see Figure 3	40	—	—	ns
d	DATA_TX hold	see Figure 3	40	—	—	ns
t _{CSB_TX_HIGH_EOM}	propagation delay 	CSB_TX LOW to HIGH to end of message ^[1]	—	—	150	ns
t ₁	CSB_TX wake#up pulse sequence timing 	CSB_TX LOW period		21		μs
t ₂		CSB_TX HIGH period		600		μs
h	time between consecutive transmit messages	see Figure 3	1.0	3.0	—	μs
Logic receive pins (CSB_RX, SCLK_RX, DATA_RX)						
V _{OH}	HIGH-level output voltage	I _{OH} = -2.0 mA; V _{IO} = 3.1 V	V _{IO} - 0.4	—	—	V
V _{OL}	LOW-level output voltage	I _{OL} = -2.0 mA; V _{IO} = 3.1 V	—	—	0.4	V
f _{SPI}	SPI_1 frequency	SCLK_RX		2.0		MHz
q	pulse frequency	see Figure 4		4.0		MHz
o	start of message	see Figure 4 ^[1]		500		ns
a	SCLK_RX HIGH	^[1]		250		ns
b	SCLK_RX LOW	^[1]		250		ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
t _{SOM_CSB_RX}	start of message to CSB_RX 	[1]		160		ns	
t _{EOM_CSB_RX}	end of message to CSB_RX 	[1]		60		ns	
t _{PDB_SCLK_DATA_RX}	pulse data bit to DATA_RX and SCLK_RX 	[1]		280		ns	
r	start of message to MSB (receive)	see Figure 4	[1]	—	250	—	ns
p		see Figure 4	[1]	—	600	—	ns
m	time between consecutive messages received	see Figure 4	1.0	3.0	—	μs	
Bus differential transmitter/receiver							
V _{RDTX(PK_DIFF)}	RDTX± differential output voltage	R _L = 50 Ω; V _{CC5} = 4.75 V		2.5		V	
I _{RDTX}	RDTX± current limit	sinking/sourcing to 2.5 V	65	—	300	mA	
V _{RDTX_IN(TH)}	RDTX± differential receiver threshold voltage	rising edge		0.74		V	
		falling edge		0.61	0.70	V	
V _{RDTX_IN_HYST}	RDTX± differential receiver threshold voltage hysteresis			130		mV	
V _{RDTX_BIAS}	transformer bias voltage	transmitter in 3-state		2.5		V	
f _{RDTX}	transmit/receive pulse frequency			4.0		MHz	
Wake-up receiver							
V _{RDTXWU_TH}	RDTX± wake#up differential receiver threshold voltage	rising edge		0.6		V	
		falling edge		0.6		V	
V _{RDTXWU_TH_HYS}	RDTX± wake#up differential receiver threshold hysteresis			100		mV	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{RDTXWU_FLT}	RDTX± wake#up filter			50		ns

[1] All bus network signals to SPI timing are referenced to 0.8 V differential threshold.

9.1 Timing diagrams

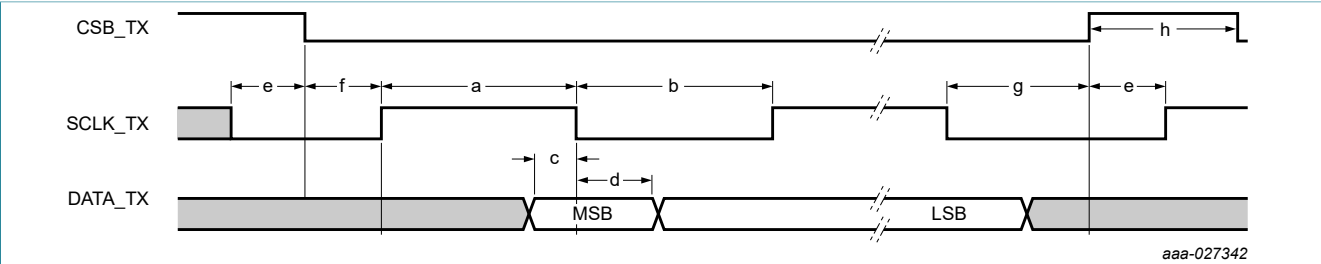


Figure 3. SPI transmit timing

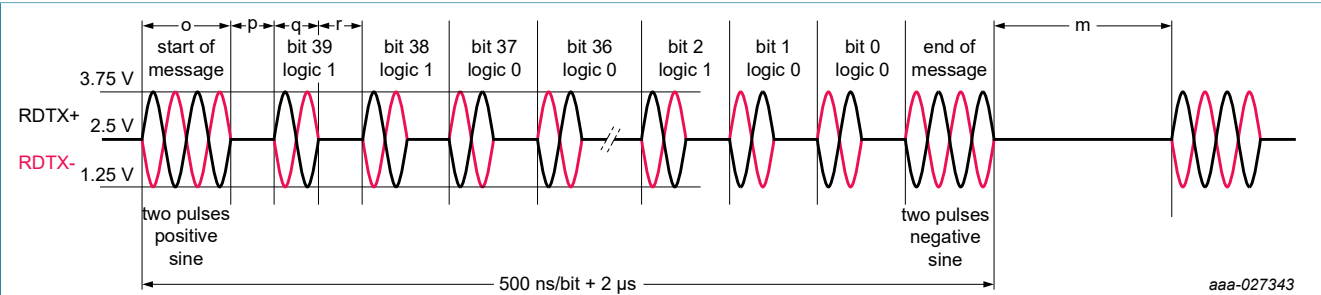


Figure 4. Transformer receive communication timing

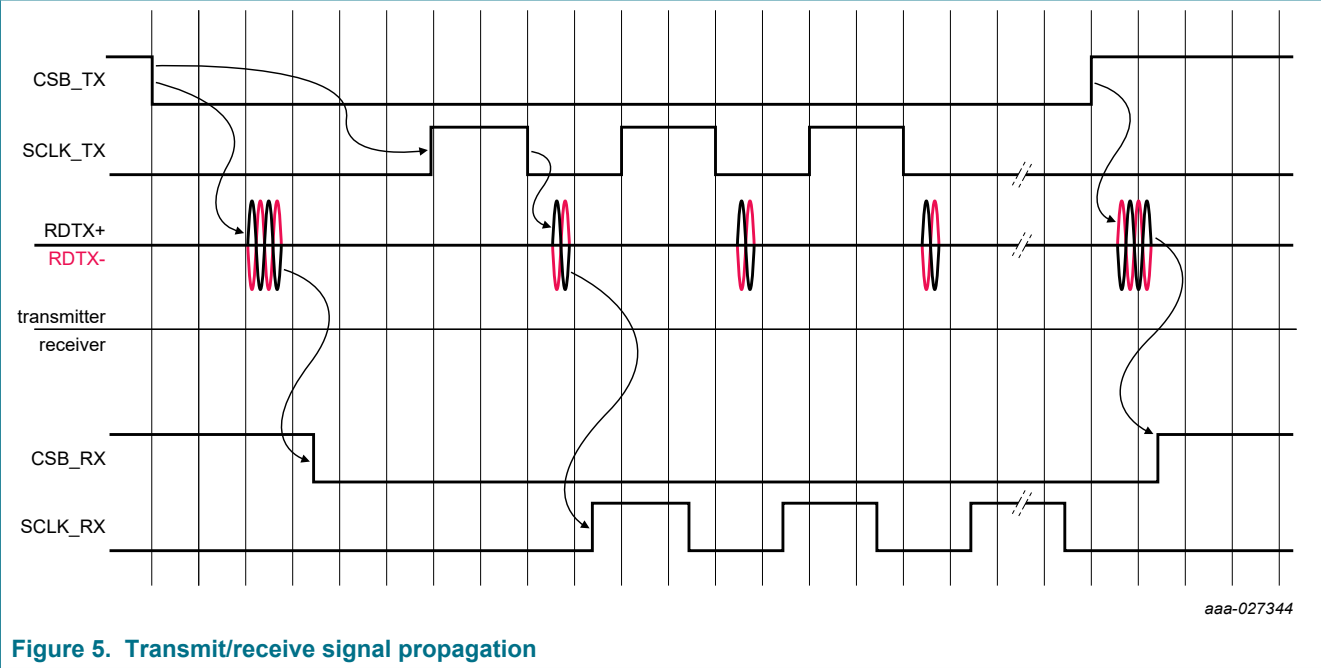
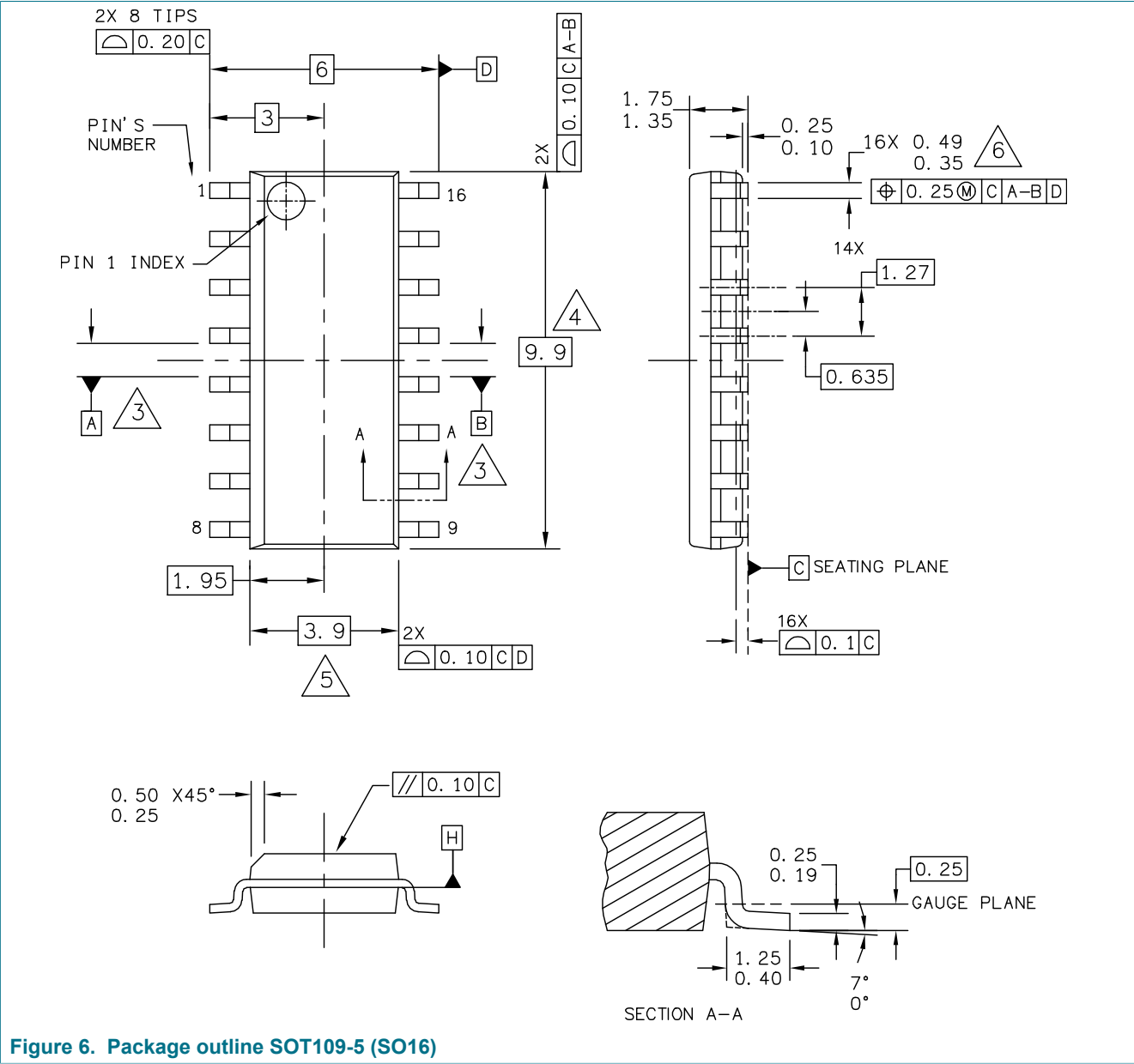


Figure 5. Transmit/receive signal propagation

10 Package outline



11 Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33664_SDS v.1.0	20180523	Technical data	—	—

12 Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
[short] Data sheet: product preview	Development	This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.
[short] Data sheet: advance information	Qualification	This document contains information on a new product. Specifications and information herein are subject to change without notice.
[short] Data sheet: technical data	Production	This document contains the product specification. NXP Semiconductors reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a technical data data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the technical data data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without

limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive

applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

POR — is a trademark of NXP B.V.

SMARTMOS — is a trademark of NXP B.V.

Tables

Tab. 1.	Ordering information	2	Tab. 5.	Thermal characteristics	5
Tab. 2.	Pin description	3	Tab. 6.	Characteristics	5
Tab. 3.	Ratings versus operating requirements	4	Tab. 7.	Revision history	11
Tab. 4.	Limiting values	4			

Figures

Fig. 1.	Typical application circuit	1	Fig. 4.	Transformer receive communication timing	9
Fig. 2.	Pin configuration for SO16	3	Fig. 5.	Transmit/receive signal propagation	10
Fig. 3.	SPI transmit timing	9	Fig. 6.	Package outline SOT109-5 (SO16)	11

Contents

1	General description	1
2	Features and benefits	1
3	Applications	2
4	Ordering information	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Ratings and operating requirements relationship	4
7	Limiting values	4
8	Thermal characteristics	5
9	Characteristics	5
9.1	Timing diagrams	9
10	Package outline	11
11	Revision history	11
12	Legal information	12

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2018.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 23 May 2018
Document identifier: MC33664_SDS