

EMI MITIGATING 2.1X 5 W CLASS D AUDIO AMPLIFIER

Features

- Digital input Delta-Sigma PWM
- Patent-pending EMI mitigation
- AM radio band noise-free notch
- GSM/iPhone friendly
- Wideband PWM carrier spreading
- Power stage slew rate control
- Power stage feedback for PSR/THD
- 2x 5 W @ 3 Ω BTL; 2x 3 W @ 8 Ω BTL
- 88% efficiency with >50 dB PSRR
- 95 dB dynamic range and <0.1% THD
- Stereo PWM DAC line analog outputs
- Master/slave I²S w/ 3 inputs & 1 output
- Automatic digital audio rate detection
- Standard audio rates from 32–192 kHz
- Audio activity detector w/ auto-standby
- Operates from external XTAL or clock
- Buffered master/regulator clock output
- Programmable 7 band parametric EQ, dynamic range compressor, tone control
- Crossbar input mixer with scaling
- Digital tone and alert generation
- 128 dB volume control in 0.5 dB steps
- Multiple low power operating modes
- Over-current and over-temperature detection w/ auto recovery
- Pop and click free operation
- Standard 2-wire control w/ 2 addresses
- System flexibility w/ 3 multi-function pins
- Dual supply voltage: 2.7–3.6 V main and 4.0–6.6 V power stage
- Available in 4x4 24-pin Power QFN and 7x7 48-pin Power eTQFP package
 - Both Pb-free/RoHS compliant

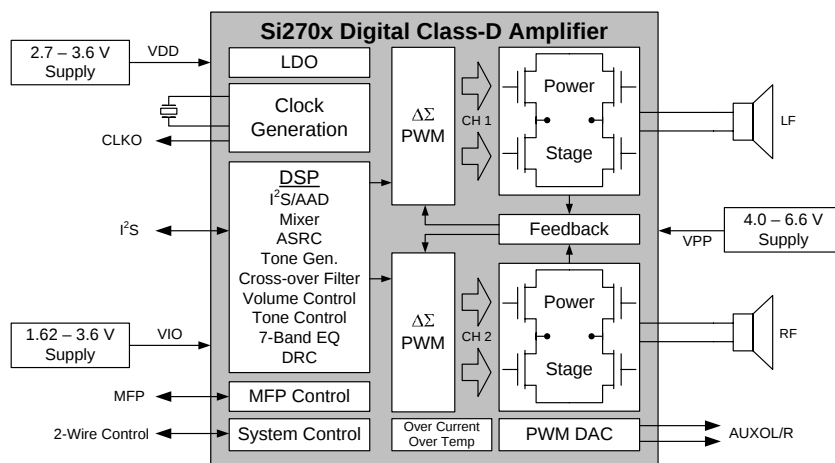
Applications

- PMP/MP3 docking stations
- Portable consumer audio electronics
- Table top and portable radios
- Active/wireless speakers
- TVs and monitors
- TV sound bars

Description

The Si2704/05/06/07 EMI mitigating 2.1 digital audio processing Class D amplifier integrates a power stage, PWM DAC, and digital audio processing (DAP) for simplified, low cost, power efficient system designs in consumer audio electronics. The digital input amplifier features delta-sigma PWM and innovative EMI mitigation technology for producing high-quality audio while effectively managing PWM switching noise for enhanced EMI compliance and AM/FM radio co-existence, while also being GSM/iPhone friendly.

Functional Block Diagram



Ordering Information:
See page 37.

Pin Assignments

Si2704/05/06/07

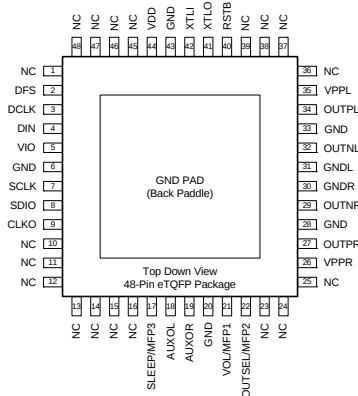
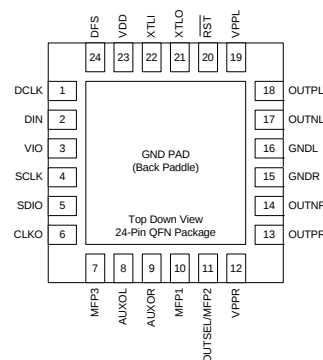


TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
1. Electrical Specifications	5
2. Typical Application Schematic	13
3. Typical System Configurations	14
4. Functional Description	16
4.1. PWM Processing	17
4.1.1. PWM Switching Rate Control	17
4.1.2. EMI Mitigation	17
4.2. Operating Modes	19
4.2.1. Active Mode	19
4.2.2. Standby Mode	20
4.2.3. Sleep Mode	20
4.2.4. Power Down Mode and Reset	20
4.3. Chip Configuration	21
4.3.1. Multi-Function Pins (MFPs)	21
4.3.2. Output Mode Configuration (Si2705/07 only)	22
4.4. Clocking	23
4.4.1. Reference Clock Input	23
4.4.2. Reference Clock Output	23
4.5. Digital Audio I2S Interface	24
4.5.1. Auto-Rate Detection	24
4.5.2. Audio Activity Detector	24
4.5.3. Digital Audio Output	24
4.5.4. Audio data formats	24
4.5.5. I ² S Master Mode	24
4.6. Digital Audio Processing (DAP)	26
4.6.1. Parametric Equalization (Si2706/07 only)	27
4.6.2. Tone Control	27
4.6.3. De-Emphasis (Si2706/07 only)	28
4.6.4. Crossover Filter (Si2706/07 only)	28
4.6.5. Digital Volume Controls	28
4.6.6. Dynamic Range Compression (Si2706/07 only)	29
4.6.7. Hard Signal Limiter	30
4.6.8. DC Notch Filter	30
4.6.9. Tone and Alert Generation	30
4.7. Fault Detection and Response	30
4.8. Power Supply and Grounding Considerations	31
4.9. Control Interface	31
4.10. Programming with Commands	31
5. Commands and Properties	32
6. Pin Descriptions	34
6.1. 24-Pin QFN Package	34
6.2. 48-Pin eTQFP Package	35
7. Ordering Guide	37
8. Package Outline	38

8.1. 24-Pin QFN Package38

8.2. 48-Pin eTQFP Package39

9. Package Markings (Top Marks)41

9.1. Si2707 Top Mark (QFN)41

9.2. Top Mark Explanation41

9.3. Si2707 Top Mark (eTQFP)42

9.4. Top Mark Explanation42

10. Additional Reference Resources43

Document Change List44

Contact Information46

1. Electrical Specifications

Table 1. Recommended Operating Conditions¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Output Supply Voltage	V_{PP}		4.0 ²	—	6.6	V
Main Supply Voltage	V_{DD}		2.7	3.3	3.6	V
Interface (I/O) Supply Voltage	V_{IO}		1.62	—	3.6	V
Load Impedance	R_L		—	3–8	—	Ω
Ambient Temperature	T_A		–20	25	85	°C
Junction Temperature	T_J		—	—	135	°C
Case Delta from Junction	θ_{JC}	Temperature delta between junction and top center of package	—	—	5	°C/W
Delta from Junction to Ambient ³	θ_{JA}	QFN package	—	25	—	°C/W
		eTQFP	—	30	—	°C/W

Notes:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_{DD} = 3.3$ V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.
2. Operation with V_{PP} as low as 3 V is possible at reduced performance.
3. The θ_{JA} is layout-dependent; therefore, PCB layout must provide adequate heat-sink capability. The θ_{JA} is specified, assuming adequate ground plane as in “AN470: 270x Layout Guidelines.”

Table 2. Absolute Maximum Ratings¹

Parameter	Symbol	Value	Unit
Power Output Supply Voltage	V_{PP}	–0.5 to 7.0	V
Main Supply Voltage	V_{DD}	–0.5 to 3.9	V
Interface (I/O) Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current ²	I_{IN}	10	mA
Input Voltage ²	V_{IN}	–0.3 to ($V_{IO} + 0.3$)	V
Operating Temperature	T_A	–20 to +85	°C
Junction Temperature	T_J	150	°C
Storage Temperature	T_A	–55 to +150	°C

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. For input pins SCLK, SDIO, DCLK, DFS, DIN, RST, OUTSEL, MFPx.

Table 3. DC Characteristics—Supplies and Interfaces

($V_{DD} = 2.7$ to 3.6 V, $V_{IO} = 1.62$ to 3.6 V, $V_{PP} = 4$ to 6.6 V, $T_A = -20$ to $+85$ °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start Up Time	T_{ONSB}	From Standby Mode with CLKO enabled	—	—	2	ms
		From Standby Mode with CLKO disabled	—	—	20	ms
	T_{ON_SLP}	From Sleep Mode	—	—	20	ms
	T_{ON_PD}	From Power Down Mode	—	—	200	ms
Active Mode Quiescent Supply Current	I_{PQ}	From V_{PP} , No load, Both Channels Active, Spread Mode PWM	—	50	—	mA
		From V_{PP} , No load, Both Channels Active, Normal Mode PWM	—	45	—	mA
	I_{DQ}	From V_{DD}	—	54	—	mA
	I_{IOQ}	From V_{IO} , I ² S Slave Mode, CLKO Disabled	—	1.3	—	mA
Standby Mode Supply Current	I_{PSTB}	Standby Mode	—	0.1	—	mA
	I_{DSTB}	Standby Mode with CLKO enabled	—	8	—	mA
		Standby Mode with CLKO disabled	—	4	—	mA
	I_{IOSTB}	Standby Mode	—	2	—	mA
Sleep Mode Supply Current	I_{PSLP}	SLEEP asserted	—	0.1	—	mA
	$I_{DSL P}$	SLEEP asserted	—	2	—	mA
	I_{IOSLP}	SLEEP asserted	—	1.5	—	mA
Power Down Mode Supply Current	I_{PPD}		—	0.1	—	mA
	I_{DPD}		—	2	—	mA
	I_{IOPD}		—	0.3	—	mA
Input pins SCLK, SDIO, DCLK, DFS, DIN, RST, OUTSEL, MFPx						
High Level Input Voltage	V_{IH}		$0.7 \times V_{IO}$	—	—	V
Low Level Input Voltage	V_{IL}		—	—	$0.3 \times V_{IO}$	V
High Level Input Current	I_{IH}	$V_{IN} = V_{IO} = 3.6$ V	–10	—	10	μA
Low Level Input Current	I_{IL}	$V_{IN} = 0$ V, $V_{IO} = 3.6$ V	–10	—	10	μA
Output pins MFPx, CLKO*						
High Level Output Voltage	V_{OH}	$I_{OUT} = 500$ μA	$0.8 \times V_{IO}$	—	—	V
Low Level Output Voltage	V_{OL}	$I_{OUT} = -500$ μA	—	—	$0.2 \times V_{IO}$	V
High Level Output Current	I_{OH}	$0.8 \times V_{IO}$	—	6	—	mA
Low Level Output Current	I_{OL}	$0.2 \times V_{IO}$	—	6	—	mA
*Note: Valid for the configuration where MFPx is configured as an output or general purpose output.						

Table 4. DC Characteristics—Class D Amplifier(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, V_{PP} = 4 to 6.6 V, T_A = –20 to +85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage Offset	V _{OS}	Differential Output	—	±10	—	mV
Total Drain-Source On-State Resistance (Total Bridge)*	R _{DS(on)}	V _{PP} = 6.6 V, I _O = 1A	—	648	—	mΩ

***Note:** Excludes package bond wire resistance.

Table 5. AC Characteristics—Class D Amplifier(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, V_{PP} = 6.6 V, R_L = 8 Ω, VOL = 0 dBFS, T_A = –20 to +85 °C, unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Continuous Output Power ¹	P _O	THD+N = 10%, f = 1 kHz, R _L = 8 Ω	—	2.7	—	W
		THD+N = 1%, f = 1 kHz, R _L = 8 Ω	—	1.9	—	W
		THD+N = 10%, f = 1 kHz, R _L = 4 Ω	—	4.7	—	W
		THD+N = 1%, f = 1 kHz, R _L = 4 Ω	—	3.4	—	W
		THD+N = 10%, f = 1 kHz, R _L = 3 Ω	—	5.0	—	W
Total Harmonic Distortion + Noise	THD+N	P _O = 1 W, f = 1 kHz	—	0.1	—	%
Signal to Noise Ratio/Dynamic Range	SNR	Normal mode PWM, f = 1 kHz, A-weighted	—	95	—	dB
		Normal mode PWM, f = 1 kHz, Unweighted	—	92	—	dB
		Spread mode PWM, f = 1 kHz, A-weighted	—	90	—	dB
		Spread mode PWM, f = 1 kHz, Unweighted	—	87	—	dB
Spread Mode Common Mode PWM Carrier Peak Attenuation ²		f = 1 kHz, Relative to Normal Mode	—	24	—	dB
Common Mode AM Band Noise Notch Attenuation ³		f = 1 kHz, Measured in ±10 kHz band around selected frequency	—	35	—	dB

Notes:

1. Measured at filter output. Power measured at the chip output is greater.
2. Guaranteed by characterization.
3. Measured relative to the integrated noise floor in Spread mode. Guaranteed by characterization.
4. Does not include filter efficiency losses.

Table 5. AC Characteristics—Class D Amplifier (Continued)

($V_{DD} = 2.7$ to 3.6 V, $V_{IO} = 1.62$ to 3.6 V, $V_{PP} = 6.6$ V, $R_L = 8\ \Omega$, $VOL = 0$ dBFS, $T_A = -20$ to $+85\ ^\circ\text{C}$, unless otherwise noted.)

Power Supply Rejection Ratio	PSRR	$P_O = -3$ dBFS, $f = 1$ kHz; 200 mV _{PP} , $f_r = 400$ Hz supply ripple	—	50	—	dB
Crosstalk		$f = 1$ kHz	—	−92	—	dB
Efficiency ⁴	η	$f = 1$ kHz, half rate PWM and 10 ns slew rate	—	88	—	%
Output Pulse Repetition Frequency	PRF	Half Rate PWM	—	480	—	kHz
		Full Rate PWM	—	960	—	kHz
Notes: 1. Measured at filter output. Power measured at the chip output is greater. 2. Guaranteed by characterization. 3. Measured relative to the integrated noise floor in Spread mode. Guaranteed by characterization. 4. Does not include filter efficiency losses.						

Table 6. AC Characteristics—PWM Digital to Analog Converter

($V_{DD} = 2.7$ to 3.6 V, $V_{IO} = 1.62$ to 3.6 V, $VOL = 0$ dBFS, $T_A = -20$ to $+85\ ^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise	THD+N	$f = 1$ kHz	—	0.02	—	%
Signal to Noise Ratio/Dynamic Range	SNR	$f = 1$ kHz, A-weighted	—	88	—	dB
		$f = 1$ kHz, Unweighted	—	85	—	dB
Output Voltage Swing	V _{out}		—	1	—	V _{P-P}
Output Voltage Common Mode Bias	V _{outcm}		—	0.8	—	V
Output Load— Resistance	R _{load}	AC coupled	5	—	50	k Ω
Output Load— Capacitance	C _{load}	AC coupling capacitor	0.1	—	1	μF

Table 7. I²S Digital Audio Interface Characteristics

($V_{IO} = 1.62$ to 3.6 V, $T_A = -20$ to $+85\ ^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Input Cycle Time	t _{CYC:DCLK}		70	—	—	ns
DCLK Input Pulse Width High	t _{HI:DCLK}		0.4 x t _{CYC:DCLK}	—	0.6 x t _{CYC:DCLK}	ns
DCLK Input Pulse Width Low	t _{LO:DCLK}		0.4 x t _{CYC:DCLK}	—	0.6 x t _{CYC:DCLK}	ns
DFS Setup Time to DCLK↑	t _{SU:DCLK}		10	—	—	ns
DFS Hold Time after DCLK↑	t _{HD:DCLK}		5	—	—	ns
DOUT Output Delay	T _{PD:DCLK}		0	—	35	ns
Capacitive Loading	C _B		—	—	15	pF

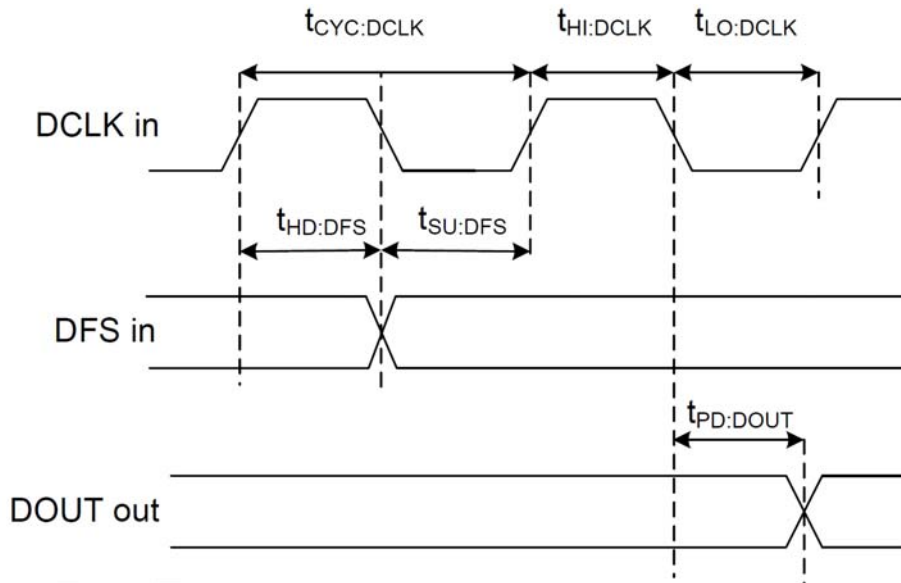


Figure 1. Digital Audio Timing Parameters

Table 8. 2-Wire Control Interface Characteristics(V_{IO} = 1.62 to 3.6 V, T_A = –20 to +85 °C, unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f _{SCL}		0	—	400	kHz
SCLK Low Time	t _{LOW}		1.3	—	—	μs
SCLK High Time	t _{HIGH}		0.6	—	—	μs
SCLK Input from SDIO Setup ↓ (START)	t _{SU:STA}		0.6	—	—	μs
SCLK Input to SDIO ↓ Hold (START)	t _{HD:STA}		0.6	—	—	μs
SDIO Input to SCLK ↑ Setup	t _{SU:DAT}		100	—	—	ns
SDIO Input to SCLK ↓ Hold	t _{HD:DAT}		0	—	900	ns
SDIO output delay	T _{PD:DAT}		300	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	t _{SU:STO}		0.6	—	—	μs
STOP to START Time	t _{BUF}		1.3	—	—	μs
SDIO Output Fall Time	t _{f:OUT}		—	—	250	ns
SDIO Input, SCLK Rise/Fall Time	t _{f:IN} t _{r:IN}		—	—	300	ns
Capacitive Loading	C _b		—	—	50	pF
Pulse Width Rejected by Input Filter	t _{SP}		—	—	50	ns

Table 9. 2-Wire Control Interface Address Selection

CLKO Startup Voltage (Pin Connection)	2-Wire Device Address
GND	1001010 (0x94)
V _{IO} (Default)	0011011 (0x36)

Table 10. Reset Timing Characteristics

(V_{IO} = 1.62 to 3.6 V, T_A = -20 to +85 °C, unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CLKO Setup Time to $\overline{\text{RST}}\uparrow$	t _{SRST}		100	—	—	μs
CLKO Hold Time after $\overline{\text{RST}}\uparrow$	T _{HRST}		30	—	—	ns

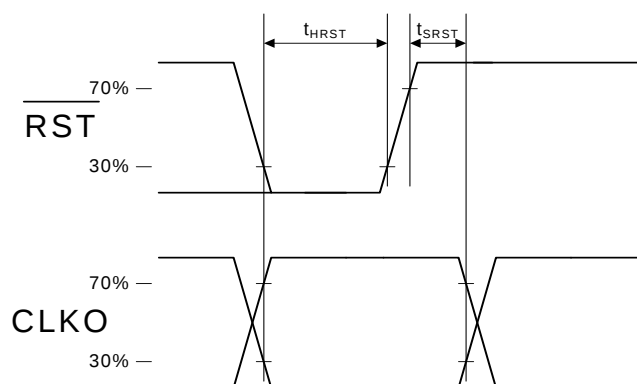


Figure 2. Reset Timing Parameters for Configuration Mode Select

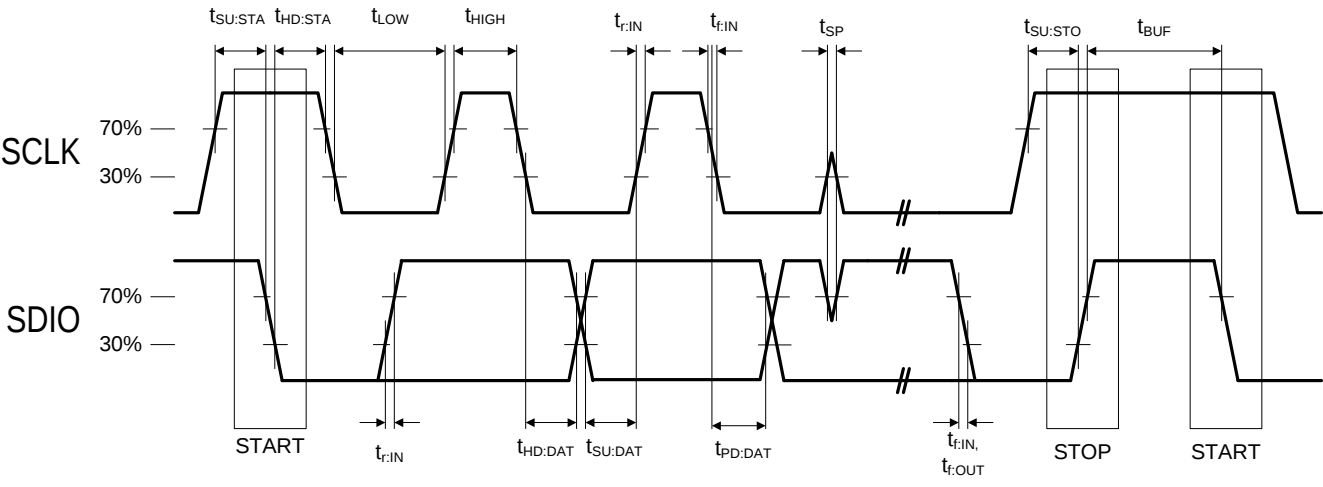


Figure 3. 2-Wire Control Interface Read and Write Timing Parameters

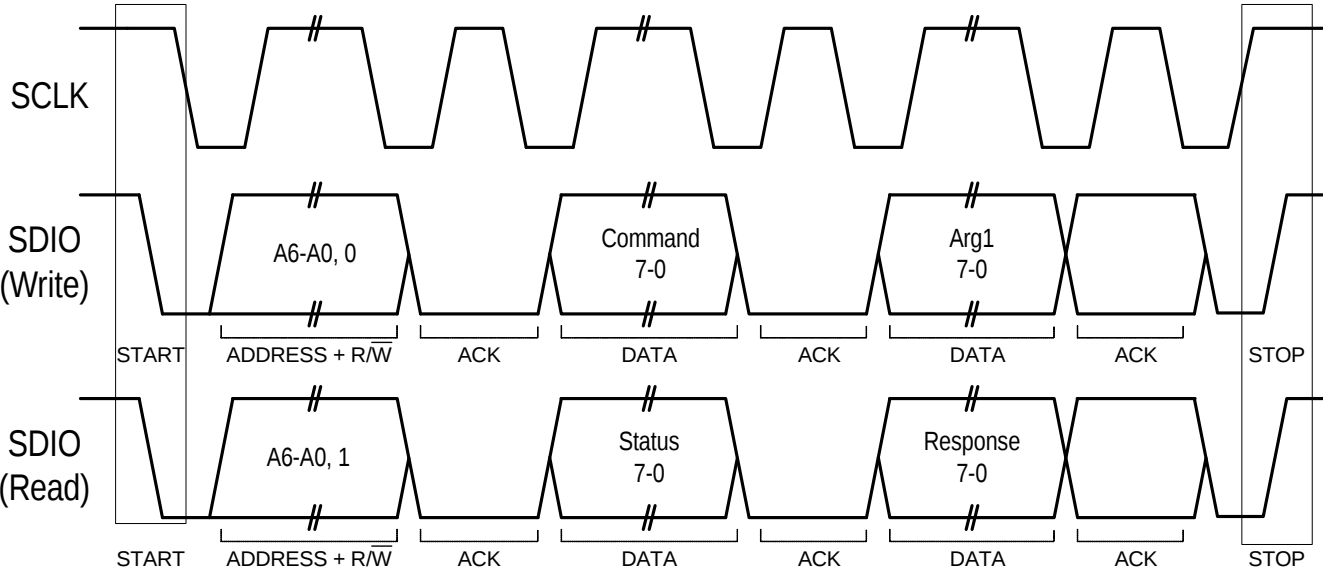


Figure 4. 2-Wire Control Interface Read and Write Timing Diagram

Table 11. Reference Clock and Crystal Characteristics(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to +85 °C, unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock, Pin XTLI						
Supported Frequencies ¹			2	—	49	MHz
Frequency Tolerance			–1000	—	1000	ppm
Jitter Tolerance ²		Integrated from 20 Hz to 1 MHz	—	—	50	psrms
High Level Input Voltage	V _{IH}		0.7xV _{IO}	—	—	V
Low Level Input Voltage	V _{IL}		—	—	0.3xV _{IO}	V
High Level Input Current	I _{IH}	V _{IN} = V _{IO} = 3.6 V	–10	—	10	μA
Low Level Input Current	I _{IL}	V _{IN} = 0 V V _{IO} = 3.6 V	–10	—	10	μA
Crystal oscillator, Pins XTLI, XTLO						
Crystal Oscillator Frequency ³			12.288	—	24.576	MHz
Crystal Frequency Tolerance			–1000	—	1000	ppm
Internal Crystal Load Capacitance			4	—	20	pF
Crystal Motion Resistance		for 24.576 MHz Crystal	—	—	100	Ω
Reference Clock Output, Pin CLKO						
Frequency Range ⁴			120	—	24576	kHz
Load Capacitance			—	—	10	pF
Notes: - Supported reference clock frequencies at XTLI include 2.048, 2.822, 3.072, 4.096, 4.234, 4.608, 5.645, 6.144, 8.192, 8.467, 9.216, 11.290, 11.2896, 12, 12.288, 16.368, 16.934, 18.432, 22.579, 24.576, 32.768, 32.869, 36.864, 45.158, and 49.152 MHz. - Required to achieve specified performance. - Supported crystal frequencies at XTLI include 12.288, 18.432, and 24.576 MHz. 120 kHz, 240 kHz, 480 kHz, 960 kHz, 1.92 MHz, 4.096 MHz, 6.144 MHz, 8.192 MHz, 12.288 MHz, 16.384 MHz, and 24.576 MHz are available at CLKO.						

2. Typical Application Schematic

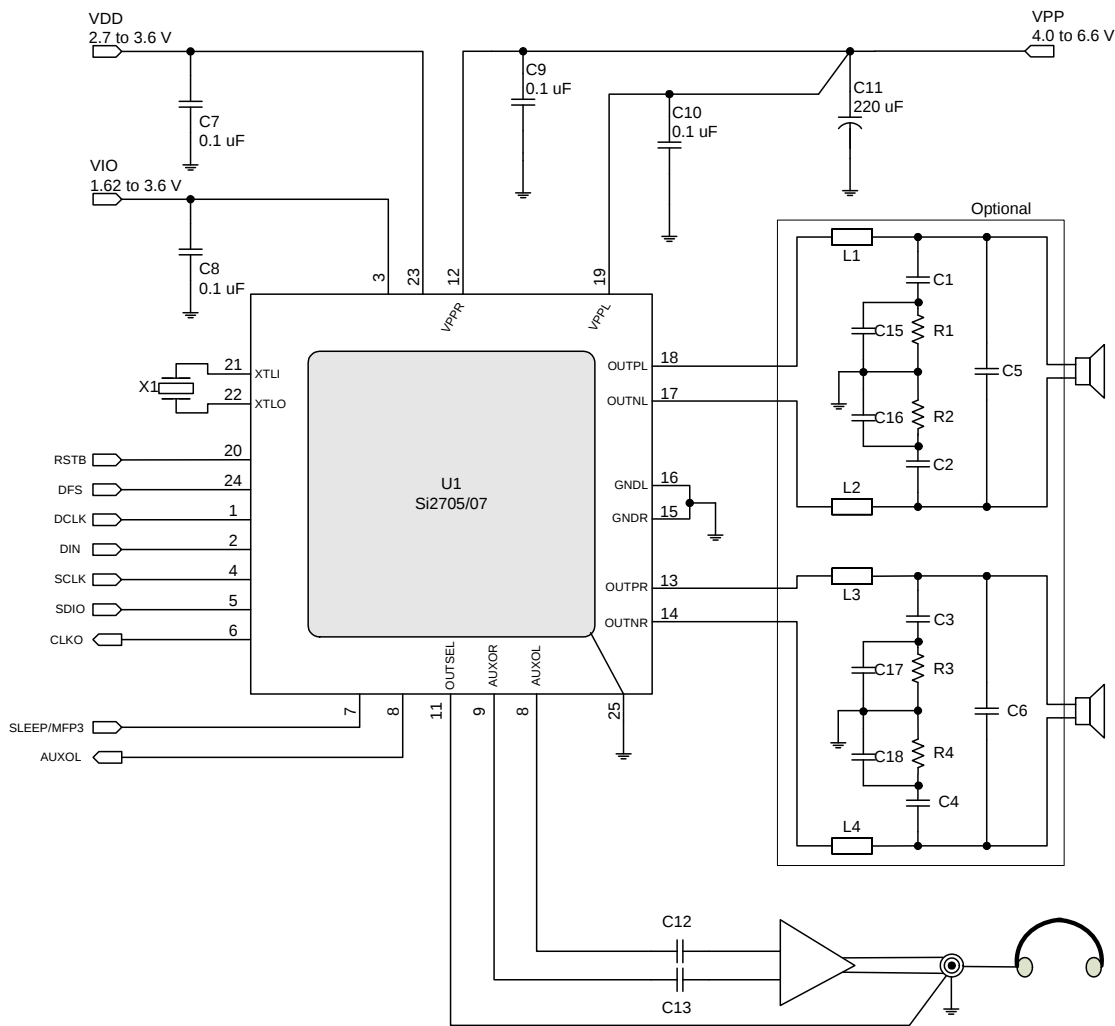


Figure 5. Typical Application Schematic

Table 12. Typical Application Schematic Bill of Materials

Component	Inductor Filter	Ferrite Bead Filter
C1, C2, C3, C4	0.68 μ F, ceramic	1000 pF, ceramic
C15, C16, C17, C18	0.33 μ F, ceramic	1000 pF, ceramic
C5, C6	0.47 μ F, Film	100 pF, ceramic
L1, L2, L3, L4	10 μ H, 1.5 A, inductor	TDK MPZ2012S601A, ferrite bead
Note: When using the ferrite bead output filter with AM radio, shielded cable is recommended.		

3. Typical System Configurations

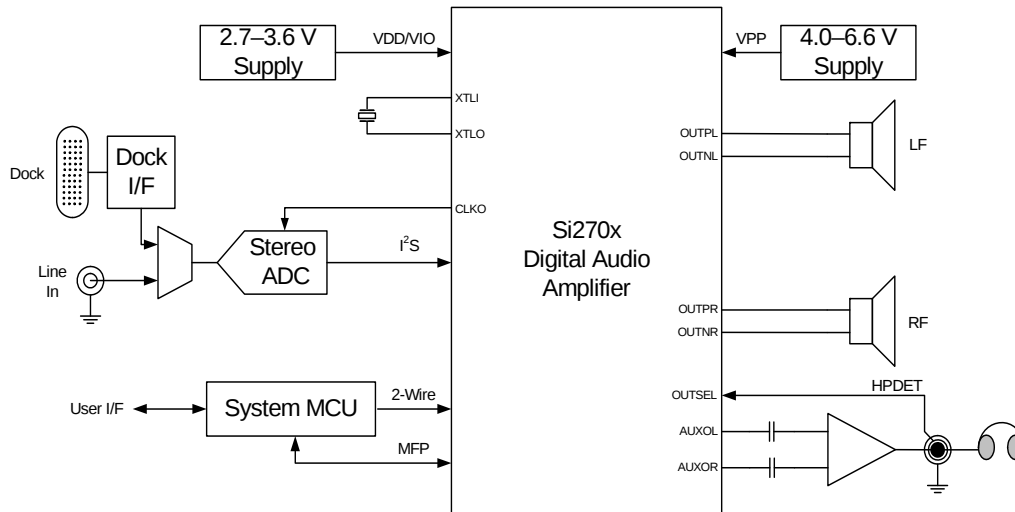


Figure 6. Basic PMP Dock System Configuration

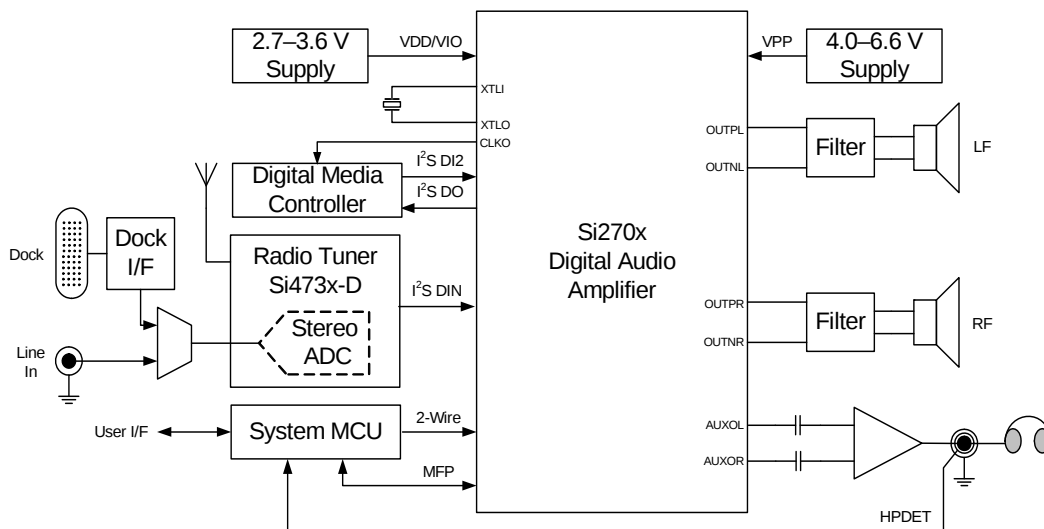


Figure 7. PMP Dock with Radio and Digital Media Controller System Configuration

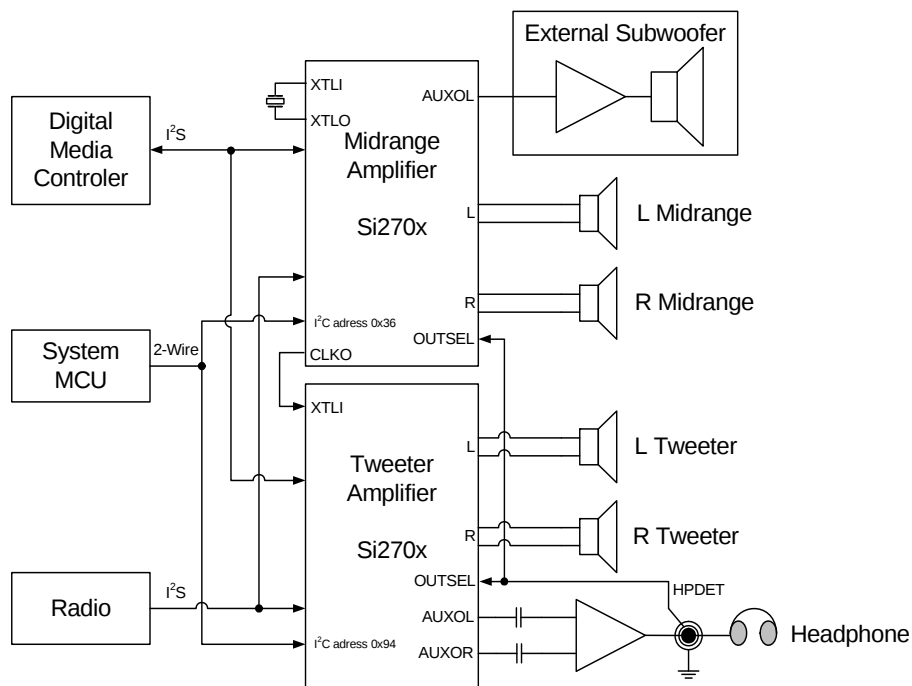


Figure 8. Stereo 2-Way Speaker System Configuration

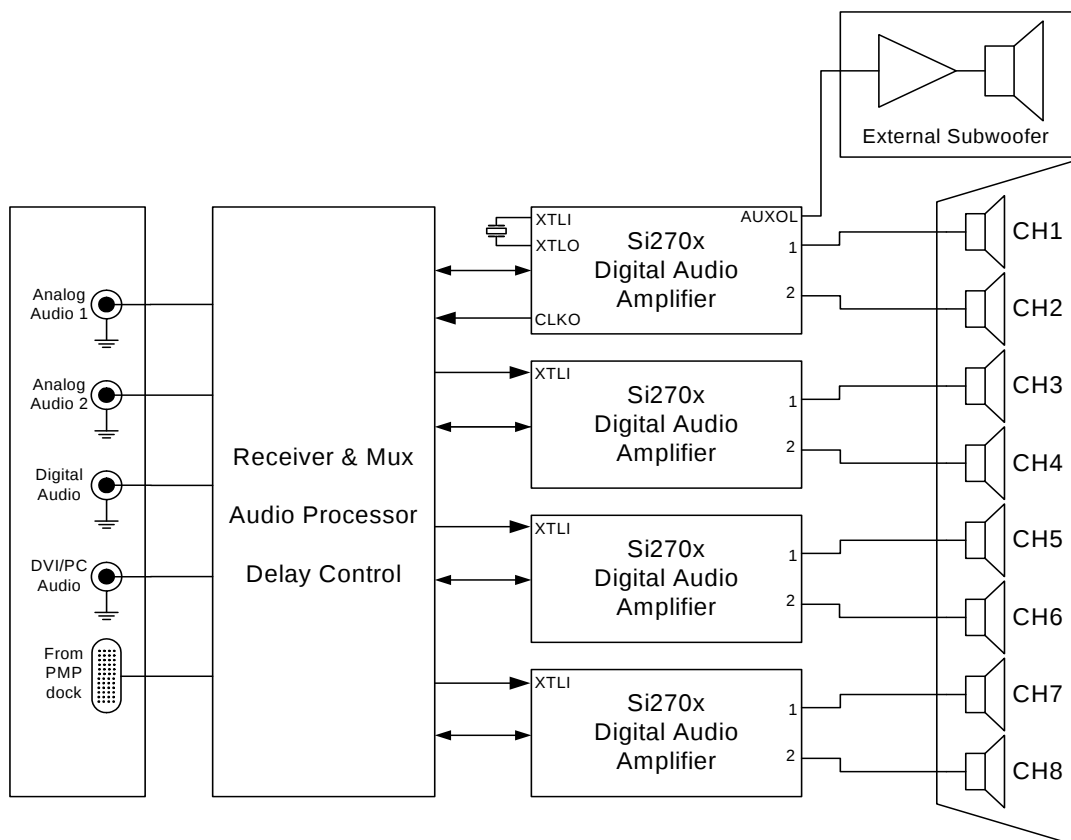


Figure 9. TV Sound Bar System Configuration

4. Functional Description

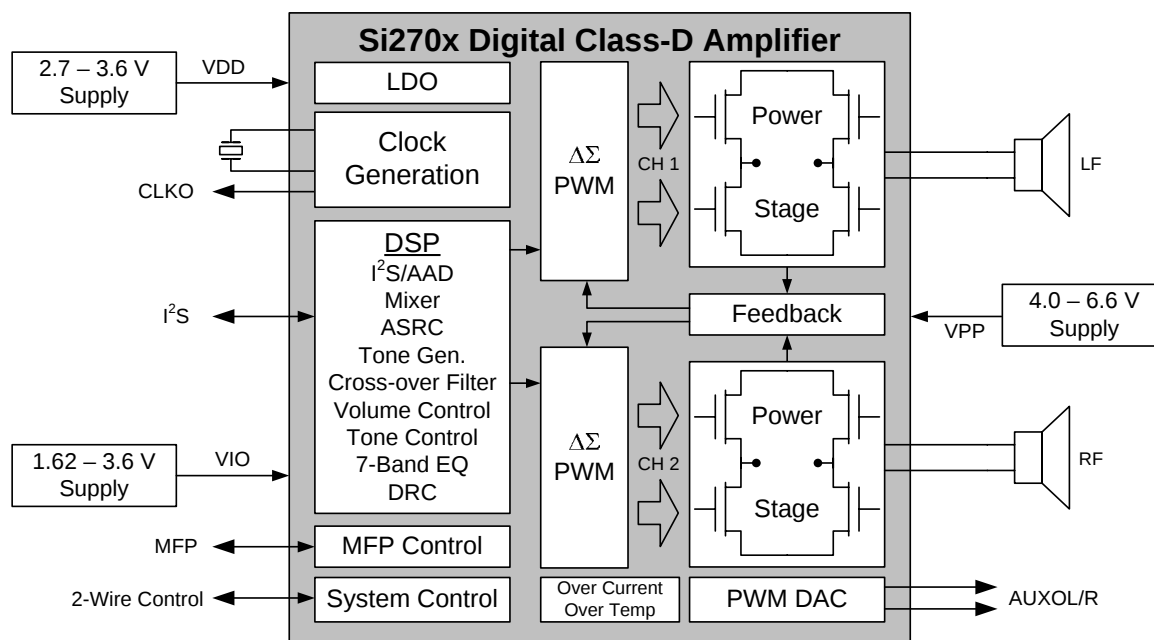


Figure 10. Functional Block Diagram

The Si2704/05/06/07 EMI mitigating 2.1 x 5 W Class D audio amplifier integrates a stereo power stage, PWM DAC, and digital signal processor (DSP) to enable simplified, low cost, power efficient system designs in consumer audio electronics. The digital input amplifier features delta-sigma PWM for high quality audio while innovative EMI mitigation technology manages PWM switching noise to suppress peak emissions more than 20 dB while providing co-existence with AM/FM radio tuners.

The power stage is capable of driving two 3 Ω bridge-tied speakers with 5 W per channel at 10% THD+N from 6.6 V power supplies. It can also drive 8 Ω bridge-tied speakers at 3 W per channel with 88% efficiency. The power stage feedback systems improve power supply rejection and harmonic distortion performance.

The Si270x connects up to three synchronous I^2S digital sources as either master or slave, two of which can be configured as input or output. The I^2S input is converted to a common sample rate for digital audio processing using an asynchronous sample rate converter (ASRC) and a digital crossbar mixer linearly combines any of the six inputs into the three audio processing channels

Integrated digital audio processing enables the amplifier to compensate for speaker and enclosure acoustic characteristics. A programmable 7-biquad parametric equalizer for each main channel allows notching out of mechanical resonances and pre-compensation of the speaker frequency response, while programmable dynamic range compression protects from overdriving speakers and increases the average output power without increasing apparent distortion. Tone control enables ± 18 dB of treble and bass boost/cut, while output volume is digitally controlled in 0.5 dB steps from -100 to $+28$ dB via the I^2C -Compliant 2-Wire interface or an analog potentiometer connected to the integrated ADC. Two independent tone generators enable mixing of multi-tone alarms and alerts into the audio channels.

The auxiliary audio processing channel (Aux Channel) with optional sub-mixing and low pass filtering generates mono line level analog audio output for driving an external active subwoofer or center speaker. The main channel L/R outputs may also be connected to the PWM DAC for driving a headphone amplifier.

A low jitter PLL generates internal system clocks referenced in master mode to an external crystal, or alternatively, in slave mode to either the I^2S data clock (DCLK) or the audio master clock (MCLK). A buffered clock (CLKO) can be output by the device to synchronously drive companion audio devices, additional amplifiers, and switching regulators.

4.1. PWM Processing

The Si270x is designed to operate using a bridge-tied-load (BTL) output configuration where both sides of the speaker are actively driven by the amplifier.

4.1.1. PWM Switching Rate Control

The output PWM switching frequency can be programmed via 2-wire control to be half rate (480 kHz) or full rate (960 kHz). The different rates can be configured by setting property PWM_FREQ.

Full Rate PWM provides better audio performance and AM radio co-existence, while Half Rate PWM provides lower switching losses and lower switching energy harmonics at high frequencies. For each configuration, the switching frequency can be offset slightly for FM band frequency planning flexibility.

4.1.2. EMI Mitigation

By nature, the switching characteristic of Class D amplifiers that provides high power efficiency also creates harmonic spurs at multiples of the PWM switching rate that can radiate as EMI. Common mode PWM switching from ground to the supply translates into a radiated pattern with large energy components at the fundamental and odd harmonics of the switching frequency. Fast pulse edge transitions and differential mode ripple currents flowing through inductor windings further contribute to radiated interference. To simplify design for EMI compliance and radio receiver co-existence, the Si270x features EMI mitigation modes for managing the PWM switching noise, including pulse edge slew rate control, common mode switching noise spectral shifting, and common mode switching noise spectral spreading/shaping.

4.1.2.1. Slew Rate Control

Output pulse edge slew rate can be programmed via 2-Wire control for 10 ns or 20 ns (property PWM_OUTPUT_SLEW_RATE). While faster transition times are favorable for higher efficiency, slower transition times are favorable for EMI attenuation.

4.1.2.2. Spectral Shifting

The frequency locations for the PWM common mode switching energy can be shifted to facilitate frequency planning. This spectral shifting is useful for example in radios to avoid radiating interference at frequencies where the radio is being tuned.

When spectral shifting is programmed for Integer Mode PWM, the common mode switching energy and harmonics are located at $F_C \times (2n-1)$ for all positive integers n , where F_C is the PWM switching frequency. Alternatively, when programmed for Fractional Mode PWM, the common mode switching energy and harmonics are shifted down in frequency by 50%, and are located at $F_C \times (2n-1)/2$.

The spectral shifting mode can be programmed dynamically by setting property PWM_CONFIG during normal operation without adversely affecting the internal audio processing or the amplified audio signal integrity.

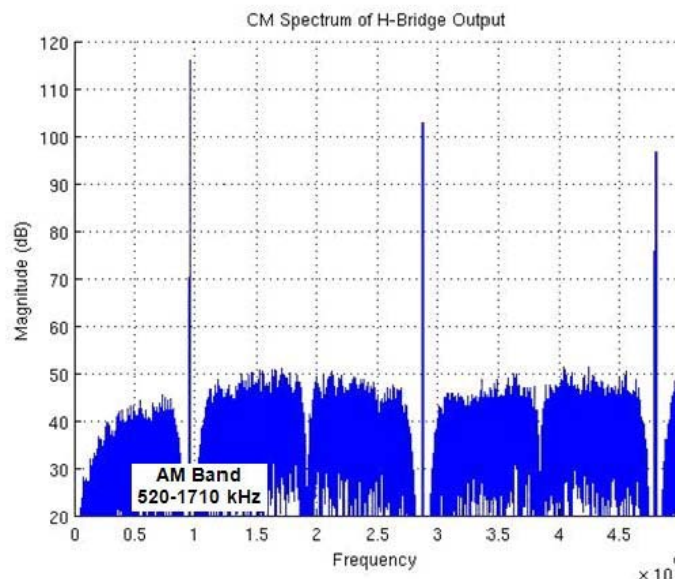


Figure 11. PWM CM Spectrum for Integer Mode PWM

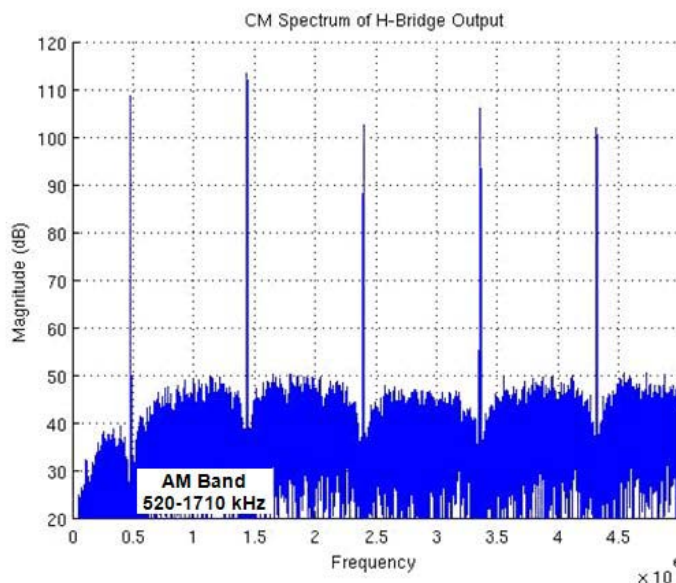


Figure 12. PWM CM Spectrum for Fractional Mode PWM

4.1.2.3. Spectral Spreading

Spread mode PWM can be used to spread PWM common mode switching energy resulting in a peak energy suppression greater than 20 dB at all frequencies. This Spectral Shaping feature is useful for mitigating EMI radiation and eliminating inductors for filter-less applications. Spread Mode PWM can be programmed dynamically by setting property PWM_CONFIG during normal operation without adversely affecting the internal audio processing or the differential output signal integrity.

4.1.2.4. Spectral Shaping Noise-Free Notch for AM Radio (Si2705/07 only)

When using Spread Mode PWM with full rate PWM switching (960 kHz), a tunable noise-free notch can be programmed via 2-Wire control to shape the switching noise and create a narrow frequency band in the AM radio spectrum in which the PWM common mode switching energy is not allowed to spread. This noise-free notch is

nominally 20 kHz wide and tunable in 5 kHz increments from 520 to 1710 kHz, virtually equalizing the noise level across the band. The noise-free notch can be dynamically tuned during normal operation without adversely affecting the internal audio processing or the differential output signal integrity.

Spread Mode PWM with the tunable noise-free notch is useful for systems in which the Si2705/07 needs to co-exist with an AM radio receiver. In normal AM radio operation, the system MCU programs the noise-free notch frequency in the Si2705/07 to the same frequency as the AM radio to inhibit PWM switching noise from interfering with radio reception. Because Spread Mode PWM is also engaged, switching noise outside of the noise-free notch band is also suppressed for mitigating broadband EMI radiation

The noise-free notch can be placed at different frequencies by programming property PWM_AM_TUNE_FREQ. More information on the complete range of programming parameters and settings available for optimized operation can be found in the “AN469: Si270x Programming Guide”.

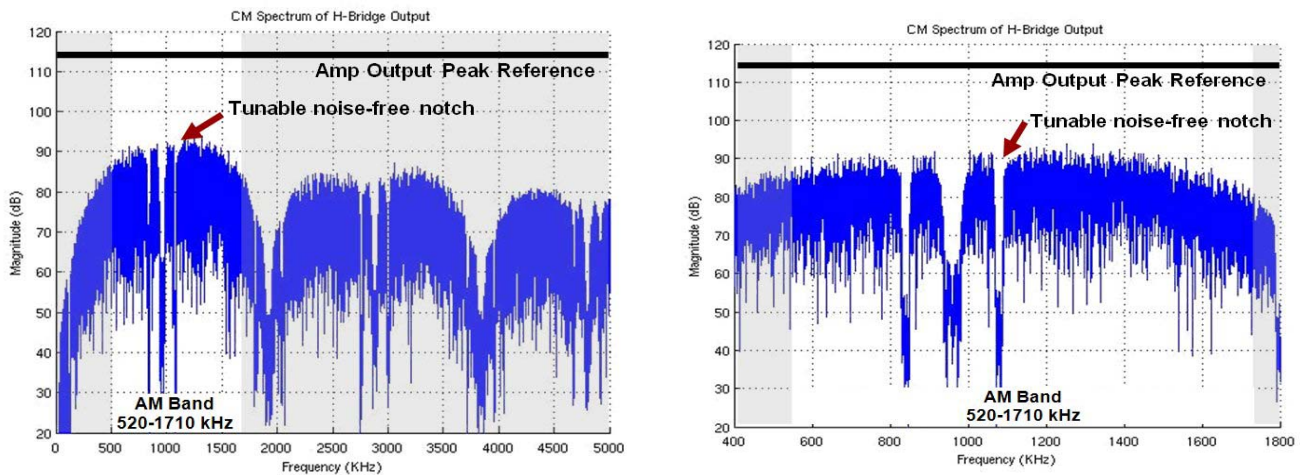


Figure 13. PWM CM Spectrum for Spread Mode PWM with Noise-Free Notch

4.2. Operating Modes

The Si2704/05/06/07 features four operating modes: one active mode (Active) and three low power modes (Standby, Sleep and Power Down). The low power modes differ on power consumption and wake up times, providing the flexibility to meet system design requirements. See Table 3, “DC Characteristics—Supplies and Interfaces,” on page 6 for additional information on startup times and power consumption.

Figure 14 illustrates the device state diagram highlighting the key operating modes and the allowed transitions.

For more information concerning operating modes and their programming requirements, refer to “AN469: Si270x Programming Guide”.

4.2.1. Active Mode

Active mode is the normal operational mode in which the chip accepts digital I²S data at the input, drives an audio output and is programmable via a 2-Wire interface bus.

Active Mode is initiated by setting the ACTIVE argument of the ACTIVATE command via the 2-Wire interface. To avoid clicks and pops in the audio output, mute is de-asserted after entering Active Mode.

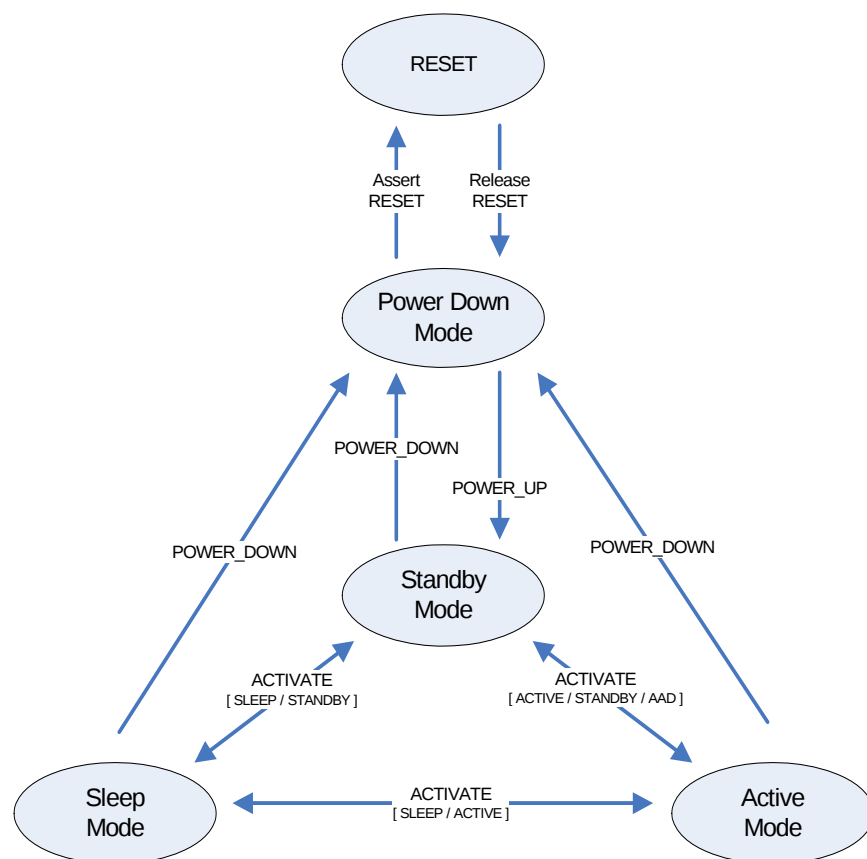


Figure 14. Operating Modes

4.2.2. Standby Mode

Standby Mode is a reduced power state where the register states are preserved and the 2-Wire interface is fully operational, allowing for new parameters and configuration settings to be programmed even though the amplifier output is powered down. This state has the shortest wake-up time relative to the other low power modes. If the buffered reference clock output (CLKO) is enabled, the timing generation circuitry remains active.

Standby Mode is initiated by setting the STANDBY argument of the ACTIVATE command via the 2-Wire interface. Standby Mode can also be initiated by setting the AAD argument of the ACTIVATE command, which additionally enables the Audio Activity Detector. See "4.5.2. Audio Activity Detector" on page 24 for additional information about this setting.

To avoid clicks and pops in the audio output, mute is first asserted before entering Standby Mode.

4.2.3. Sleep Mode

Sleep Mode is the lowest power consumption state in which the chip parameters and configurations are retained. However, chip parameter and configuration settings cannot be programmed and the buffered reference clock output (CLKO) is disabled in this mode. The time to activate the chip is shorter from the Sleep Mode than when activating from the Power Down Mode.

Sleep mode is initiated by setting the SLEEP argument of the ACTIVATE command.

4.2.4. Power Down Mode and Reset

Asserting the $\overline{\text{RST}}$ pin low disables the analog and digital circuitry, resets the registers to their default settings, and disables the 2-Wire bus. The $\overline{\text{RST}}$ pin should always be asserted low when power to the device is ramped up, and released once the power supply voltages have stabilized.

After $\overline{\text{RST}}$ is released high, the chip comes up in Power Down Mode with the registers set to their default values. The 2-Wire interface remains active but only responds to the POWER_UP command that puts the device into

Standby Mode so that the high power outputs are prevented from being enabled prior to the registers being configured. Any other command sent to the device is acknowledged on the bus but ignored by the device. This mode has the highest wake-up time and lowest power consumption of the three low power modes.

A POWER_DOWN command causes a transition to Power Down Mode, disabling the outputs and resetting all parameter registers to default values.

4.3. Chip Configuration

The Si270x can be programmed via the 2-Wire interface for several operating configurations.

4.3.1. Multi-Function Pins (MFPs)

Three multi-function pins (MFPs) support a wide range of system configurations while minimizing pin count. These MFPs are programmed via the 2-Wire interface. Table 13 outlines all available signals, and Table 14 shows the signal configuration options available on each MFP with the default in bold.

Table 13. Multi-Function Signal Definitions

Signal Name	Functional Description
OUTSEL	Tri-level output mode select
$\overline{\text{INT}}$	Interrupt flag
DIN2	I ² S data input 2
DIN3	I ² S data input 3
DOUT	I ² S data output
GPO1–3	General purpose output

The MFPs default to High-Z state. MFP1 can be programmed to be signal $\overline{\text{INT}}$ or GPO1. MFP2 can be programmed to be signal OUTSEL, DIN2, DOUT2 or GPO2. MFP3 can be programmed to be signal DIN3, DOUT or GPO3. Table 14 summarizes the MFP configuration options with the default functionality shown in bold.

Table 14. MFP Configuration Options

Pin Name	Pin Number	Signal Options
MFP1	#10 (QFN) #13 (eTQFP)	High-Z , $\overline{\text{INT}}$, GPO1
MFP2	#11 (QFN) #14 (eTQFP)	High-Z , OUTSEL, DIN2, DOUT, GPO2
MFP3	#7 (QFN) #10 (eTQFP)	High-Z , DIN3, DOUT, GPO3

The Si270x can receive digital I²S audio signal from up to three different sources with the default configuration being only one input. For cases where more than one signal input is desired or alternatively a signal output is desired, the MFPs should be programmed to an appropriate configuration with additional DINx/DOUT signals.

Three general purpose output (GPO) pins are also available. The GPOs can be programmed to output logic 1, logic 0, or a Hi-Z state. These pins can be used for example to control multiplexer switches in the application via the 2-Wire bus.

MFP pin function is established using the MFP_PIN_CFG command. Refer to the “AN469: Si270x Programming Guide” for more information on the options and settings requested for operation of the multi function pins.

4.3.2. Output Mode Configuration (Si2705/07 only)

The Si2705/07 can be programmed via 2-Wire or configured using the OUTSEL MFP to operate in three different output modes: 2.1 mode, 2.0 mode and aux out mode, with the 2.0 mode being the default. If OUTSEL is not configured as OUTSEL, these output modes can instead be programmed by setting the argument OUTSEL_MODE of the ACTIVATE command. Refer to the “AN469: Si270x Programming Guide” for more information on the options and settings requested for the different operation modes.

OUTSEL is a three-level input with decoding to configure the analog audio signal output at AUXOL/R pins as shown in Table 15.

Table 15. OUTSEL MFP Decoding

OUTSEL	Output Configuration	Description		
		H-Bridge Amplifier	Aux Channel Analog Output (mono aux out)	Main Channel Analog Output (stereo aux out)
GND	Aux Out Mode	disable	disable	enable
$V_{IO}/2$	2.0 Mode	enable	disable	disable
V_{IO}	2.1 Mode	enable	enable	disable

For stereo implementations, the 2.0 mode is selected enabling the main channel stereo power stage outputs. This is the default mode when OUTSEL is not externally driven, or when OUTSEL is driven to mid-level between V_{IO} and GND.

In 2.1 mode, with OUTSEL driven high to V_{IO} , the main channel stereo power stage is enabled to drive stereo bridge-tied loads while a PWM DAC produces mono analog audio from the auxiliary channel to drive a subwoofer or central channel analog input amplifier.

To drive an external stereo analog amplifier (e.g., for headphones) the PWM DAC can be configured to output the main stereo channel. In this case, OUTSEL is driven low to GND.

To avoid unwanted audible pop noises on the output, the Si270x implements circuitry to minimize the output transients that occur while charging and discharging the PWM DAC ac coupling capacitor (see C10 and C11 in the typical application schematic on page 13). The click and pop noise reduction circuit controls the charging and discharging currents on the capacitors to prevent sudden changes in the output bias level and the consequent glitches in the output voltage.

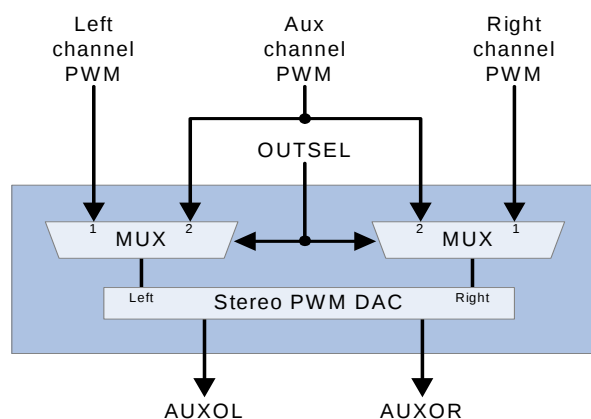


Figure 15. MUX OUTSEL Configuration

OUTSEL can be driven by a headphone plug detection circuit as shown in Figure 16. The ratio between the two resistors in the diagram configures the outputs for a 2.0 (with $R1=R2$) or a 2.1 application (with $R2 \gg R1$). In this application example, OUTSEL may be used for enabling and disabling the external amplifiers.

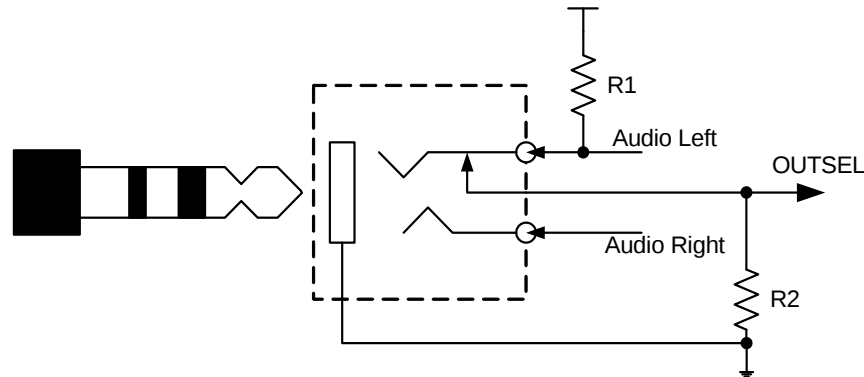


Figure 16. Headphone Plug Detection Application Schematic

4.4. Clocking

A low jitter on-chip PLL synchronizes to an external clock reference and generates all necessary internal clocks. Three options are available for the external reference: a crystal, a reference clock or the digital I²S audio bit clock. In addition, a buffered user-programmable output clock can be generated on the CLKO pin for use as a clock reference for external circuits.

4.4.1. Reference Clock Input

Using an external crystal, the on-chip crystal oscillator generates a precise, low jitter internal clock reference for the best audio performance.

For system design flexibility, the device also supports the options to use either an external reference clock or the I²S bit clock as the PLL reference. Noise performance of the amplifier is a direct function of the jitter characteristics of the external source.

The source of the external reference is programmed using the CLOCK_SOURCE property through the 2-Wire interface.

4.4.1.1. Crystal Oscillator Operation

When a crystal is connected between XTLI and XTLO pins and the chip is configured properly all the timing for the chip is derived from the on-chip crystal oscillator.

A range of crystals are supported and the device needs to be programmed to the selected frequency using the CLOCK_REF_FREQ property. The crystal oscillator provides the best audio performance.

4.4.1.2. External Reference Clock Operation

In this mode, the device operates in slave clock mode and the reference clock is provided by an external clock source on pin XTLI. A wide range of input clock frequencies are supported in this mode ranging from 2.048 to 49 MHz. Refer to Table 11 on page 12 or to the “AN469: Si270x Programming Guide” for more information on the complete range of frequencies and settings required for operation on this mode.

4.4.1.3. I²S Reference Clock Operation

The device can operate in slave clock mode using the DCLK signal from the I²S bus as a timing reference. In this mode the device needs to be programmed for one of the supported I²S clock rates and pin XTLI should be connected to ground.

4.4.2. Reference Clock Output

The Si2704/05/06/07 may provide a buffered output clock to be used as reference for external circuits when the chip is programmed for either Active or Standby mode. The clock output frequency and synchronization source is programmable.

The Si270x supports a number of reference clock frequencies that are related to the PWM switching rate. These CLKO output frequencies can be especially useful for synchronizing the amplifier to switching power supplies.

Refer to the “AN469: Si270x Programming Guide” for more information on the settings requested for operation.

4.5. Digital Audio I²S Interface

The Si270x receives digital audio data using its I²S interface. I²S inputs DIN2 and DIN3 can be configured as either an input or output while DIN is restricted to input only, and all three can be configured to operate in either master or slave mode. Only one output is supported at a time. All data ports operate synchronously from a single bit-clock and frame-clock signal. During normal operation, the crossbar mixer outputs are independently programmed to be a linear combination of any of the channels from the configured inputs with a scaling range from -1 to +1 for each channel with 8-bit precision.

4.5.1. Auto-Rate Detection

The Si270x features an auto-rate detector. It actively monitors the I²S bit and frame clock inputs during operation, detects rate changes, and makes the necessary adjustments to various clock system parameters to ensure correct operation of the amplifier.

4.5.2. Audio Activity Detector

The device has an audio activity detector (AAD) that monitors the presence of audio at the input. In normal operation, if the input audio level falls below a programmable threshold for a programmable period of time, it causes the device to enter the low power Standby Mode. When the input audio level subsequently increases above the threshold, the device returns to normal Active Mode.

4.5.3. Digital Audio Output

The Si270x provides a bypass mode that routes I²S audio input directly to the I²S output port. The output port in turn can be connected to an off-chip device such as a DAC, DSP or digital media controller.

4.5.4. Audio data formats

The digital audio interface supports 3 different audio data formats: I²S, Left-Justified and DSP Mode.

In I²S mode, the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high. Figure 17 shows a diagram for the I²S digital audio format.

In Left-Justified mode, the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low. Figure 18 shows a diagram for the Left-Justified digital audio format.

In DSP mode, the DFS becomes a pulse, one DCLK period wide. The left channel is transferred first, followed immediately by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge. Figure 19 shows a diagram for the DSP digital audio format.

In all audio formats, depending on the word size, DCLK frequency and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In this event, for power saving, in I²S slave mode DCLK sent to the Si270x can be programmed to remain low until the next DFS transition appears.

The device supports both rising edge and falling edge DCLK. The number of audio bits in each audio sample defaults to 24 bits and can be configured to 16, 20, 24 or 32 bits. The leading edge and the data format are selected using the DIGITAL_AUDIO_CONFIG property.

4.5.5. I²S Master Mode

In master mode, the Si270x is configured for 32-bit word per audio sample, rising edge DCLK, and I²S mode data format.

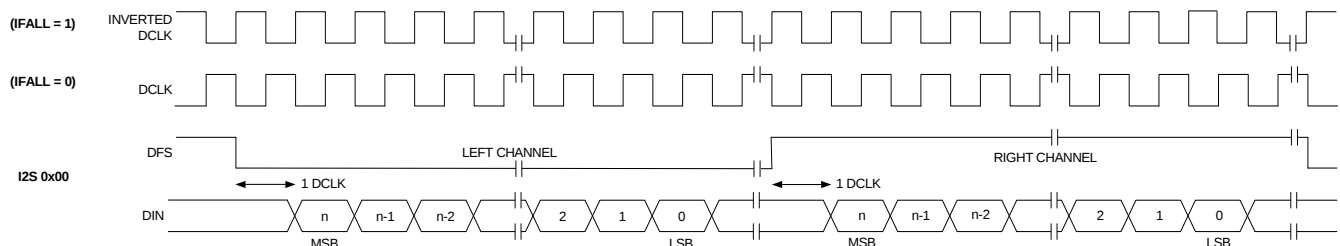


Figure 17. I²S Digital Audio Format

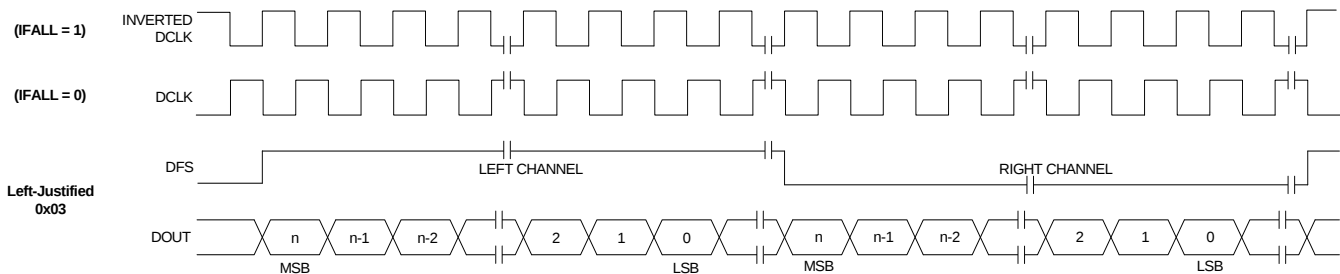


Figure 18. Left-Justified Digital Audio Format

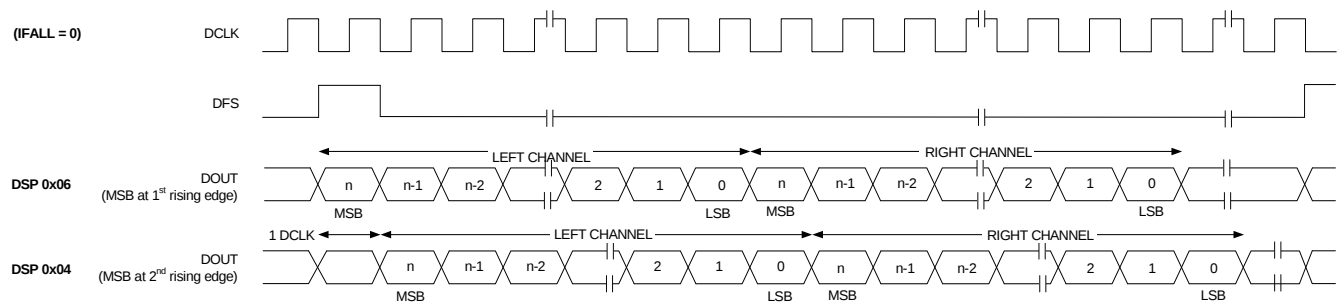


Figure 19. DSP Digital Audio Format

4.6. Digital Audio Processing (DAP)

The Si270x implements programmable digital audio processing which features volume control, dynamic range compressor (DRC), and audio filtering such as tone control, parametric equalization, crossover, and de-emphasis. The three channel digital audio processing chain for the Si2707 is shown in Figure 20.

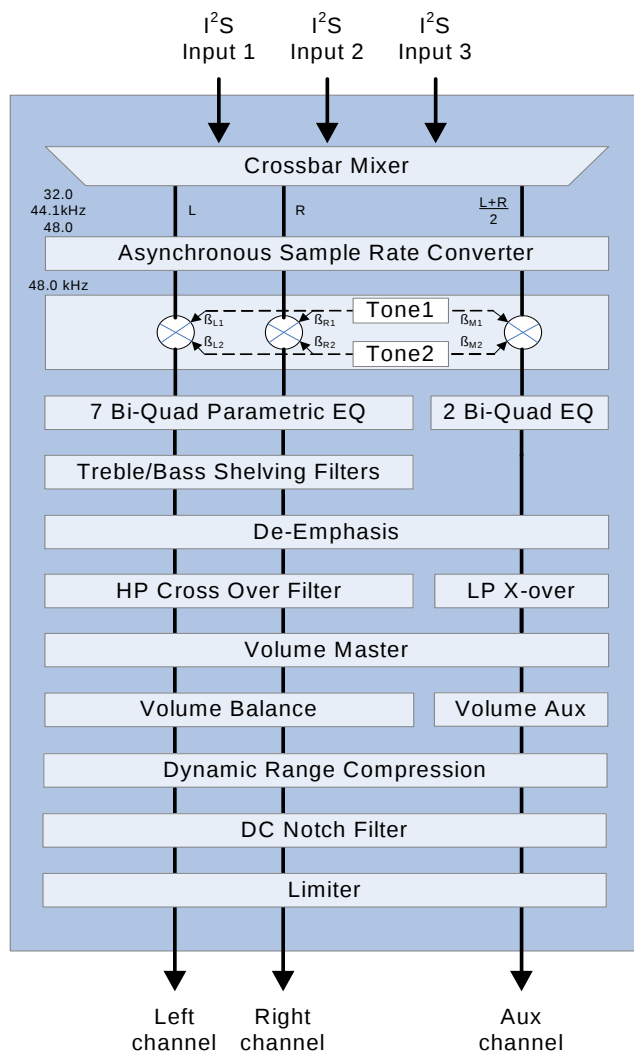


Figure 20. Signal Processing Chain

As outlined in "4.5. Digital Audio I²S Interface " on page 24, the crossbar mixer combines the selected audio sources and outputs the corresponding Left and Right main channels and an Aux Channel containing any linear combination of the inputs. The Aux Channel can either be disabled completely, configured as a mono low pass subwoofer channel, or as a mono full bandwidth center channel according to system requirement.

To make all downstream audio processing independent of the input I²S clock frequencies, an asynchronous sample rate converter (ASRC) normalizes the input rate to 48 kHz.

Refer to the "AN469: Si270x Programming Guide" for more information on the complete range of programming parameters and settings requested for operation of the digital audio processing features.

4.6.1. Parametric Equalization (Si2706/07 only)

The Si2706/07 includes 16 fully programmable parametric equalizer filters. Seven of these filters are implemented in each of the Left/Right main channels and the remaining two are used for the Aux Channel. The filters are implemented using a biquad form and can be programmed to shape the frequency response of each channel independently. The filters implement the configuration presented on Figure 21 which can be represented by the following equation:

$$y[n]=b_0x[n]+b_1x[n-1]+b_2x[n-2]+a_1y[n-1]+a_2y[n-2];$$

Where $x[n]$ is the input sample and $y[n]$ is the output sample.

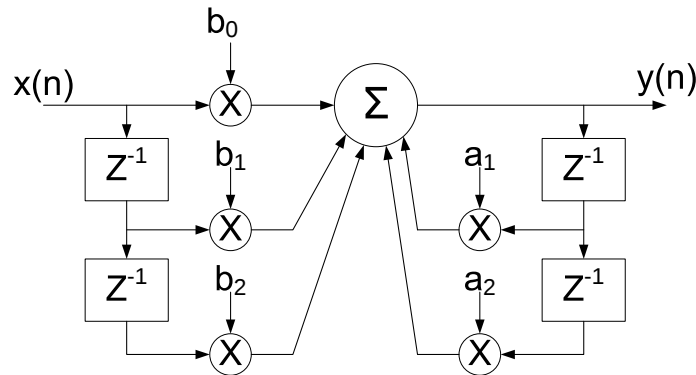


Figure 21. Biquad Filter Configuration

The five coefficients for each biquad are programmed via the 2-Wire interface by using the command SET_EQ_BIQUAD_FILTER_COEFF.

4.6.2. Tone Control

The Si270x implements tone control in the form of two second order shelving filters for bass and treble. Each filter has programmable cut-off frequency and boost/cut gain. Cut-off frequency can be adjusted from 5 to 20 kHz by setting properties BASS_CORNER_FREQ (for bass) and TREBLE_CORNER_FREQ (for treble). Gain can be adjusted from -18 to +18 dB in 1 dB steps by setting properties BASS_BOOST_CUT (for bass) and TREBLE_BOOST_CUT (for treble). Figure 22 shows the characteristics of the bass and treble shelving filters.

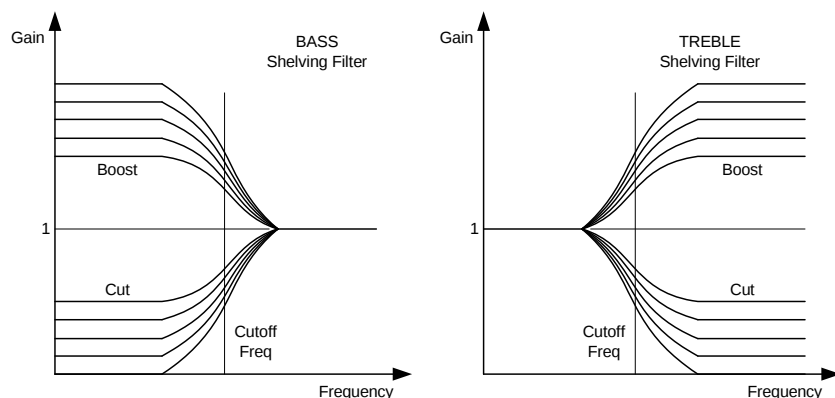


Figure 22. Generic Bass/Treble Shelving Filter Characteristics

4.6.3. De-Emphasis (Si2706/07 only)

The Si2706/07 features a de-emphasis filtering option in order to be able to process recorded audio that for noise reasons has been subject to 50/15 μ s pre-emphasis. The 50/15 μ s filter implemented has corner frequencies at 3.183 kHz and 10.610 kHz.

4.6.4. Crossover Filter (Si2706/07 only)

The Si2706/07 features a programmable frequency 12 dB/octave Linkwitz-Riley type crossover filter that provides separation of the low and high frequency content of the audio signal. The filter high-pass output is used to drive the Left/Right main channel and the low-pass output feeds the Aux Channel to be used in 2.1 Mode with an external subwoofer power driver. The cutoff frequency can be programmed from 80 to 320 Hz in 40 Hz steps via the 2-Wire interface by setting the CROSSOVER_FREQ property. The same property can also be used to disable and bypass the crossover filter.

4.6.5. Digital Volume Controls

The volume control maintains a master volume for all the channels, including the Left/Right main channels and the Aux Channel. The channel volume can be set in 0.5 dB gain/attenuation steps ranging from –100 dB (mute level) to +28 dB using the VOLUME_MASTER property.

To prevent audible artifacts due to volume transitions, the slope of the change in volume can be programmed by configuring the VOLUME_RAMP property. The default configuration is 0.1 dB/ms (dB per millisecond) and programming can be done in 0.1 dB/ms steps and ranging from 0.1 to 6.3 dB/ms.

The device also provides balance control between the Left and Right channels through the use of the VOLUME_BALANCE property. This property specifies the audio gain/attenuation division in terms of percent split between the two channels.

The Aux Channel volume control specifies the percentage of gain/attenuation levels relative to the master volume using the VOLUME_AUX_CHANNEL property.

Mute is implemented using the VOLUME_MUTE. Un-muting returns the volume setting to the value stored in the volume registers at the programmed volume transition slope rate. During the mute condition, the PWM outputs switch at a 50% duty cycle.

4.6.6. Dynamic Range Compression (Si2706/07 only)

The Si2706/07 features dynamic range compression (DRC) with programmable linear gain, compression threshold, compression ratio, look ahead time, attack rate, and release rate.

DRC increases the net output power without clipping by decreasing the peak amplitudes of audio signals and increasing the rms content of the lower amplitude signal. Audio signals below the threshold are increased by the linear gain and audio signals above the threshold are compressed by a pre-defined compression ratio.

Figure 23 shows a plot of dynamic range compression audio processing with the DRC_THRESHOLD parameter set at -40 dBFS, DRC_GAIN parameter at $+20$ dB relative to an uncompressed transfer function and DRC_SLOPE set for a 2:1 compression ratio. For input signals below the compression threshold of -40 dBFS, the output signal is increased by 20 dB relative to the input signal. For input signals above the compression threshold the input signal is increased by 1 dB for every 2 dB increase in audio input level.

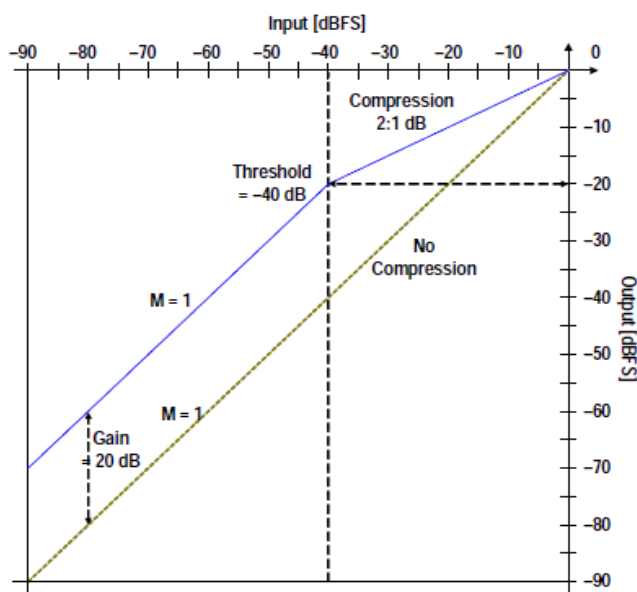


Figure 23. Dynamic Range Compression Example

In this example, the input dynamic range of 90 dB is reduced to an output dynamic range of 70 dB.

Figure 24 shows the time domain response of the dynamic range compression. The DRC_ATTACK_TIME parameter sets how quickly the gain compression responds to changes in the input level, and the DRC_RELEASE_TIME parameter sets how quickly the gain compression returns to linear gain once the audio input level drops below the compression threshold.

DRC_LOOKAHEAD_TIME allows setting the look ahead time that permits the DRC circuit to adjust the compression to sudden level changes thus preventing the clipping of the fast changing signal. Refer to “AN503: Si270x Class-D Amplifier—Dynamic Range Compressor Use” for additional information.

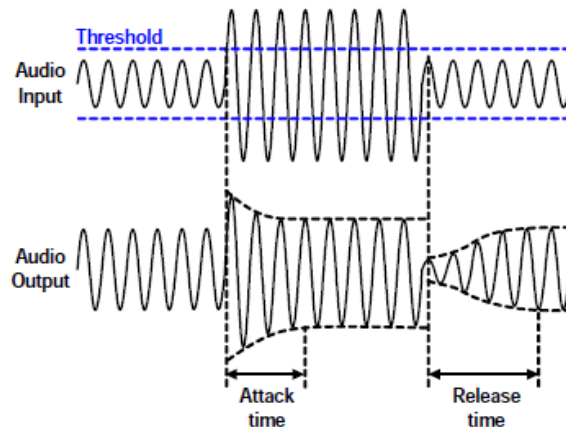


Figure 24. Time Domain Characteristics of the Audio Dynamic Range Controller

4.6.7. Hard Signal Limiter

The device implements a hard limiter to avoid exceeding the maximum modulation rate of the amplifier. The hard limiter is always enabled.

4.6.8. DC Notch Filter

A dc notch filter with a 5 Hz corner frequency is implemented as the final function in the signal processing chain to remove any dc component from the output signal. Each channel has a separate dc notch filter.

4.6.9. Tone and Alert Generation

The Si270x includes two independent tone generators with programmable frequencies and on/off times.

The output of both tone generators is fed to a mixer which combines the tones with the I²S inputs. The tones' amplitudes can be adjusted by programming the mixer coefficients using the SET_AUDIO_INPUT_MIXER command.

This feature allows customization of audible alarms and alerts. Programmable frequencies range from 100 Hz to 20 kHz in 100 Hz steps and on/off times range from 0 to 65 seconds in 1 ms steps and are set via the 2-Wire interface using the properties TONE_ONE_FREQ, TONE_ONE_ON_TIME, TONE_ONE_OFF_TIME, and TONE_ONE_AMPLITUDE for the first tone and TONE_TWO_FREQ, TONE_TWO_ON_TIME, TONE_TWO_OFF_TIME, and TONE_TWO_AMPLITUDE for the second tone.

4.7. Fault Detection and Response

To help protect the H-bridge driver and external loads, the output stage has fault detection circuitry that allows the device to respond to over-current and over-temperature events.

The over-temperature circuitry monitors the temperature of the device and if the temperature exceeds 135 °C a thermal error is issued, and the output stage is shut down by transitioning the device to Standby Mode.

The over-current protection circuit constantly monitors the current of the output stage and triggers a fault alarm if an over-current condition is detected from three different events: a short circuit across the speaker terminals, a short circuit of any of the outputs to ground and a short circuit of any of the outputs to the supply voltage. In each case, the detector issues a fault if the 2.5 A current threshold is exceeded. In response to this fault the device power stage is shut down by transitioning the device to Standby Mode.

4.8. Power Supply and Grounding Considerations

Careful attention should be given to the power and ground routing to allow for optimal performance of the Si270x.

The low voltage supplies, V_{DD} and V_{IO} , should be decoupled with 0.1 μ F capacitors soldered as close to the device as possible so that parasitic inductances are minimized. For the power stage supplies V_{PPL} and V_{PPR} , each should be bypassed with a 0.1 μ F in ceramic capacitor, located as close to the device as possible, in parallel with a 220 μ F electrolytic capacitor. This allows for optimal filtering in the full frequency spectrum. For detailed information on board layout considerations and examples refer to “AN470: Si270x Layout Guidelines.”

4.9. Control Interface

An I²C-compatible 2-Wire serial port slave interface allows an external controller to send commands, configure properties, and receive responses from the Si270x. Commands may only be sent after V_{IO} and V_{DD} supplies are applied and the RST pin has been released high.

The CLK0 pin serves as a configuration boot-strap to select one of two unique addresses to which the Si270x responds. During reset, if CLK0 is pulled low using a 2.2 k Ω resistor connected to ground, then the 7 bit device address is 1001010 (0x94). If CLK0 is left floating, a 22 k Ω internal pull-up within the Si270x causes the 2-Wire to select a device address of 0011011 (0x36).

A 2-wire transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the 2-wire master drives an 8-bit control word serially on SDIO which is captured by the device on rising edges of SCLK. The control word consists of a 7 bit device address followed by a read/write bit (read = 1, write = 0). If the address matches, the Si270x acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

For write operations, the 2-Wire master sends an eight bit data byte on SDIO following the control word, which is captured by the device on rising edges of SCLK. The Si270x acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The 2-Wire master may write up to eight data bytes during a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si270x has acknowledged the control byte, it drives a data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The 2-wire master acknowledges each data byte by driving SDIO low for one cycle on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction ends. The 2-wire master may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si270x. A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high. For details on timing specifications and diagrams, refer to Table 8 on page 9, Figure 3 on page 11, and Figure 4 on page 11.

4.10. Programming with Commands

The Si270x provides a simple yet powerful software interface to program configuration and parameter settings. The device is programmed using commands, arguments, properties, and responses. To perform an action, the user writes a command byte and associated arguments causing the chip to execute the given command. Commands control actions, such as powering up the device, shutting down the device, or configure the audio input source. Arguments are specific to a given command and are used to modify the command. For example, for the SET_AUDIO_INPUT_MIXER command, arguments are required to set the coefficients of the linear combination of the sources. Properties are a special command argument used to modify the default chip operation and are generally configured immediately after power up. Examples of properties include CLOCK_SOURCE and DEEMPHASIS. A complete list of commands and properties is available in “5. Commands and Properties”. Responses provide the user information and are returned after a command and associated arguments are sent. At a minimum, all commands respond with a one-byte status reply indicating interrupt and clear-to-send status information. Subsequent sections of this data sheet mention many of the commands and properties that are used to alter different functions. More information on the complete list of programming modes of operation and properties can be found in the “AN469: Si270x Programming Guide.”

5. Commands and Properties

Table 16 and Table 17 are the summary of commands and properties for the Si270x Class D Audio Amplifier device.

Table 16. Class D Audio Amplifier Command Summary

Common Commands		
Number	Name	Summary
0x01	POWER_UP	Power-up the device.
0x10	FUNC_INFO	Returns the Function revision information of the device.
0x12	SET_PROPERTY	Set the value of a property.
0x13	GET_PROPERTY	Retrieve a property's value.
0x14	MFP_PIN_CFG	Configure MFP pins.
0x15	SET_AUDIO_INPUT_MIXER	Configure Audio input source.
0x16	OUTSEL	Select amplifier outputs.
0x21	SET_EQ_BIQUAD_FILTER_COEFF	Set Biquad Filter.
0x22	GET_INT_STATUS	Read interrupt status bit.
0x23	GET_FAULT_STATUS	Get the source of the fault condition.
0x24	GET_AUDIO_STATUS	Read back audio parameters.
0x31	ACTIVATE	Enable or disable audio processing & amplifier output operations.
0x32	POWER_DOWN	Power-down the device.

Table 17. Class D Audio Amplifier Property Summary

Category	Number	Name	Summary
Interrupt	0x0001	INT_ENABLE	Configure Interrupt Source.
Clock	0x0101	REF_CLOCK_SOURCE	Select the reference source for PLL.
	0x0102	REF_CLOCK_FREQ	Set the reference clock freq for the PLL in kHz units.
	0x0103	CLOCK_OUT_FREQ	Configure output clock frequency.
I2S	0x0104	DIGITAL_AUDIO_SAMPLE_RATE	Set the digital audio sampling rate.
	0x0201	DIGITAL_AUDIO_CONFIG	Sets the Digital Audio Input Format Configuration.
AAD	0x0301	AAD_CONFIG	Set Audio Activity Detector (AAD) Configuration.
	0x0302	AAD_THRESHOLD	Set audio level threshold where the device will go into standby if the audio input level falls below this threshold.
	0x0303	AAD_DURATION	Set how long the signal has been below the threshold in ms before going to standby state.

Table 17. Class D Audio Amplifier Property Summary (Continued)

Category	Number	Name	Summary
Biquad Filter	0x1901	CROSSOVER_FREQ	Set crossover freq between Main Channel and Aux Channel.
	0x2103	BASS_BOOST_CUT	Set bass shelving filter boost/cut for the Left and Right Channel.
	0x2104	BASS_CORNER_FREQ	Set bass shelving filter corner freq for the Left and Right Channel.
	0x2105	TREBLE_BOOST_CUT	Set treble shelving filter boost/cut for the Left and Right Channel.
	0x2106	TREBLE_CORNER_FREQ	Set treble shelving filter corner freq for the Left and Right Channel.
Volume	0x2201	VOLUME_MUTE	Mute speaker output.
	0x2202	VOLUME_MASTER	Set Master Volume.
	0x2203	VOLUME_BALANCE	Set L and R Volume Balance from 0% to 100%.
	0x2204	VOLUME_AUX_CHANNEL	Set Aux Channel Volume.
	0x2205	VOLUME_RAMP	Set volume transition slope.
DRC	0x2301	DRC_CONFIG	Configure DRC.
	0x2302	DRC_THRESHOLD	Set DRC threshold.
	0x2303	DRC_SLOPE	Set the DRC slope. DRC slope is the inverse of DRC compression ratio.
	0x2304	DRC_GAIN	Set DRC gain.
	0x2305	DRC_ATTACK_TIME	Set DRC attack time constant in ms units.
	0x2306	DRC_RELEASE_TIME	Set DRC release time constant in ms units.
	0x2307	DRC_LOOKAHEAD_SAMPLES	Sets the number of look-ahead samples.
PWM	0x2701	PWM_CONFIG	Set PWM Output Mode and Max Modulation Index.
	0x2702	PWM_FREQ	Set PWM Freq in kHz units.
	0x2703	PWM_AM_TUNE_FREQ	Set where the currently AM Tune Freq is to put the notch when EMI mitigation mode is used.
	0x2704	PWM_MAX_MODULATION_INDEX	Set PWM maximum modulation index.
	0x2705	PWM_OUTPUT_SLEW_RATE	Set output stage slew rate.
Programmable Tone	0x2901	TONE_ONE_AMPLITUDE	Set programmable tone generator amplitude.
	0x2902	TONE_ONE_FREQ	Set programmable tone generator frequency.
	0x2903	TONE_ONE_ON_TIME	Set programmable tone generator ON Time in ms.
	0x2904	TONE_ONE_OFF_TIME	Set programmable tone generator OFF Time in ms.
	0x2905	TONE_TWO_AMPLITUDE	Set programmable tone generator amplitude.
	0x2906	TONE_TWO_FREQ	Set programmable tone generator frequency.
	0x2907	TONE_TWO_ON_TIME	Set programmable tone generator ON Time in ms.
	0x2908	TONE_TWO_OFF_TIME	Set programmable tone generator OFF Time in ms.

6. Pin Descriptions

6.1. 24-Pin QFN Package

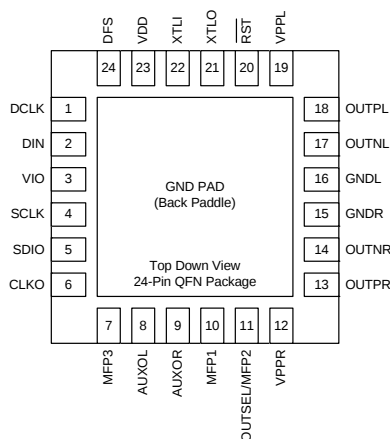


Figure 25. Pin Configuration

Table 18. Pin Descriptions

Pin Number	Name	Function
GND PAD	GND	Low voltage ground for VDD. Connect to PCB ground plane.
1	DCLK	I ² S digital I/O data clock.
2	DIN	I ² S digital data input port.
3	VIO	I/O supply voltage.
4	SCLK	Serial clock input for I ² C-compliant 2-Wire control interface.
5	SDIO	Serial data input/output for I ² C-compliant 2-Wire control interface.
6	CLKO	Buffered reference clock output. Configures 2-Wire address on $\overline{\text{RST}}$.
7	MFP3	Multi-function pin 3.
8	AUXOL	PWMDAC left channel analog output on Si2705/07 (Reserved on Si2704/06).
9	AUXOR	PWMDAC right channel analog output on Si2705/07 (Reserved on Si2704/06).
10	MFP1	Multi-function pin 1.
11	OUTSEL/MFP2	Output select three-level control input: 2.0, 2.1 or line out mode.
12	VPPR	Right channel power stage supply voltage.
13	OUTPR	Right channel power stage “P” output.
14	OUTNR	Right channel power stage “N” output.
15	GNDR	Right channel power stage ground.
16	GNDL	Left channel power stage ground.
17	OUTNL	Left channel power stage “N” output.
18	OUTPL	Left channel power stage “P” output.
19	VPPL	Left channel power stage supply voltage.
20	$\overline{\text{RST}}$	Device reset (active low) input.
21	XTLO	External crystal output.
22	XTLI	Reference clock or external crystal input.
23	VDD	Low voltage supply voltage.
24	DFS	I ² S digital I/O data frame synch.

6.2. 48-Pin eTQFP Package

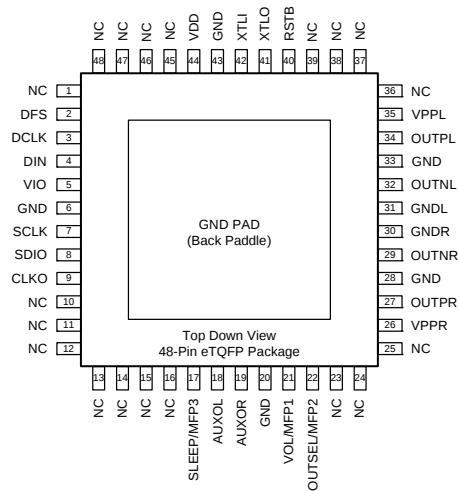


Figure 26. Pin Configuration

Table 19. Pin Descriptions

Pin Number	Name	Function
1, 10, 11, 12, 13, 14, 15, 16, 23, 24, 25, 36, 37, 38, 39, 45, 46, 47, 48	NC	No connect. Connect to PCB ground plane.
2	DFS	I ² S digital I/O data frame synch.
3	DCLK	I ² S digital I/O data clock.
4	DIN	I ² S digital data input port.
5	VIO	I/O supply voltage.
6, 20, 28, 33, 43	GND	Ground. Connect to PCB ground plane.
7	SCLK	Serial clock input for I ² C-compliant 2-Wire control interface.
8	SDIO	Serial data input/output for I ² C-compliant 2-Wire control interface.
9	CLKO	Buffered reference clock output. Configures 2-Wire address on $\overline{\text{RST}}$.
17	MFP3	Multi-function pin 3.
18	AUXOL	PWMDAC left channel analog output on Si2705/07 (Reserved on Si2704/06).
19	AUXOR	PWMDAC right channel analog output on Si2705/07 (Reserved on Si2704/06).
21	MFP1	Multi-function pin 1.
22	OUTSEL/MFP2	Output select three-level control input: 2.0, 2.1 or line out mode.
26	VPPR	Right channel power stage supply voltage.
27	OUTPR	Right channel power stage “P” output.

Table 19. Pin Descriptions (Continued)

Pin Number	Name	Function
29	OUTNR	Right channel power stage “N” output.
30	GNDR	Right channel power stage ground.
31	GNDL	Left channel power stage ground.
32	OUTNL	Left channel power stage “N” output.
34	OUTPL	Left channel power stage “P” output.
35	VPPL	Left channel power stage supply voltage.
40	$\overline{\text{RST}}$	Device reset (active low) input.
41	XTLO	External crystal output.
42	XTLI	Reference clock or external crystal input.
44	VDD	Low voltage supply voltage.

7. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si2704-A10-GM	2.0 EMI Mitigating Class D Power Amplifier	4x4 QFN Pb-Free	–20 to 85 °C
Si2704-A10-GQ	2.0 EMI Mitigating Class D Power Amplifier	7x7 eTQFP Pb-Free	–20 to 85 °C
Si2705-A10-GM	2.1 EMI Mitigating Class D Power Amplifier with tunable noise notch for AM radio	4x4 QFN Pb-Free	–20 to 85 °C
Si2705-A10-GQ	2.1 EMI Mitigating Class D Power Amplifier with tunable noise notch for AM radio	7x7 eTQFP Pb-Free	–20 to 85 °C
Si2706-A10-GM	2.0 EMI Mitigating Class D Power Amplifier with EQ/DRC	4x4 QFN Pb-Free	–20 to 85 °C
Si2706-A10-GQ	2.0 EMI Mitigating Class D Power Amplifier with EQ/DRC	7x7 eTQFP Pb-Free	–20 to 85 °C
Si2707-A10-GM	2.1 EMI Mitigating Class D Power Amplifier with tunable noise notch for AM radio with EQ/DRC	4x4 QFN Pb-Free	–20 to 85 °C
Si2707-A10-GQ	2.1 EMI Mitigating Class D Power Amplifier with tunable noise notch for AM radio with EQ/DRC	7x7 eTQFP Pb-Free	–20 to 85 °C
*Note: Add an “R” at the end of the device part number to denote tape and reel option.			

8. Package Outline

8.1. 24-Pin QFN Package

Figure 27 illustrates the package details for 24-pin QFN package option for the Si2704/05/06/07. Table 20 lists the values for the dimensions shown in the illustration.

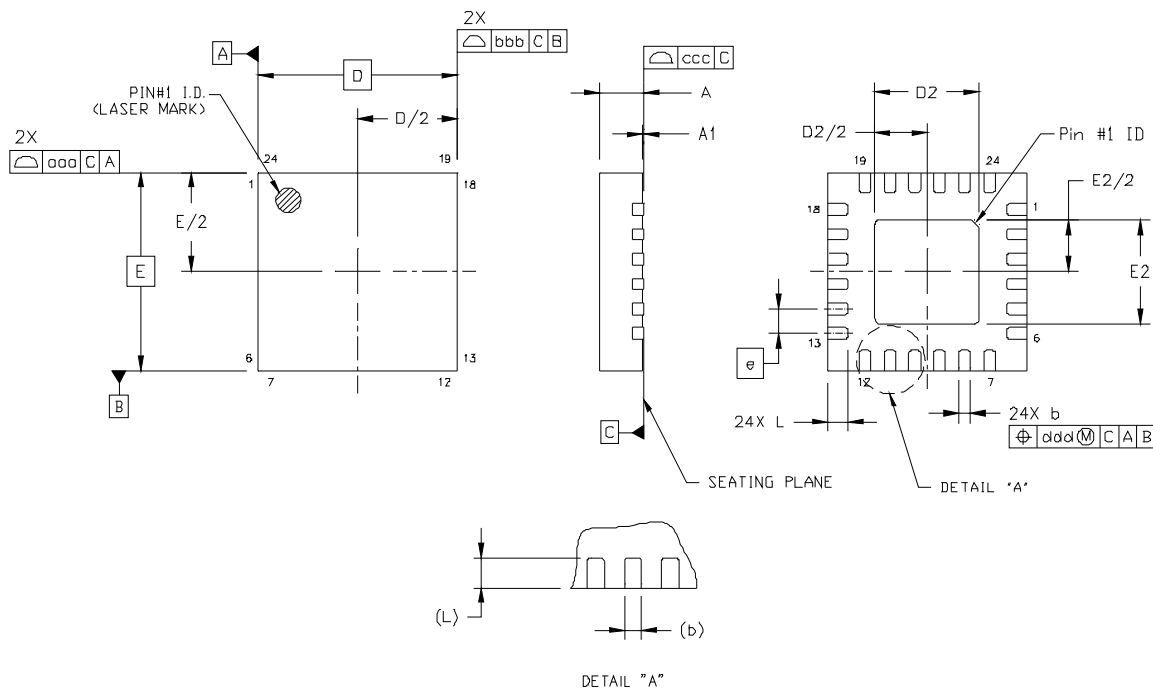


Figure 27. 24-Pin QFN

Table 20. 24-Pin QFN Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.40	2.50	2.60
e	0.50 BSC		
E	4.00 BSC		

Dimension	Min	Nom	Max
E2	2.40	2.50	2.60
L	0.20	0.25	0.30
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2. 48-Pin eTQFP Package

Figure 28 illustrates the package details for 48-pin eTQFP package option for the Si2704/05/06/07. Table 21 lists the values for the dimensions shown in the illustration.

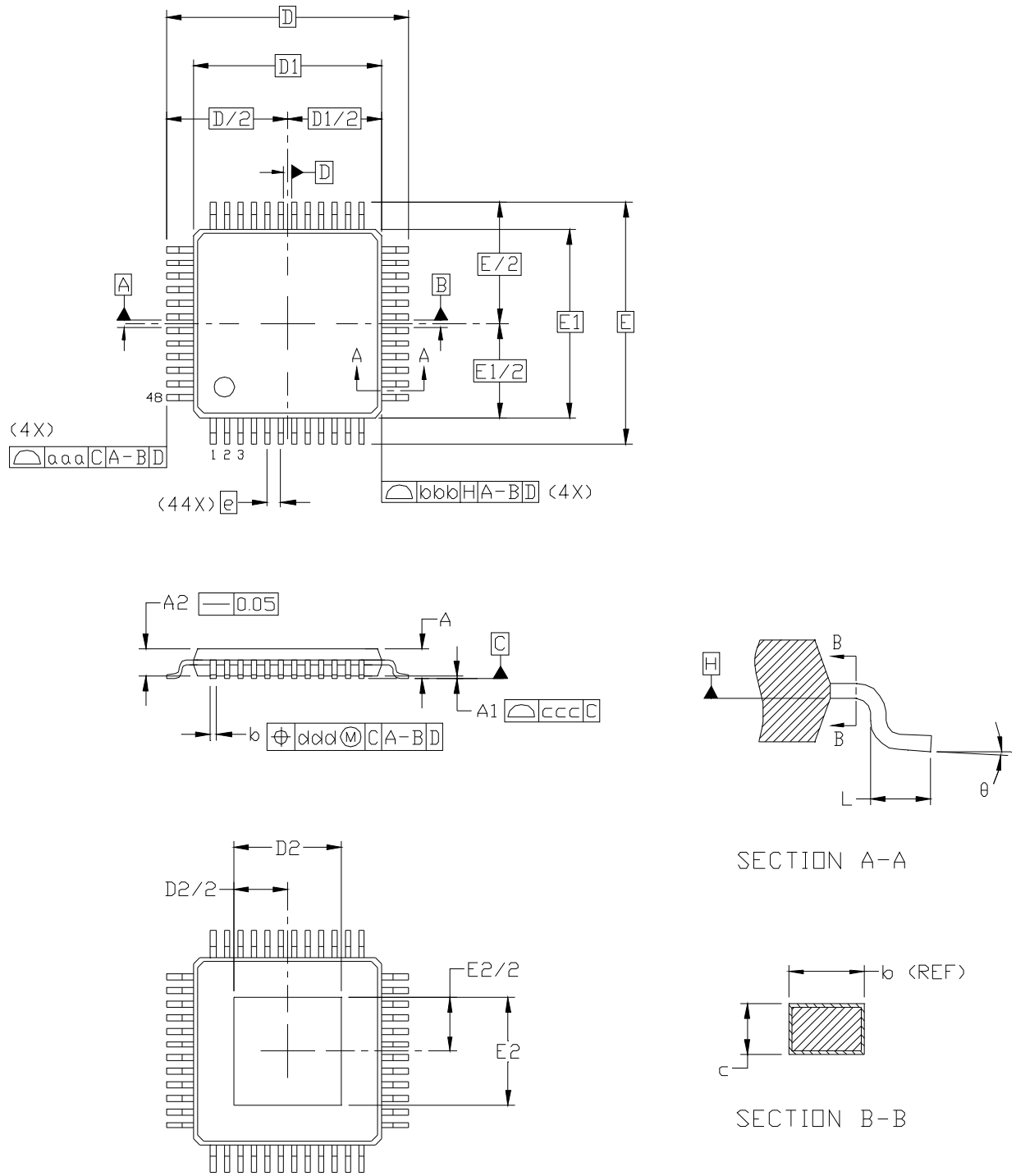


Figure 28. 48-Pin eTQFP

Table 21. 48-Pin eTQFP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
D2	3.71	3.81	3.91
e	0.50 BSC		

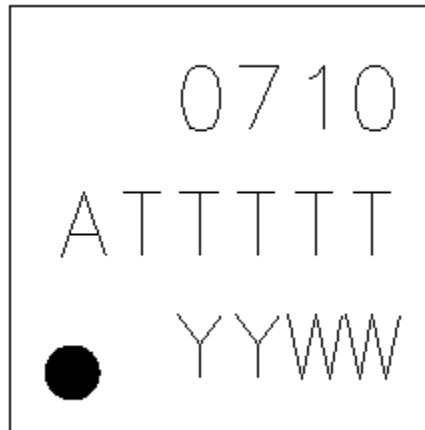
Dimension	Min	Nom	Max
E	9.00 BSC		
E1	7.00 BSC		
E2	3.71	3.81	3.91
L	0.45	0.60	0.75
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08
Θ	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Package Markings (Top Marks)

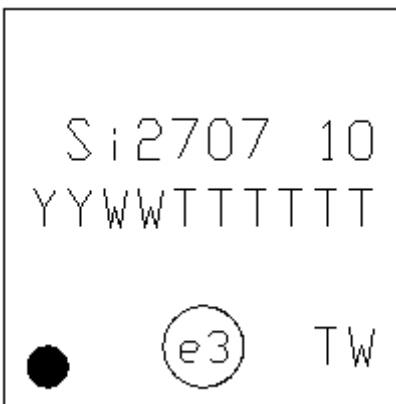
9.1. Si2707 Top Mark (QFN)



9.2. Top Mark Explanation

Mark Method	YAG Laser	
Line 1 Marking	Part Number	04 = Si2704 05 = Si2705 06 = Si2706 07 = Si2707
	Firmware Revision	10 = Firmware Revision 1.0
Line 2 Marking	Die Revision	A = Revision A Die
	TTTTT = Internal Code	Internal Tracking Code
Line 3 Marking	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

9.3. Si2707 Top Mark (eTQFP)



9.4. Top Mark Explanation

Mark Method	YAG Laser	
Line 1 Marking	Part Number	Si2704 Si2705 Si2706 Si2707
	Firmware Revision	10 = Firmware Revision 1.0
Line 2 Marking	Die Revision	A = Revision A Die
	TTTTT = Internal Code	Internal Tracking Code
Line 3 Marking	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

10. Additional Reference Resources

- Si270x Evaluation Board User's Guide
- AN469: 270x Programming Guide
- AN470: 270x Layout Guidelines
- AN502: Si270x Class-D Amplifier—Analog Source Setup
- AN503: Si270x Class-D Amplifier—Dynamic Range Compressor Use
- AN504: Si270x Class-D Amplifier—Dynamic Bass Configuration
- AN505: Si270x Class-D Amplifier—Measuring Output Power
- AN509: Si270x Class-D Amplifier—Ferrite Bead Filter
- AN510: Si270x Class-D Amplifier—Calculating Filter Loss
- Si270x Customer Support Site:

<http://www.silabs.com>

This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access to some of these documents. To request access, send mysilabs user name and request for access to AudiolInfo@silabs.com.

DOCUMENT CHANGE LIST

Revision 0.4 to Revision 0.5

- Updated Table 3 on page 6.
- Updated Table 4 on page 7.
- Updated Table 5 on page 7.
- Updated Table 6 on page 8.
- Updated Table 11 on page 12.
- Updated "2. Typical Application Schematic" on page 13.
- Updated Figure 15 on page 22.
- Added "4.5.5. I²S Master Mode" on page 24.
- Added note to "7. Ordering Guide" on page 37.
- Added "9. Package Markings (Top Marks)" on page 41.
- Added "9.3. Si2707 Top Mark (eTQFP)" on page 42.

Revision 0.5 to Revision 0.6

- Updated eTQFP pin assignments on pages 1 and 35.
- Updated eTQFP pin descriptions in Table 19 on page 35.
- Updated Table 1 on page 5.
- Updated Table 3 on page 6.
- Updated Table 4 on page 7.
- Updated Table 5 on page 7.
- Updated Table 11 on page 12.
- Updated "2. Typical Application Schematic" on page 13.
- Updated "3. Typical System Configurations" on page 14
 - Updated Figure 6 on page 14.
 - Updated Figure 9 on page 15.
- Updated "4. Functional Description" on page 16.
- Updated "4.4.1.2. External Reference Clock Operation" on page 23.
- Updated "5. Commands and Properties" on page 32.
 - Updated Table 16 on page 32.
 - Updated Table 17 on page 32.
- Updated "10. Additional Reference Resources" on page 43.

NOTES:

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