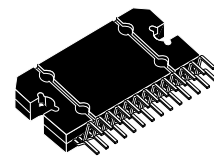




STA575

100+100W STEREO **BASH®** DIGITAL FIDELITY POWER AMPLIFIER

- MONOCHIP BRIDGE STEREO AMPLIFIER ON BASH® ARCHITECTURE
- 80+80W OUTPUT POWER @ $R_L = 4/8 \Omega$, THD = 0.5%
- 100+100W OUTPUT POWER @ $R_L = 4/8 \Omega$, THD = 10%
- HIGH DYNAMIC PREAMPLIFIER INPUT STAGES
- EXTERNAL PROGRAMMABLE FEEDBACK TYPE COMPRESSORS
- AC COUPLED INPUT TO CLASS AB BRIDGE OUTPUT AMPLIFIER
- PRECISION RECTIFIERS TO DRIVE THE DIGITAL CONVERTER
- ON-OFF SEQUENCE/ TIMER WITH MUTE AND STANDBY
- PROPORTIONAL OVER POWER OUTPUT CURRENT TO LIMIT THE DIGITAL CONVERTER
- ABSOLUTE POWER BRIDGE OUTPUT



FLEXIWATT27

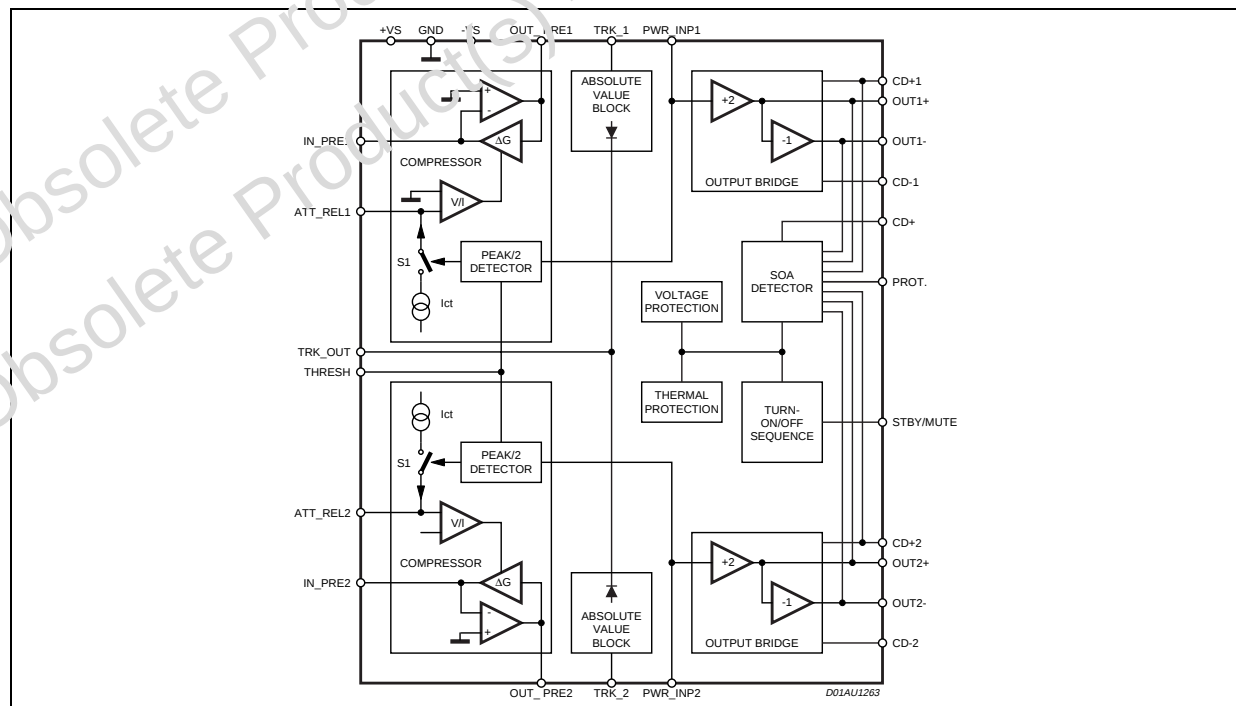
TRANSISTOR POWER PROTECTION

- ABSOLUTE OUTPUT CURRENT LIMIT
- INTEGRATED THERMAL PROTECTION
- POWER SUPPLY OVER VOLTAGE PROTECTION
- FLEXIWATT POWER PACKAGE WITH 27 PIN
- BASH® LICENCE REQUIRED

DESCRIPTION

The STA575 is a fully integrated power module designed to implement a BASH® amplifier when used in conjunction with STABP01 digital processor.

BLOCK DIAGRAM



DESCRIPTION (continued)

Notice that normally only one Digital Converter is needed to supply a stereo or multi-channel amplifier system, therefore most of the functions implemented in the circuit have summing outputs

The signal circuits are biased by fixed negative and positive voltages referred to Ground. Instead the final stages of the output amplifiers are supplied by two external voltages that are following the audio signal. In this way the headroom for the output transistors is kept at minimum level to obtain a high efficiency power amplifier.

The Compressor circuits, one for each channel, performs a particular transfer behavior to avoid the dynamic restriction that an adaptive system like this requires. To have a high flexibility the attack / release time and the threshold levels are externally programmable. The tracking signal for the external digital converter is generated from the Absolute Value block that rectifies the audio signal present at the compressor output. The outputs of these blocks are decoupled by a diode to permit an easy sum of this signal for the multichannel application. The output power bridges have a dedicated input pin to perform an AC decoupling to cancel the compressor output DC offset. The gain of the stage is equal to 4 (+12dB). A sophisticated circuit performs the output transistor power detector that, with the digital converter, reduces the power supply voltage. Moreover, a maximum current output limiting and the over temperature sensor have been added to protect the circuit itself. The external voltage applied to the STBY/MUTE pin forces the two amplifiers in the proper condition to guarantee a silent turn-on and turn-off.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
+V _S	Positive supply voltage referred to pin 13 (GND)	30	V
-V _S	Negative supply voltage referred to pin 13 (GND)	-24	V
V _{CD+}	Positive supply voltage tracking rail referred to pin 13 (GND)	22	V
V _{CD+}	Positive supply voltage operated to V _{S+} ⁽¹⁾	0.3	V
V _{CD-}	Negative supply voltage referred to -V _S ⁽¹⁾	-0.3	V
V _{CD-}	Negative supply voltage tracking rail referred to pin 13 (GND)	-22	V
V _{Att_Rel1} V _{Att_Rel2}	Pin 3, 25 Negative & Positive maximum voltage referred to GND (pin 13)	-0.5 to +20	V
V _{Pwr_imp1} V _{Pwr_imp2} V _{Trk_1} V _{Trk_2}	Pin 7, 21, 18, 10 Negative & Positive maximum voltage referred to GND (pin 13)	-20 to +20	V
V _{In_pre1} V _{In_pre2}	Pin 8, 20 Negative & Positive maximum voltage referred to GND (pin 13)	-0.5 to +0.5	V
V _{threshold}	Pin 17 Negative & Positive maximum voltage referred to GND (pin 13)	-7 to +0.5	V
I _{stb-max}	Pin 11 maximum input current (Internal voltage clamp at 5V)	500	μA
V _{stbmute}	Pin 11 negative maximum voltage referred to GND (pin 13)	-0.5	V
I _{out}	Output current	7.7	A

Note 1: V_{CD-} must not be more negative than -V_S and V_{CD+} must not be more positive than +V_S

Note 2: All pins withstand ±2KV ESD but not pin 11

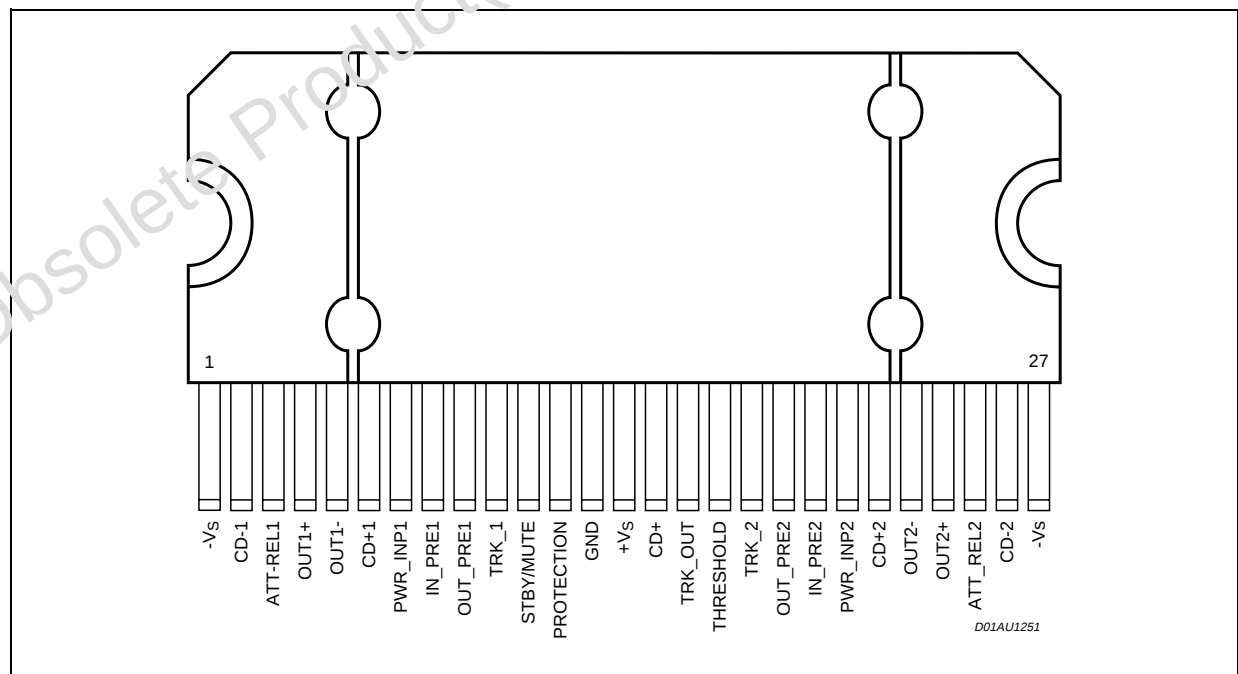
THERMAL DATA

Symbol	Parameter	Value	Unit
T_j	Max Junction temperature	150	°C
$R_{th\ j_case}$	Thermal Resistance Junction to case max	1	°C/W

OPERATING RANGE

Symbol	Parameter	Value	Unit
$+V_s$	Positive supply voltage	+20 to +28	V
$-V_s$	Negative supply voltage	-10 to -23	V
ΔV_{s+}	Delta positive supply voltage	$5V \leq (V_{s+} - V_{CD+}) \leq 10V$	V
V_{CD+}	Positive supply voltage tracking rail	+3 to 20.7	V
V_{CD-}	Negative supply voltage tracking rail	-20.7 to -3	V
I_{in_Max}	Current at pin In_Pre1, In_Pre2, related to compressor behaviour	-1 to +1	mA peak
$V_{threshold}$	Voltage at pin Threshold	-5 to 0	V
T_{amb}	Ambient Temperature Range	0 to 70	°C
I_{sb_max}	Pin 11 maximum input current (Internal voltage comp at 5V)	200	µA

PIN CONNECTION



Note: Slug connected to pins n. 1 and 27

PIN FUNCTION

N°	Name	Description
1	-Vs	Negative Bias Supply
2	CD-1	Channel 1 Time varying tracking rail negative power supply
3	Att_Rel1	Attack release rate for channel 1
4	Out1+	Channel 1 speaker positive output
5	Out1-	Channel 1 speaker negative output
6	CD+1	Channel 1 positive power supply
7	Pwr_Inp1	Input to channel 1 power stage
8	In_pre1	Pre-amp input for channel 1 (virtual ground)
9	Out_pre1	Output channel 1 pre-amp
10	Trk_1	Absolute value block input for channel 1
11	Stby/mute	Standby/mute input voltage control
12	Protection	Protection signal for STABP01 digital processor
13	Gnd	Analog Ground
14	+Vs	Positive Bias Supply
15	CD+	Time varying tracking rail positive power supply
16	Trk_out	Reference output for STABP01 digital processor
17	Threshold	Compressor threshold input
18	Trk_2	Absolute value block input for channel 2
19	Out_pre2	Output channel 2 pre-amp
20	In_pre2	Pre-amp input for channel 2 (virtual ground)
21	Pwr_Inp2	Input to channel 2 power stage
22	CD+2	Channel 2 positive power supply
23	Out2-	Channel 2 speaker negative output
24	Out2+	Channel 2 speaker positive output
25	Att_Rel2	Attack release rate for channel 2
26	CD-2	Channel 2 Time varying tracking rail negative power supply
27	-Vs	Negative Bias Supply

ELECTRICAL CHARACTERISTICS (Test Condition: $V_{S+} = 28V$, $V_{S-} = -23V$, $V_{CD+} = 20V$, $V_{CD-} = -20V$, $R_L = 8\Omega$, external components at the nominal value $f = 1KHz$, $T_{amb} = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PREAMPLIFIER AND COMPRESSOR						
$V_{out\ clamp}$	Maximum Voltage at Out_pre pin		9	11	13	Vpeak
I_{in}	Audio input current				0.8	mA
$V_{control}$	Voltage at Attack_Release pin	Attenuation = 0dB Attenuation = 6dB Attenuation = 26dB	0.35 6	0 0.5 9	0.65 12	V V V
$V_{C_{omp_Th}}$	Input voltage range for the compression		-5		-1	V
Z_{th}	Input impedance of Threshold pin		100			K Ω
Voffset	Output Offset at Out_pre pin with:	$V_{CRT} = 0V$; Attenuation = 0dB $V_{CRT} = 0.5V$; Attenuation = 6dB $V_{CRT} = 9V$; Attenuation = 26dB	-15 -250 -1000		15 250 450	mV mV mV
THD	Distortion at Out_pre:	$V_{CRT} = 0V$; Attenuation = 0dB $V_{CRT} = 0.5V$; Attenuation = 6dB $V_{CRT} = 9V$; Attenuation = 26dB		0.01	0.1 0.5 2	% % %
EN	Noise at Out_pre pin :	$V_{CRT} = 0V$; Attenuation = 0dB $V_{CRT} = 0.5V$; Attenuation = 6dB $V_{CRT} = 9V$; Attenuation = 26dB		$10^{(2)}$ 50 60		μV μV μV
I_{ct}	Attack time current at pin Attack_release		0.5	1.5	3	mA

1. This value is due to the thermal noise of the external resistors R_r and R_i .

TRACKING PARAMETERS

G_{trk}	Tracking reference voltage gain		13	14	15	V
V_{trk_out}	Tracking ref. output voltage		0	20		V
I_{trk_out}	Current capability		5	6	7	mA
Z_{trk_in}	Input impedance ($T_{RK1/2}$)			1		M Ω

OUTPUT BRIDGE

G_{out}	Half Output bridge gain		5.5	6	6.5	dB
G_{ch}	Output bridge differential gain		11	12	13	dB
ΔG_{ch}	Output bridges gain mismatch		-0.5		0.5	dB
P_{out}	Continuous Output Power	THD = 0.5% THD = 10%	75 95	80 100		W W
		THD = 10%; $R_L = 4\Omega$; $V_{CD+} = 16V$; $V_{CD-} = -16V$; $V_{S+} = 22V$; $V_{S-} = -22V$	90	100		W
THD	Total harmonic distortion of the output bridge	$P_o = 5W$		0.01	0.1	%
		$f = 20Hz$ to $20KHz$; $P_o = 50W$			0.2	%
V_{Off}	Output bridge D.C. offset		-70		70	mV

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
EN	Noise at Output bridge pins	$f = 20\text{Hz to } 20\text{kHz}; R_g = 50\Omega$		12		μV
Z_{br_in}	Input impedance		100	140	180	$\text{K}\Omega$
R_{dson}	Output power R_{dson}	$I_O = 1\text{A}$		200	400	$\text{m}\Omega$
OLG	Open Loop Voltage Gain			100		dB
GB	Unity Gain Bandwidth			1.4		MHz
SR	Slew Rate			8		$\text{V}/\mu\text{s}$
PROTECTION						
V_{stby}	Stby voltage range		0		5.8	V
V_{mute}	Mute voltage range		1.6		2.5	V
V_{play}	Play voltage range		4		5	V
T_{h1}	First Over temperature threshold			130		$^{\circ}\text{C}$
T_{h2}	Second Over temperature threshold			150		$^{\circ}\text{C}$
Unbal. Ground	Upper Unbalancing ground threshold	Referred to $(CD^+ - CD^-)/2$		5		V
Unbal. Ground	Lower Unbalancing ground threshold	Referred to $(CD^+ - CD^-)/2$		-5		V
UV_{th}	Under voltage threshold	$ V_{S+} + V_{S-} $	18	20	22	V
$P_{d_reg.}$	Power dissipation threshold for system regulation	$I_{prot} = 50\mu\text{A}; @ V_{ds} = 10\text{V}$	26	32	39	W
P_{d_max}	Switch off power dissipation threshold	@ $V_{ds} = 10\text{V}$		60		W
I_{prot}	Protection current slope	for $P_d > P_{d_reg}$		400		$\mu\text{A}/\text{W}$
I_{lct}	Limiting Current threshold		6.3	7	7.5	A
I-Vs	Positive supply current	Stby ($V_{stby}/\text{mute pin} = 0\text{V}$) Mute ($V_{stby}/\text{mute pin} = 2.5\text{V}$) Play ($V_{stby}/\text{mute pin} = 5\text{V}$ no signal)	20 20	5 35 35	7 50 50	mA mA mA
I-Vs	Negative supply current	Stby ($V_{stby}/\text{mute pin} = 0\text{V}$) Mute ($V_{stby}/\text{mute pin} = 2.5\text{V}$) Play ($V_{stby}/\text{mute pin} = 5\text{V}$ no signal)	20 20	5 35 35	7 50 50	mA mA mA
ICD+	Positive tracking rail supply current	Stby ($V_{stby}/\text{mute pin} = 0\text{V}$) Mute ($V_{stby}/\text{mute pin} = 2.5\text{V}$) Play ($V_{stby}/\text{mute pin} = 5\text{V}$ no signal)	50 60 60	100 110 110	200 180 180	μA mA mA
ICD-	Negative tracking rail supply current	Stby ($V_{stby}/\text{mute pin} = 0\text{V}$) Mute ($V_{stby}/\text{mute pin} = 2.5\text{V}$) Play ($V_{stby}/\text{mute pin} = 5\text{V}$ no signal)	50 60 60	100 110 110	200 180 180	μA mA mA

FUNCTIONAL DESCRIPTION

The circuit contains all the blocks to build a stereo amplifier. Each single channel is based on the Output Bridge Power Amplifier, and its protection circuit. Moreover, the compression function and a signal rectifier are added to complete the circuit.

The operation modes are driven by The Turn-on/off sequence block. In fact the IC can be set in three states by the Stby/mute pin:

Standby ($V_{pin} < 0.8V$), Mute ($1.6V < V_{pin} < 2.5V$), and Play ($V_{pin} > 4V$).

In the Standby mode all the circuits involved in the signal path are in off condition, instead in Mute mode the circuits are biased but the Speakers Outputs are forced to ground potential.

These voltages can be get by the external RC network connected to Stby/Mute pin.

The same block is used to force quickly the I.C. In standby mode or in mute mode when the I.C. dangerous condition has been detected. The RC network in these cases is used to delay the Normal operation restore.

The protection of the I.C. are implemented by the Over Temperature, Unbalance Ground, Output Short circuit, Under voltage, and output transistor Power sensing as shown in the following table:

Table 1. Protection Implementation

Fault Type	Condition	Protection strategy	Action time	Release time
Chip Over temperature	$T_j > 130\text{ }^{\circ}\text{C}$	Mute	Fast	Slow Related to Turn_on sequence
Chip Over temperature	$T_j > 150\text{ }^{\circ}\text{C}$	Standby	Fast	Slow, Related to Turn_on sequence
Unbalancing Ground	$ V_{gnd} > ((CD+) - (CD-))/2 + 5V$	Standby	Fast	Slow, Related to Turn_on sequence
Short circuit	$I_{out} > 7A$	Standby	Fast	Slow, related to Turn_on sequence
Under Voltage	$ V_{s+} + V_{s-} < 20V$	Standby	Fast	Slow, related to Turn_on sequence
Extra power dissipation at output transistor	$P_{d\ tr.} > 32W$	Reducing DIGITAL CONVERTER output voltage.	Related to the DIGITAL CONVERTER	Related to the DIGITAL CONVERTER
Maximum power dissipation at output transistor	$P_{d\ tr.} > 60W$	Standby	Fast	Slow, related to Turn_on sequence

See the POWER PROTECTION paragraph for the details

Compression

An other important function implemented, to avoid high power dissipation and clipping distortion, is the Compression of the signal input. In fact the preamplifier stage performs a voltage gain equal to 5, fixed by R_i and R_r external resistor, but in case of high input signal or low power supply voltage, its gain could be reduced of 26dB. This function is obtained with a feedback type compressor that, in practice, reduces the impedance of the external feedback network. The behavior of compression it's internally fixed but depends from the Audio input voltage signal level, and from the Threshold voltage applied to the Threshold pin. The attack and release time are programmable by the external RC network connected to the Att_Rel pins.

The constraints of the circuit in the typical application are the following:

$V_{threshold}$ range = -5 to 0
 $V_{in\ peak\ max}$ = 8V
 $V_{out\ peak\ max}$ = 10V

Gain without compression (G) = 5

Max Attenuation ratio = 26 dB

The following graph gives the representation of the Compressor activation status related to the Vthreshold and the input voltage. The delimitation line between the two fields, compression or not, is expressed by the formula :

$$\frac{2 \cdot (|V_{\text{threshold}}| + 200\text{mV})}{G}$$

Where G is the preamplifier gain without compression.

In the compression region the gain of the preamplifier will be reduced

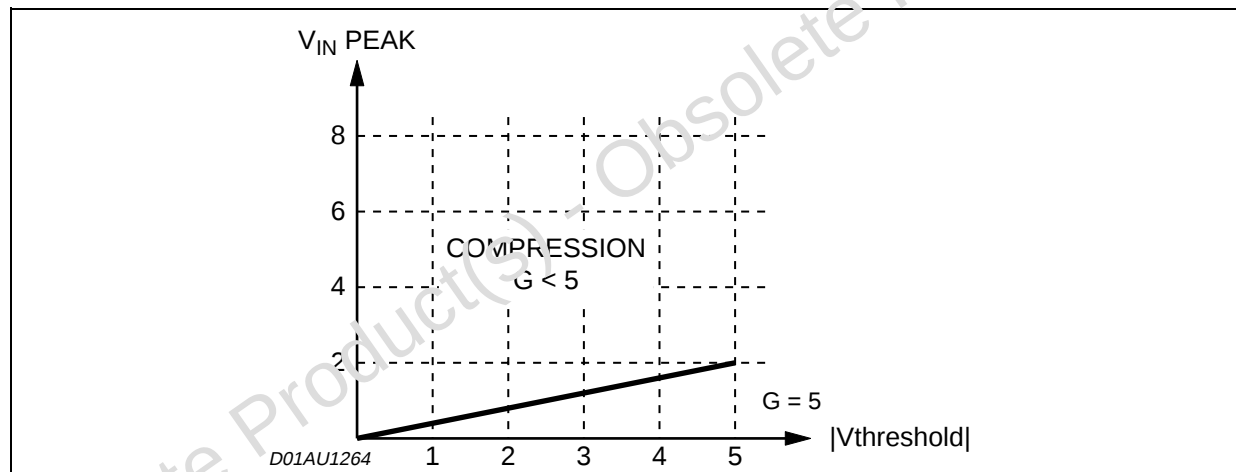
($G = 2 \cdot V_{\text{threshold}}/V_{\text{in}}$) to maintain at steady state the output voltage equal $2 \cdot |V_{\text{threshold}}|$.

Instead in the other region the compressor will be off ($G = 5$).

The delimitation line between the two fields can be related to the output voltage of the preamplifier: in this case the formula is :

$$V_{\text{out}} = 2 \cdot (|V_{\text{threshold}}| + 200\text{mV})$$

Figure 1. Compressor activation field



The relative attenuation introduced by the variable gain cell is the following :

$$\text{Attenuation} = 20\log \frac{2}{5} \cdot \frac{(|V_{\text{th}}| + 200\text{mV})}{V_{\text{in_peak}}}$$

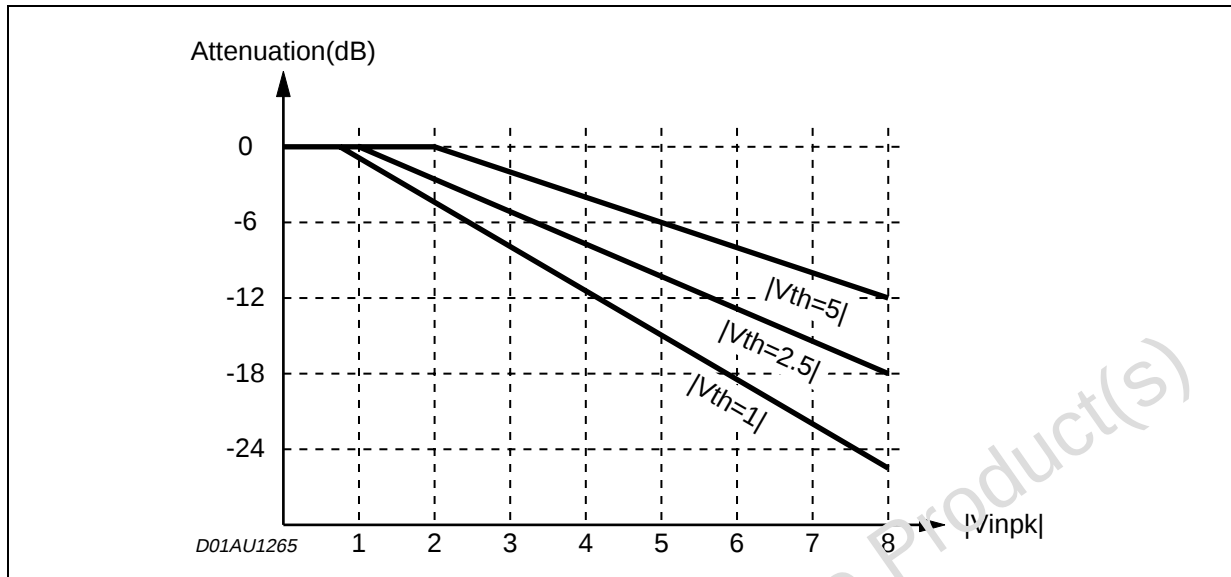
The total gain of the stage will be:

$$G_{\text{db}} = 20\log 5 + \text{Attenuation}$$

The maximum input swing is related to the value of input resistor, to guarantee that the input current remain under $I_{\text{in_Max}}$ value (1 mA).

$$R_i > \frac{V_{\text{in_peak}}}{I_{\text{in_max}}}$$

Figure 2. Compressor attenuation vs. input amplitude



ABSOLUTE VALUE BLOCK

The absolute value block rectifies the signal after the compression to extract the control voltage for the external digital converter. The output voltage swing is internally limited, the gain is internally fixed to 14.

The input impedance of the rectifier is very high, to allow the appropriate filtering of the audio signal before the rectification (between Out_pre and Trk pins).

OUTPUT BRIDGE

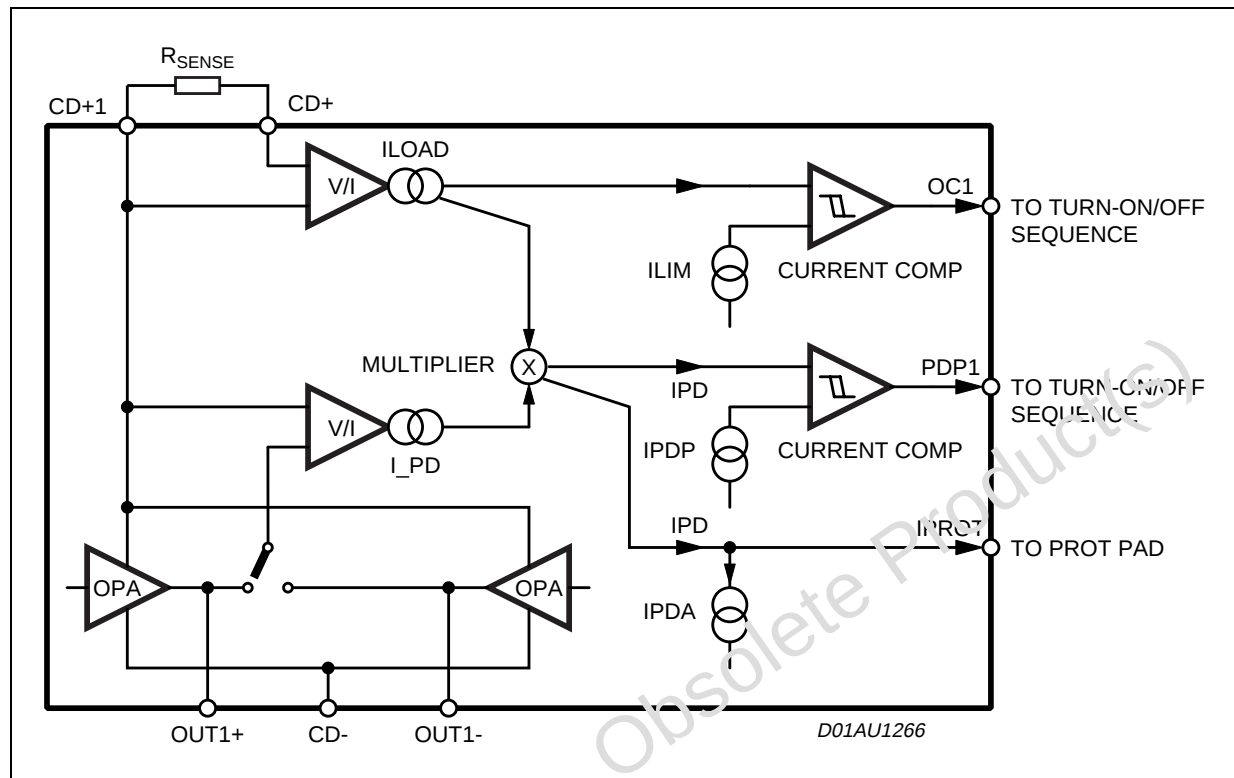
The Output bridge amplifier makes the single-ended to Differential conversion of the Audio signal using two power amplifiers, one in non-inverting configuration with gain equal to 2 and the other in inverting configuration with unity gain. To guarantee the high input impedance at the input pins, Pwr_Inp1 and Pwr_Inp2, the second amplifier stages are driven by the output of the first stages respectively.

POWER PROTECTION

To protect the output transistors of the power bridge a power detector is implemented (fig 3).

The current flowing in the power bridge and through the series resistor R_{sense} is measured reading the voltage drop between CD+1 and CD+. In the same time the voltage drop on the relevant power (V_{ds}) is internally measured. These two voltages are converted in current and multiplied: the resulting current, I_{pd} , is proportional to the instantaneous dissipated power on the relevant output transistor. The current I_{pd} is compared with the reference current I_{pda} , if bigger (dissipated power > 32W) a current, I_{prot} , is supplied to the Protection pin. The aim of the current I_{prot} is to reduce the reference voltage for the digital converter supplying the power stage of the chip, and then to reduce the dissipated power. The response time of the system must be less than 200 μ Sec to have an effective protection. As further protection, when I_{pd} reaches an higher threshold (when the dissipated value is higher than 60W) the chip is shut down, forcing low the Stby/Mute pin, and the turn on sequence is restarted.

Figure 3. Power Protection Block Diagram



In fig. 3 there is the power protection strategy pictures. Under the curve of the 32W power, the chip is in normal operation, over 60W the chip is forced in Standby. This last status would be reached if the digital converter does not respond quickly enough reducing the stress to less than 60W.

The fig.4 gives the protection current, i_{prot} , behavior. The current sourced by the pin Prot follows the formula:

$$I_{prot} \equiv \frac{(P_d - P_{d_{av_{th}}}) \cdot 5 \cdot 10^{-4}}{1.25V}$$

for $P_d < P_{d_{av_{th}}}$ the $I_{prot} = 0$

Independently of the output voltage, the chip is also shut down in the following conditions:

When the current through the sensing resistor, R_{sense} , reaches 7A (Voltage drop $(CD+) - (CD+1) = 700mV$).

When the average junction temperature of the chip reaches 150°C.

When the ground potential differ from more than 5V from the half of the power supply voltage, $((CD+) - (CD-))/2$

When the sum of the supply voltage $|Vs+| + |Vs-| < 20V$

The output bridge is muted when the average junction temperature reaches 130°C.

Figure 4. Power protection threshold

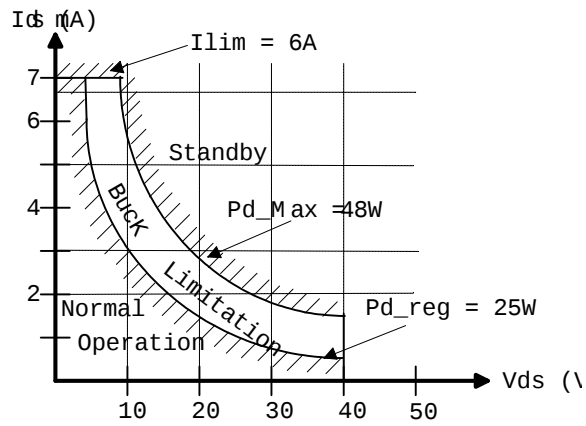


Figure 5. Protection current behaviour

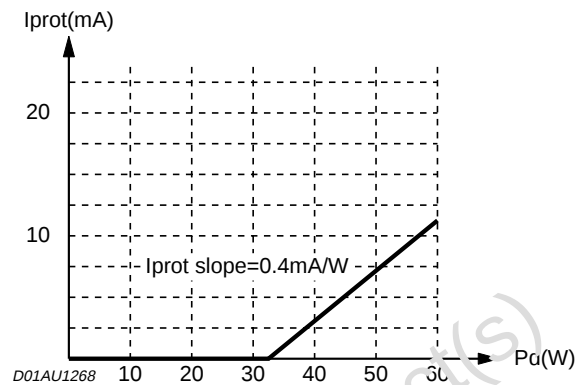
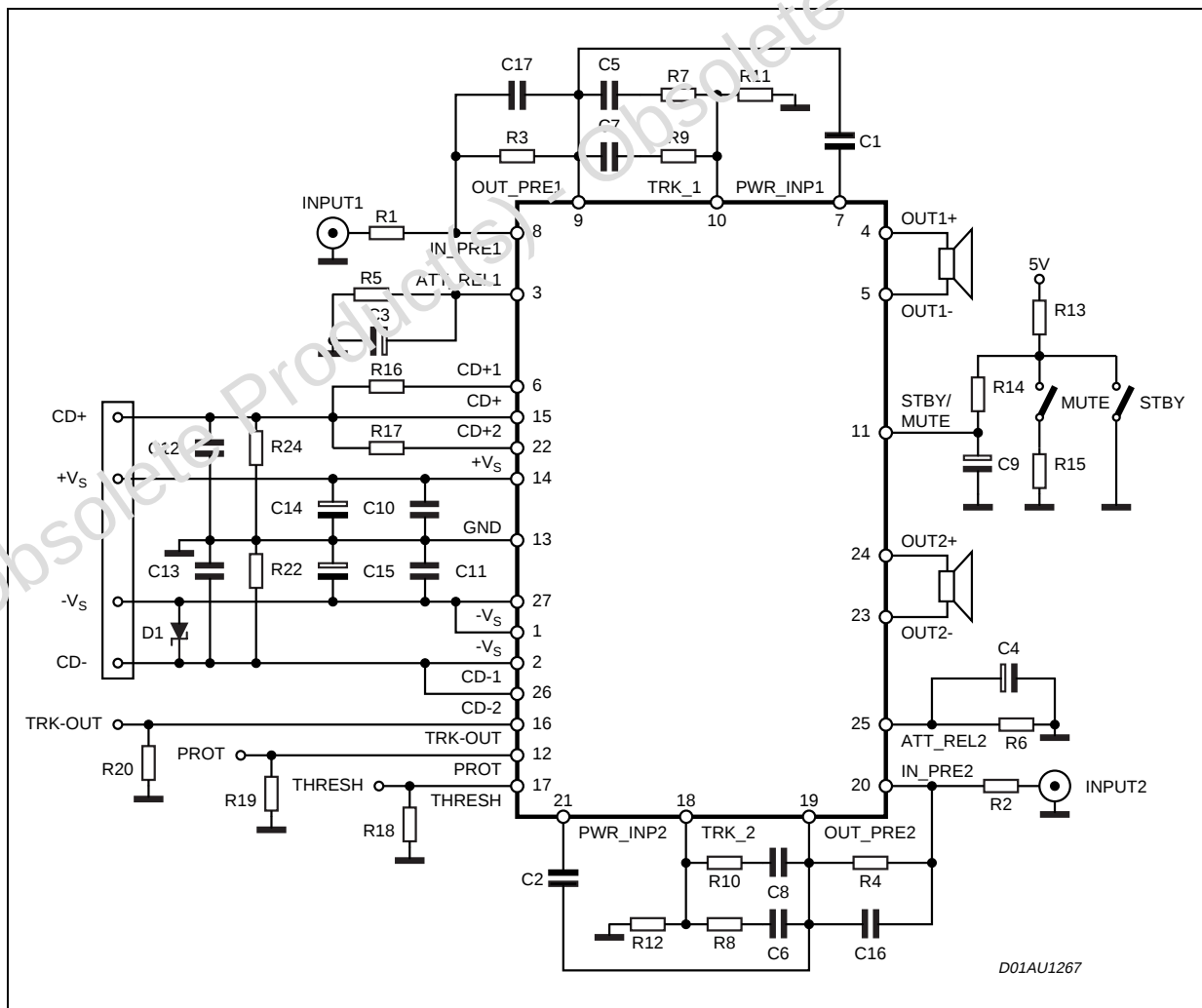


Figure 6. Test Circuit for STA575 Stand-alone



EXTERNAL COMPONENTS (refer to fig. 6)

Name	Function	Value	Formula
R _i R1 = R2	Input resistor	10KΩ (G = 5, R _r = 50KΩ)	$R_i = \frac{R_r}{ G }$
R _r R3 = R4	Feedback resistor	50KΩ (G = 5, R _i = 10KΩ)	$R_r = G \cdot R_i$
C _{ac} C1 = C2	AC Decoupling capacitor	100nF (f _p = 16Hz, R _{ac} = 100KΩ)	$C_{ac} = \frac{1}{2\pi \cdot f_p \cdot R_{ac}}$
C _{ct} C3 = C4	Capacitor for the attack time	2.2μF (T _{attack} = 13mSec, V _{control} = 9V, I _{ct} = 1.5mA)	$C_{ct} = \text{attack} \cdot \frac{I_{ct}}{V_{control}}$
R5 = R6	Release constant time Resistor	470KΩ (t = 1 Sec. , C _{ct} = 2.2 μF)	$R_{ct} = \frac{\tau}{C_{ct}}$
R7 = R8	Resistor for tracking input voltage filter	10KΩ	
R9 = R10	Resistor for tracking input voltage filter	56KΩ	
R11 = R12	Resistor for tracking input voltage filter	10KΩ	
C5 = C6	Capacitor for Tracking input voltage filter	1nF	
C7 = C8	Dc decoupling capacitor	1μF	
R13	Bias Resistor for Stby/Mute function	10KΩ	
R14	Stby/Mute constant time resistor	30KΩ	
R15	Mute resistor	30KΩ	
C9	Capacitor for Stby/Mute resistor	2.2μF	
R16 = R17	Sensing resistor for SOA detector	100mΩ 5% 4W	
R18	Conversion resistor for threshold voltage	100KΩ	
C10 = C11	Power supply filter capacitor	100nF	
R22 = R24	Centering resistor	400 Ω , 1W	
C12 = C13	Tracking rail power supply filter	680nF	
R19	Protection	1KΩ	
R20	TRK_out	40KΩ	
C14 = C15	Power supply filter capacitor	470 μF , 63V	
C16 = C17	Feedback capacitor	100pF	
D1	Schottky diode	SB360	

Note: V_{control} is the voltage at Att_Rel pin.

APPLICATION HINTS (refer to fig. 6)**PREAMPLIFIER AND COMPRESSOR**

In the test circuit showed in figure 6, R_1/R_3 (or R_2/R_4) ratio fix the gain of the preamplifier.

If the input signal is very low, is possible to increase the gain fixing the product $V_{in} \cdot G = \text{cost}$.

In that case is possible to increase G decreasing $R_{1,2}$ from $10K\Omega$ until $2K\Omega$ without relevant effects on the circuit behavior and remaining in the operating range $I_{in_max} = V_{in_max}/R_{1(2)} < 1\text{mA}$.

So it is possible to increase the preamplifier gain until 25.

If no compression is present (equivalent compressor $G_m=0$), the effects are:

- The output voltage offset increase
- The SNR decrease

The following table shows these variations:

$R_{1,2}$	$V_{IN\ MAX}$	G	V_{OFFSET}	V_{EN}
$10K\Omega$	8V	5	15mV	$10\mu V$
$5K\Omega$	4V	10	30mV	$13\mu V$
$2K\Omega$	1.6V	25	75mV	$20\mu V$

$R_{3(4)} = 50K\Omega$ and all the other external components are the same

Attenuation = 0 dB

If the compression is active the circuit behaviour is the same

It's also possible to eliminate the compressor. In this case the ATT_REL (1,2) pin must be connected to gnd.

STBY-MUTE CIRCUIT

In the suggested application circuit (figure 6), the resistor for Standby/Mute function (R_{13}) is connected between the Standby/Mute switches and 5V Supply.

It is possible to connect the resistor to another Supply Voltage level V_L , but in that case also the resistor value ($R_{13,14}$) must be changed according to the following formula (fixing $V_{STBY/MUTE} = 2.5V$ and $R_{15} = 10K\Omega$):

$$R_{13} = (4 \cdot V_L - 10)K\Omega$$

$$R_{14} = (4 \cdot V_L + 10)K\Omega$$

HEADROOM

In the suggested application circuit the supply voltage to obtain 75W (Power Output) on 8Ω (R_{load}) is:

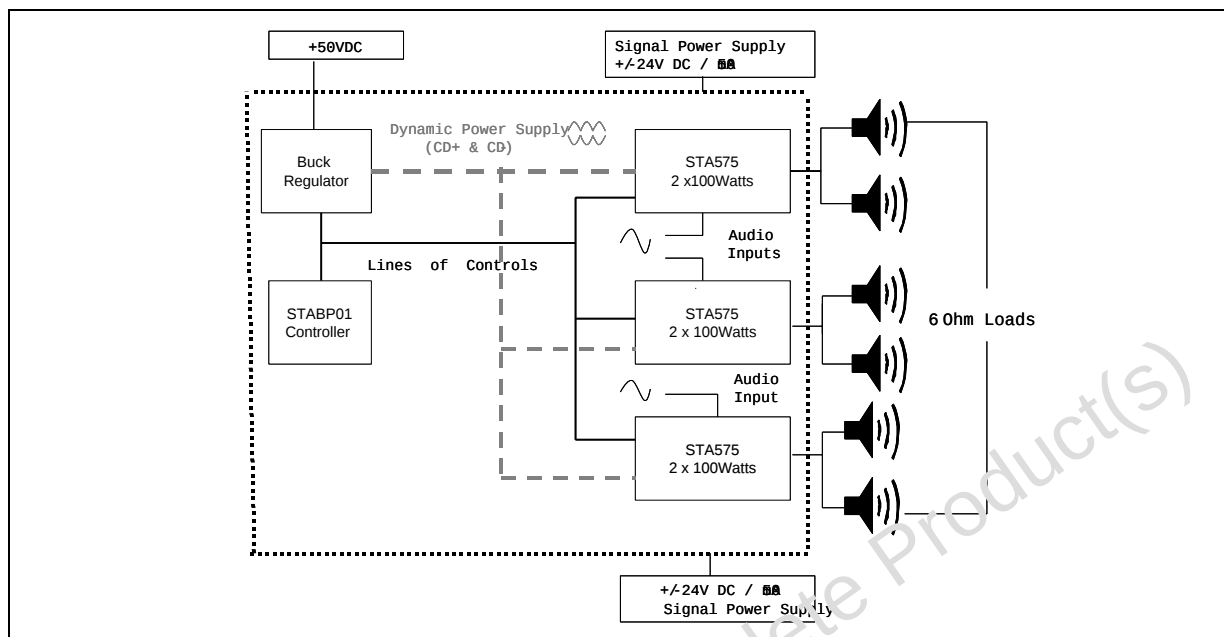
$$V_{supply} = \Delta V + I_{L, MAX} \cdot R_{DSon}$$

It is also possible to increase the system's efficiency forcing the headroom to follow the output signal (variable drop instead of a constant drop).

In that case:

$$V_{supply} = \Delta V + I_L(V) \cdot R_{DSon}$$

Figure 7. BASH® module SAM351 5.1 with 2 x STA575 (see application note AN1656)

**Power - On-Off sequences:**

In order to avoid damages to the SAM261 board it is important to follow these sequences:

At **Power-On** apply in the first the **Auxiliary Power Supply ($\pm 24V$)** and after the **Main Power Supply ($+50V$)**, in this condition the system is in "Mute state" and it can move in "play state" with the switch present on the pcb.

At **Power-Off** is better to bring the SAM module in "Mute state" and after that to follow this order: switch-off the **Main Supply Voltage ($+50V$)** and subsequently the **Auxiliary Power Supply. ($\pm 24V$)**.

System Description & Operating Rules

SAM351 is a BASH® 5.1 amplifier (6 x 100W) implementation utilizing the STA575 Integrated Circuit.

Specifically designed for multi-channel implementation in DVD - HTIB systems, Multi-Media systems, AV Receivers.

SAM351 is dimensioned to provide the maximum Output Power (THD=10 %) on two channels and instantaneously and 1/3 max Pout on the remaining Outputs, or 1/8 of max Pout continuous; this rule is important to define the main Power Supply size (+50V).

Buck Regulator Description

The function of the buck regulator is to convert efficiently an input voltage to a lower voltage by adjusting the ratio of the switching transistor's on-time to off-time. The resulting waveform is averaged by the output filter to recover an analog signal.

In the BASH amplifier this output is in effect split in half by centering it on the audio ground to provide CD+ and CD- rails.

To avoid the need for a high side driver for the transistor switch in the buck regulator the buck circuit recommended has the switch in the return path. Hence the gate drive circuit (part of the STPB01) is referenced to the negative return of the main supply that provides power for the buck regulator.

Interfacing STA575 to STPB01 (Feedback circuit)

This circuit produces a control signal current that is fed back to the STPB01 digital controller. The network used in this example compares the track signal (STA575 track out) to a fixed ratio of buck regulator's output (CD+) using a transistor. This method is effective because the controller's reference is the negative of the main DC supply, which is not referenced to audio ground.

The tracking signal is generated inside the STA575 (track out) by taking the absolute value of the pre-amp's output. The outputs of each channel and of each STA575 are then tied together in a diode-oring arrangement. This means that the highest of any given output is the output that determines the tracking signal.

The absolute value circuit inside the STA575 has gain. This makes it possible to use an RC network and a resistor divider to create a phase shift in the tracking signal at higher frequencies. This is also useful in optimizing the alignment of the buck regulator's output with the output signal of the bridge amplifier at high frequency.

This circuit first converts the buck switch current to a peak voltage. The control current is then converted to a voltage (using a resistor) and added to the peak voltage. By doing this, the buck is better able to maintain the desired headroom over a wide load range and output level.

Centering Network for CD+ & CD- Rails

The power rail of a bridge amplifier has no current flowing through the ground node, as the load is not connected to ground. However there are several different small sources of dynamic and continuous ground currents flowing from either CD+ or CD- to support the function of various things such as the control signal to the STPB01 controller.

The centering network prevents these currents from shifting the CD+/- rails away from center i.e. away from a symmetric split of the buck's output about ground. This is critical, even a small centering error requires an increase in headroom which results in a significant drop in output losses. In its simplest form the centering network could be a resistor divider from CD+ to CD- with its center tied to ground.

As long as the impedance is low enough (for example 200 ohms) this will swamp the smaller offset currents. It is helpful to put this kind of passive network on the board with the STA575 devices to help when testing this board on its own.

Power Amplifier Heatsink requirements

The heatsink requirements are dependent on several design goals. However there are two common references: Pink noise at 1/8 of full power, all channels loaded. This would approximate a system with all channels reproducing music at full volume with clipping occurring only occasionally. The second would be full power at 1kHz for 5 minutes after a one hour pre-soak at 1/8 power.

The worse of these two is the full power test. A conservative approach is to assume that the heatsink would come to thermal equilibrium after 5 minutes. Thus the Rth of the heatsink can be determined by:

$$R_{th \text{ heatsink}} = \frac{T_{jmax} - T_{amb}}{P_d} - R_{th-j \text{ case}} - R_{th \text{ case to heatsink}}$$

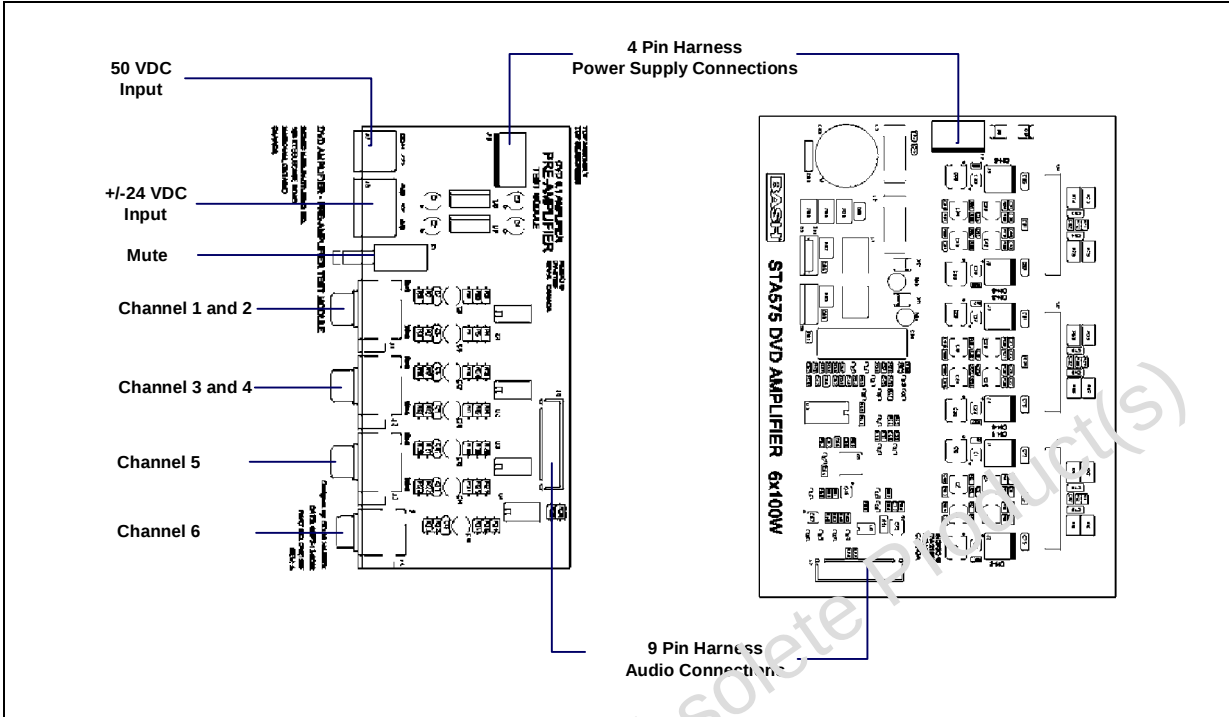
For example in the STA575 the Rth jc is 1°C / W. R case-to-heatsink with grease is about 0.5°C / W. The maximum operating junction temperature is 130°C, which for margin should be derated to 120°C

Buck Regulator Heatsink

The Buck regulator heatsink can be designed in a similar manner and does not change by varying power supply. In general the efficiency will be in the order of 85%. The thermal impedances from the junction(s) to the heatsink may be lower and the maximum operating temperature will be higher.

Usually either the sub or the remaining channels are tested at full power. The result is that usually the Buck heatsink is about ¼ the size of the linear heatsink, but this can be strongly affected by the design.

Figure 8. PCBs AND COMPONENTS LAYOUT



SAM261 Specification

Parameter	Rating	Notes
Output Power	100W _{avg} @10% - 6Ω	see graphs
THD + N	< 0.05% @ 40 Watts < 0.05% @ 75 Watts	Measured @ 1KHZ
SNR	-104 dB (relative to full power) -113 dB (A-weighted)	
Sensitivity	1 .3VRMS	Amplifier
Cross talk	-76dB (relative to 10W)	1KHz 8 Ohms,
Main Power Supply Inputs	60Volts @ 4 Amps	Maximum Voltage is 60V Minimum Voltage is 50V
Aux Power Supply Inputs	+ 24 Volts @ 100mA -24 Volts @ 100mA	Vs supply
Input Board	1 .3VRMS	Supplied to facilitate testing

Figure 9. THD +N FR Channel

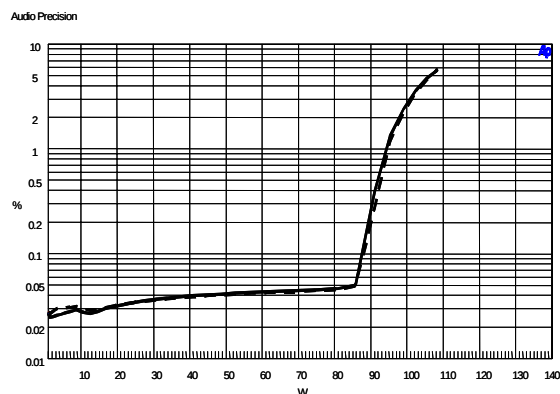


Figure 11. Residual Noise vs. Frequency

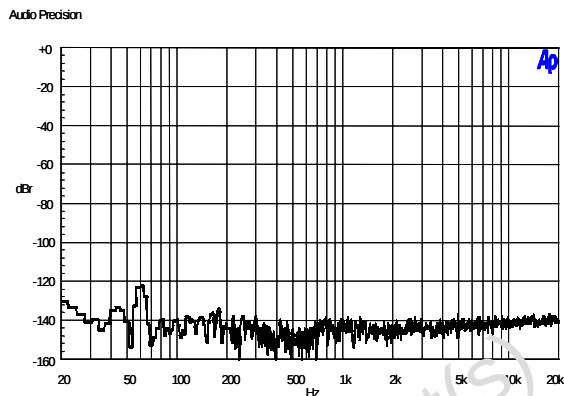


Figure 10. THD + N Frequency

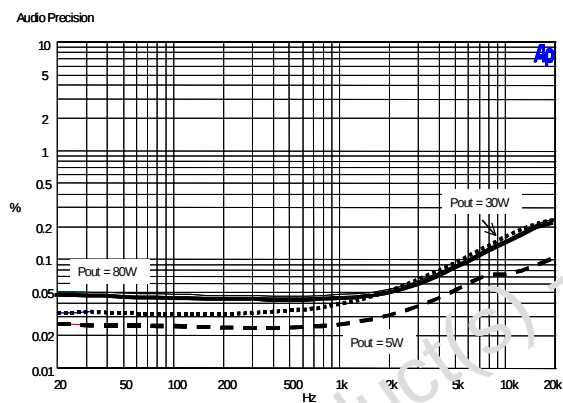


Figure 12. Frequency Response

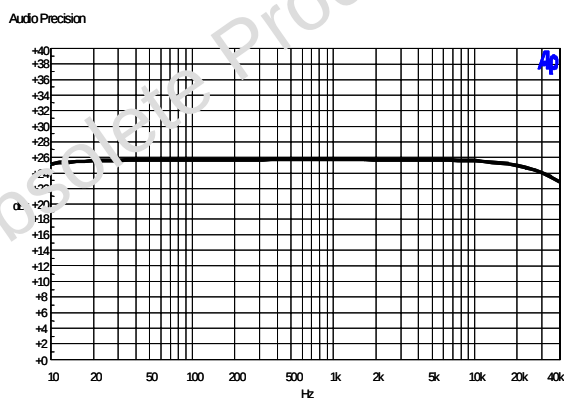
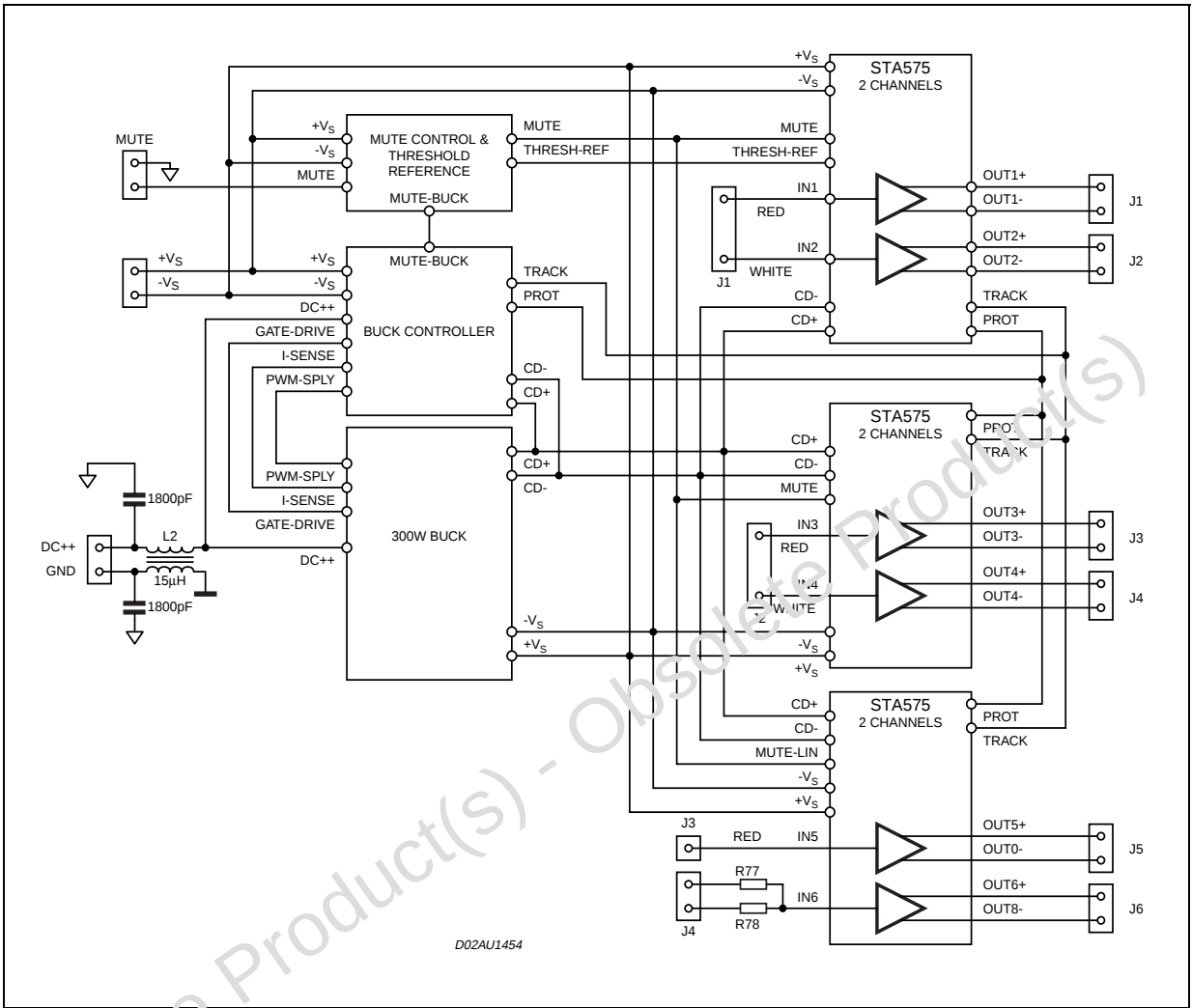


Figure 13. APPLICATION BLOCK DIAGRAM

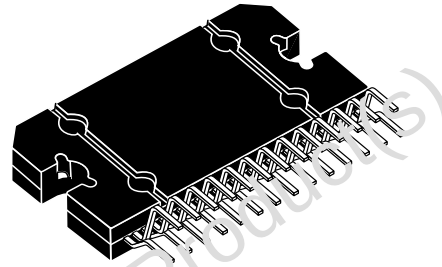


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

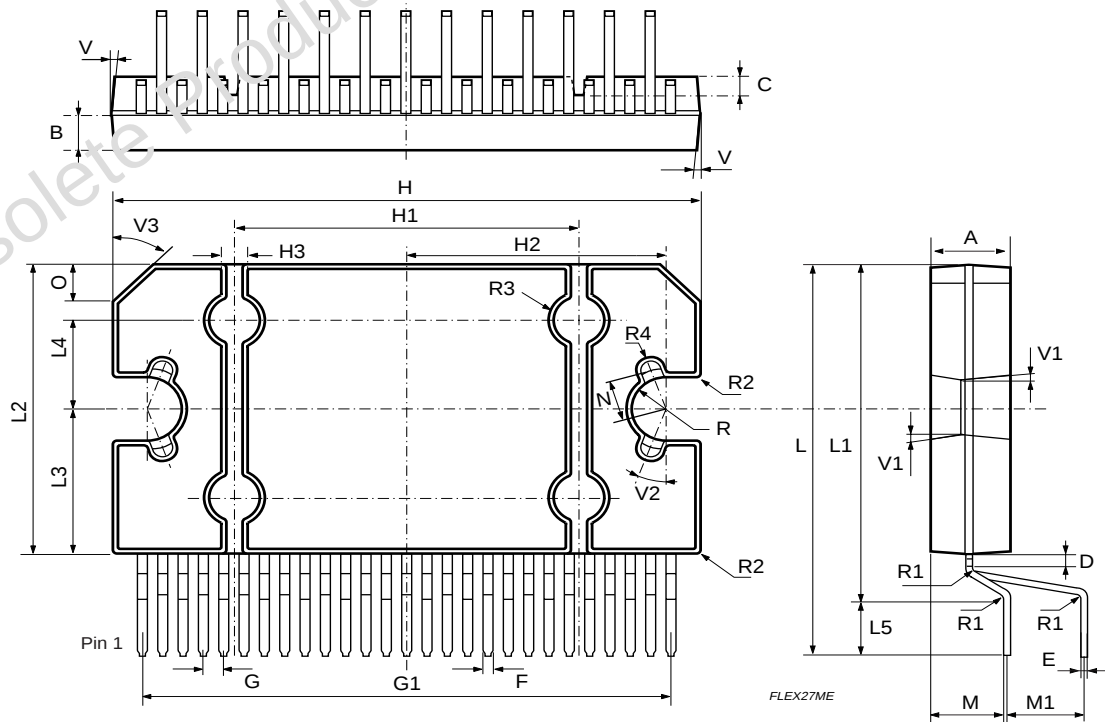
(1): dam-bar protusion not included

(2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)



Obsolete Product(s) - Obsolete Product(s)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

® 2003 STMicroelectronics - All Rights Reserved

 is the registered trademark and patented technology of INDIGO manufacturing inc.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>