

4.5V to 25V Input 1ch Synchronous Buck DC/DC Controller

BD95601MUV-LB

General Description

This is the product guarantees long time support in industrial market.

BD95601MUV-LB is a high current buck regulator that produces low output voltage (0.75V to 2.0V) from a wide input voltage range (4.5V to 25V). High efficiency is realized using external N channel MOSFETs.

Using H³Reg™, Rohm's advanced proprietary control method that uses constant on-time control to provide ultra-high transient responses to load changes.

SLLM (Simple Light Load Mode) technology is added to improve efficiency with light loads giving high efficiency over a wide load range. Soft start functionality, short circuit protection with timer latch, over current protection and tracking are all included features. This switching regulator was designed for low voltage high current power supplies.

Features

- Long Time Support Product for Industrial Applications.
- Adjustable Light Load and Selectable Continuous Modes.
- Multifunctional Protection Circuits.
 - Thermal Shut down (TSD).
 - Under Voltage Lock Out (UVLO).
 - Over Current Protection (OCP).
 - Over Voltage Protection (OVP).
 - Short Circuit Protection (SCP).
- Adjustable Soft Start.
- Power Good Output.
- 200kHz to 500kHz Switching Frequency.

Key Specifications

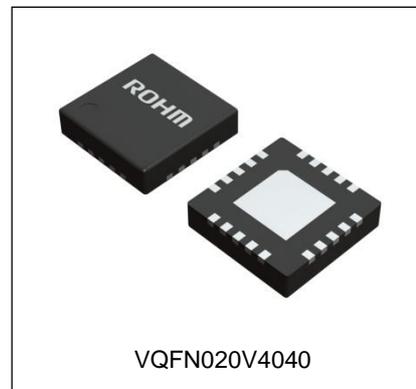
- VIN Input Voltage Range : 4.5V to 25V
- VCC Input Voltage Range : 4.5V to 5.5V
- VDD Input Voltage Range : 4.5V to 5.5V
- Output Voltage Range : 0.75V to 2.0V
- Standby Current : 0μA (Typ)
- Operating Temperature Range : -10°C to +85°C

Package

VQFN020V4040

W(Typ) x D(Typ) x H(Max)

4.00mm x 4.00mm x 1.00mm



VQFN020V4040

Applications

- FPGA, POL application.
- Mobile PC, Desktop PC, LCD-TV, Digital Components etc.
- Industrial Equipment.

Typical Application Circuit

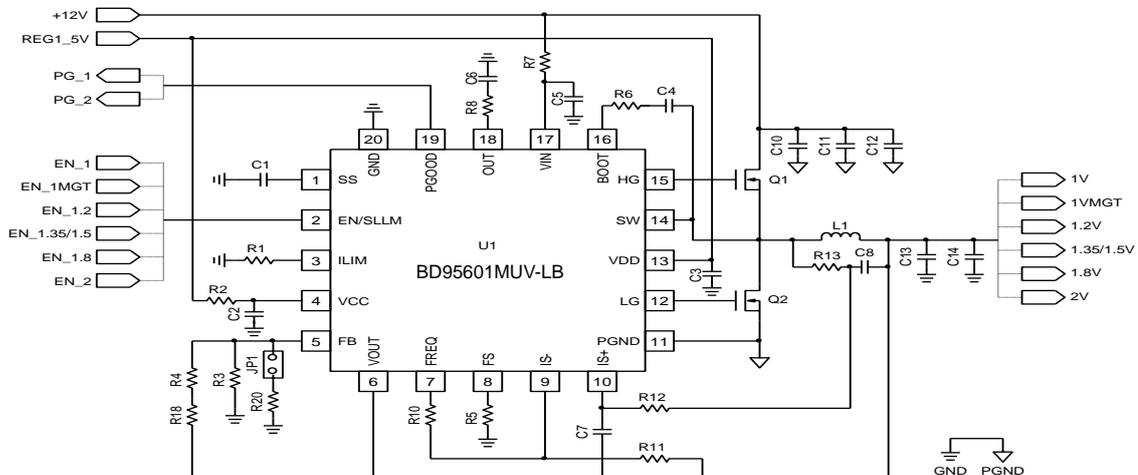


Figure 1. Application Circuit

Pin Configuration

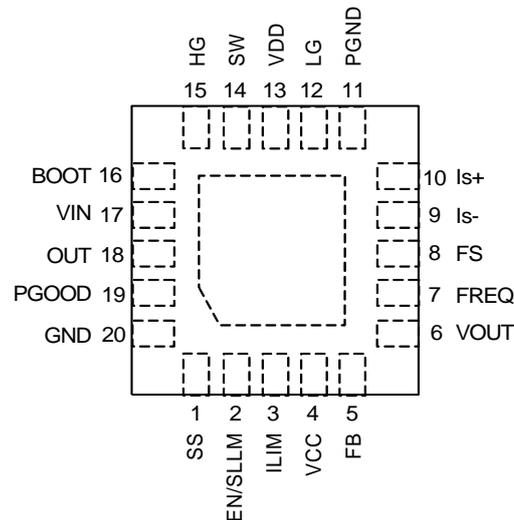


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	SS	Soft Start Time input. The rise time is set by a capacitor connected between SS and ground. At startup, a fixed current flows into the SS capacitor. Output voltage is controlled until the SS input reaches the reference voltage of 0.75V.
2	EN/SLLM	Enable and Mode Selection Input. Voltage on this input selects the operating mode. Standby Mode: < 0.8V Continuous Mode: 2.3V – 3.8V Light Load Mode: 4.2V – 5.5V
3	ILIM	Coil Current Limit input. A 100KΩ resistor should be connected between this input and ground.
4	VCC	IC Internal Circuits Power input.
5	FB	Output Voltage Sense input. A resistor divider to this input sets the output voltage.
6	VOUT	Output Voltage Monitor input.
7	FREQ	Current Sense Amplifier Output.
8	FS	Frequency input. A resistor sets the switching frequency. The frequency can be set from 200kHz to 500kHz.
9	Is-	Input Current Sense Amplifier input. FREQ pin is output.
10	Is+	Output Current Sense Amplifier input. If the voltage between this pin and VOUT pin reaches the specified voltage level (setting at ILIM pin), the switching is turned OFF.
11	PGND	Ground pin for Low-side FET driver.
12	LG	This is the pin to drive the gate of the Low-side FET. This voltage swings between VDD and PGND. High-speed gate driving for the Low-side FET is achieved using an output MOS (3Ω when LG is high, 0.5Ω when LG is low.).
13	VDD	This is the power supply pin to drive the Low-side FET. It is recommended that 10μF bypass capacitor be used to compensate for peak current during the FET on/off transition.
14	SW	This is the ground pin for High-side FET. The maximum absolute rating is 30V from ground.
15	HG	This is the pin to drive the gate of the High-side FET. The status of the switching swings between BOOT and SW. High-speed gate driving for High-side FET is achieved using an output MOS (3Ω when HG is high, 2Ω when HG is low).
16	BOOT	This is the power supply pin to drive the High-side FET. The maximum absolute ratings are 35V from ground and 7V from SW. The switching waveform sweeps from (VIN+VDD) to VDD by BOOT operation.
17	VIN	This is the pin for H ³ Reg™ control. It determines necessary on-time by monitoring input voltage. It is recommended to connect 1kΩ / 0.1μF CR filter.
18	OUT	This is the output pin of output voltage control amp. Please connect a resistor and capacitor to ground in series. It is recommended that a 0.01μF capacitor be established in normal operation.
19	PGOOD	Power Good output. This pin outputs a high-level when the FB pin voltage is above 63% of the reference voltage. This is an open drain pin and therefore requires an external pull-up.
20	GND	Ground pin of control circuit. It is the same as FIN potential.
FIN	FIN	Backside thermal pad. Please connect to the Ground.

Block Diagram

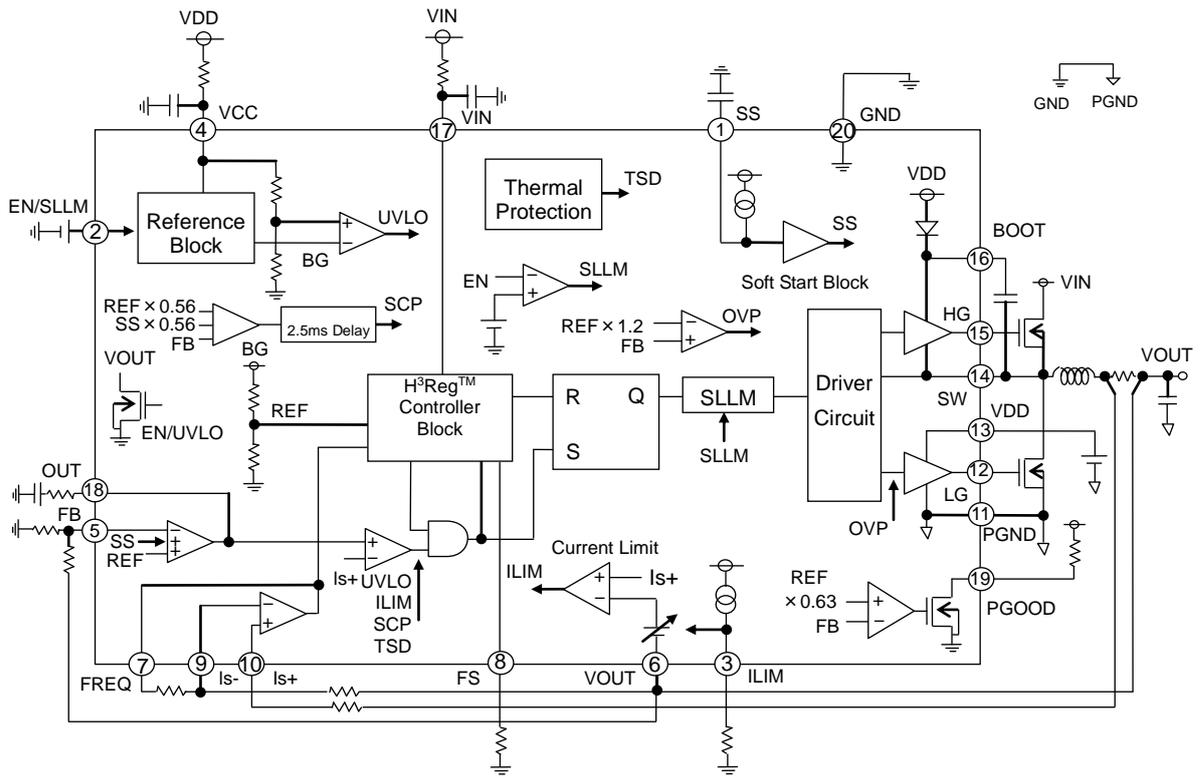


Figure 3. Block Diagram

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Condition
Input Voltage 1	V _{CC}	7	V	Note 1, Note 2
Input Voltage 2	V _{DD}	7	V	Note 1, Note 2
Input Voltage 3	V _{IN}	28	V	Note 1, Note 2
BOOT Voltage	BOOT	35	V	Note 1, Note 2
BOOT-SW Voltage	BOOT-SW	7	V	Note 1, Note 2
HG-SW Voltage	HG-SW	7	V	Note 1, Note 2
LG Voltage	LG	V _{DD}	V	
Output Voltage	V _{OUT} /I _{S+} /I _{S-}	V _{CC}	V	
EN Input Voltage	EN	7	V	Note 1
Power Dissipation 1	Pd1	0.34	W	Note 3
Power Dissipation 2	Pd2	0.70	W	Note 4
Power Dissipation 3	Pd3	2.20	W	Note 5
Power Dissipation 4	Pd4	3.56	W	Note 6
Operating Temperature Range	Topr	-10 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Maximum Junction Temperature	Tjmax	+150	°C	

(Note 1) Not to exceed Pd.

(Note 2) Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.

(Note 3) Derating in done 2.7 mW/°C for operating above Ta ≥ 25°C (when don't mounted on a heat radiation board).

(Note 4) Derating in done 5.6 mW/°C for operating above Ta ≥ 25°C (Mount on 1-layer 74.2mm x 74.2mm x 1.6mm board).
Surface heat dissipation copper foil:10.29mm².

(Note 5) Derating in done 17.6 mW/°C for operating above Ta ≥ 25°C (Mount on 4-layer 74.2mm x 74.2mm x 1.6mm board
Two sides heat dissipation copperfoil:10.29mm². 2 or 3-layer : heat dissipation copper foil : 5505mm²).

(Note 6) Derating in done 28.5 mW/°C for operating above Ta ≥ 25°C (Mount on 4-layer 74.2mm x 74.2mm x 1.6mm board)
All layers heat dissipation copper foil:5505mm².

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= 25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input Voltage 1	V _{CC}	4.5	-	5.5	V	
Input Voltage 2	V _{DD}	4.5	-	5.5	V	
Input Voltage 3	V _{IN}	4.5	-	25	V	
BOOT Voltage	BOOT	4.5	-	30	V	
SW Voltage	SW	-0.7	-	25	V	
BOOT-SW Voltage	BOOT-SW	4.5	-	5.5	V	
EN Input Voltage	EN	0	-	5.5	V	
I _S Input Voltage	I _{S+} /I _{S-}	0.7	-	2.7	V	
MIN ON Time	TONMIN	-	-	80	ns	

Electrical Characteristics

(Unless otherwise specified VCC=5V VDD=5V EN=3V VIN=12V VOUT=1.05V RFS=36kΩ Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Whole Device						
VCC Bias Current	I _{CC}	-	1500	1800	μA	
VCC Stand-by Current	I _{CCSTB}	-	0	10	μA	EN= 0V
VIN Bias Current	I _{IN}	-	30	80	μA	
VIN Stand-by Current	I _{INSTB}	-	0	10	μA	EN= 0V
EN Low Voltage	EN _{LOW}	GND	-	0.8	V	
EN High Voltage (Forced Continuous Mode)	EN _{HIGH_CON}	2.3	-	3.8	V	
EN High Voltage (SLLM Mode)	EN _{HIGH_SLLM}	4.5	-	5.5	V	
EN Bias Current	I _{EN}	-	15	25	μA	EN= 3V
Under Voltage Locked Out						
VCC Threshold Voltage	V _{CC_UVLO}	3.7	4.0	4.2	V	VCC:Sweep up
VCC Hysteresis Voltage	dV _{CC_UVLO}	100	160	220	mV	VCC:Sweep down
H ³ Reg™ Control						
ON Time	T _{ON}	194	219	244	ns	
MAX ON Time	T _{ONMAX}	-	3.5	-	μs	
MIN OFF Time	T _{OFFMIN}	-	490	700	ns	
FET Driver						
HG High-side ON Resistance	HGHON	-	3.0	6.0	Ω	
HG Low-side ON Resistance	HGLON	-	2.0	4.0	Ω	
LG High-side ON Resistance	LGHON	-	3.0	6.0	Ω	
LG Low-side ON Resistance	LGLON	-	0.5	1.0	Ω	
SCP						
SCP Start-up Voltage	V _{SCP}	0.345	0.420	0.495	V	
SCP Delay Time	T _{SCP}	-	2.5	-	ms	
OVP						
FB Threshold Voltage	V _{OVP}	0.825	0.900	0.975	V	
Soft Start						
Charge Current	I _{SS}	1	2	3	μA	
Stand-by Voltage	V _{SS_STB}	-	-	50	mV	
Current Limit						
Setting Current	I _{LIM}	-	10	-	μA	
Current Limit Threshold Voltage	V _{LIM}	75	100	120	mV	R _{LIM} = 100kΩ
Output Voltage Sense						
Output Reference Voltage 1	REF1	0.743	0.750	0.757	V	
Is+ Input Voltage	I _{S+}	-1	0	1	μA	LS+= 1.05V
Is- Input Voltage	I _{S-}	-1	0	1	μA	LS-= 1.05V
POWER GOOD						
FB Power Good Voltage	V _{PGOOD}	0.38	0.47	0.56	V	
Discharge ON Resistance	R _{ONPGOOD}	-	50	150	Ω	
Diode for BOOT						
V _F Voltage	V _F	0.4	0.5	0.6	V	I _F = 1mA

Typical Performance Curves (Reference data)

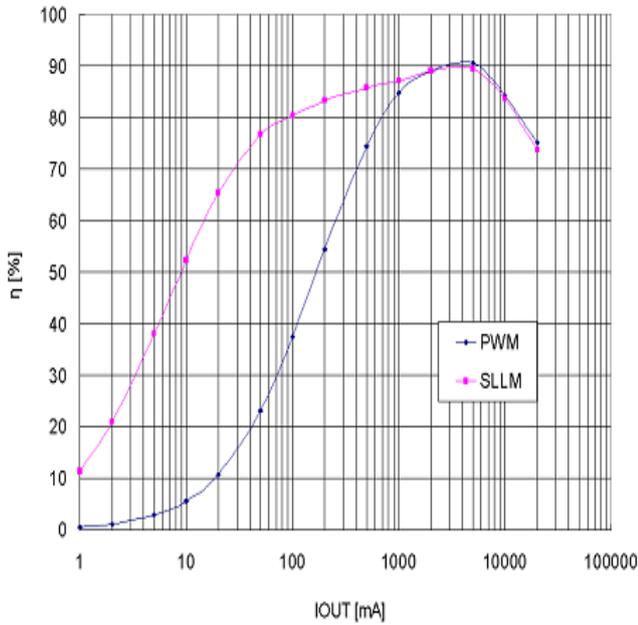


Figure 4. Efficiency ($V_{IN}=7.5V$)

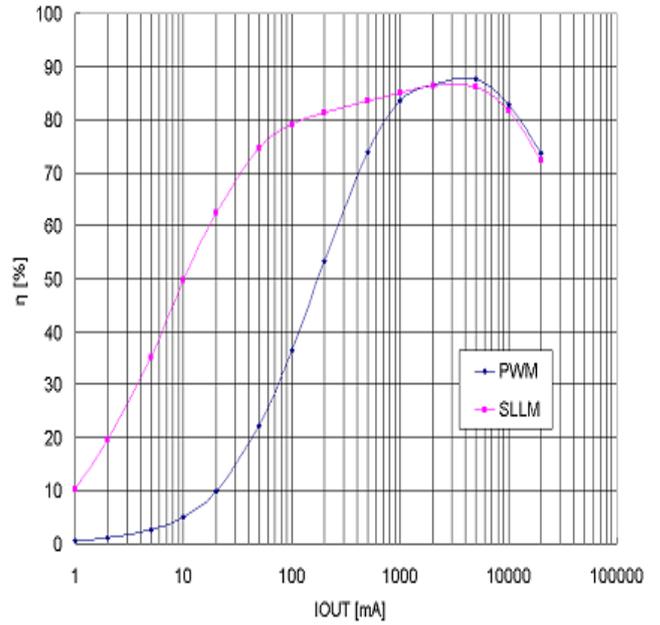


Figure 5. Efficiency ($V_{IN}=12V$)

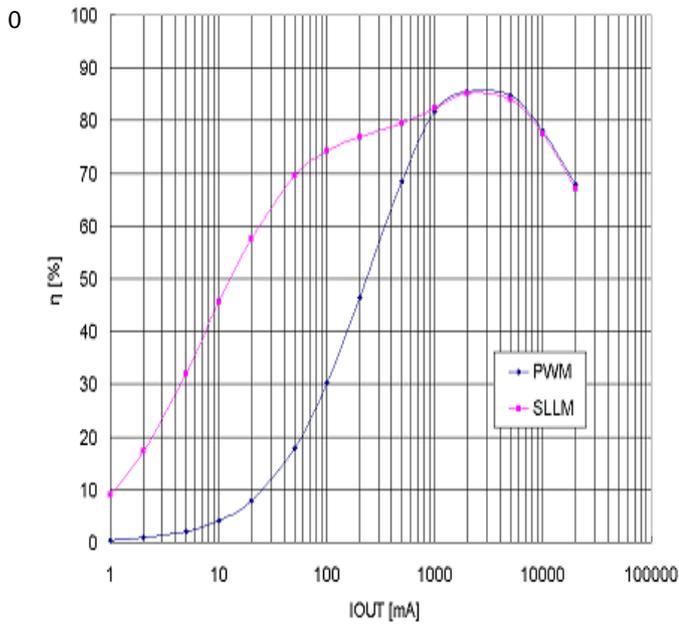


Figure 6. Efficiency ($V_{IN}=21V$)

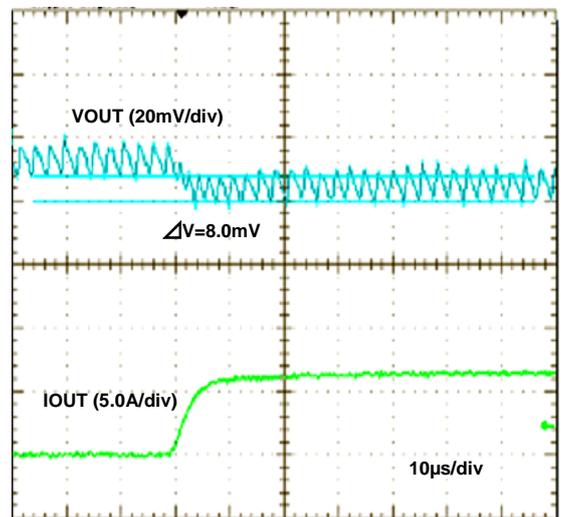


Figure 7. Transient Response Waveform ($V_{IN}=5V$)

Typical Performance Curves (Reference data) - continued

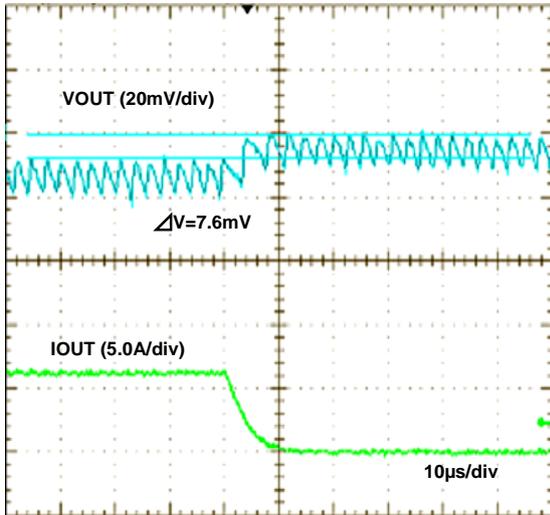


Figure 8. Transient Response Waveform ($V_{IN} = 5\text{V}$)

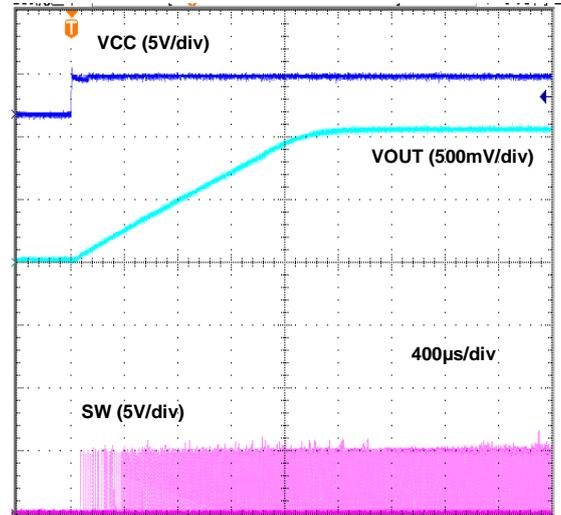


Figure 9. Power-up with VCC

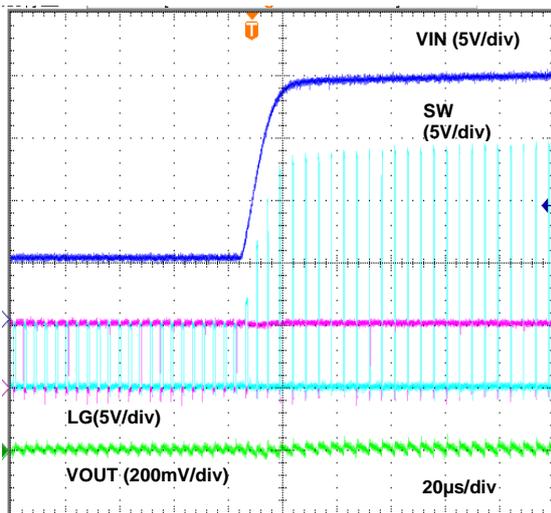


Figure 10. Line Regulation

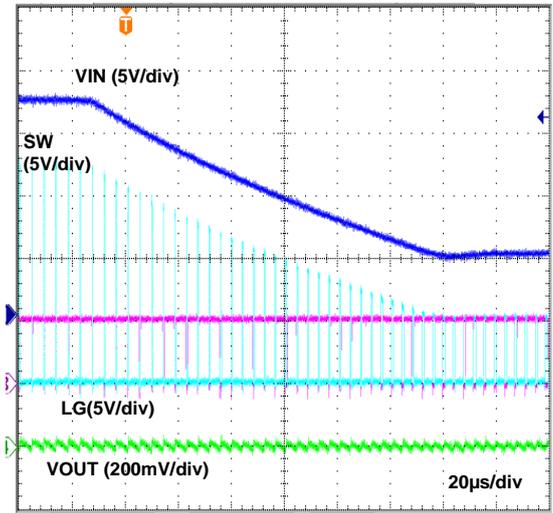


Figure 11. Line Regulation

Typical Performance Curves (Reference data) - continued

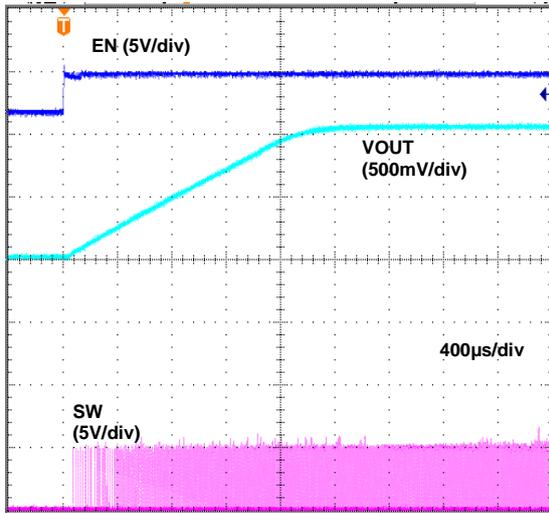


Figure 12. Power-up with EN

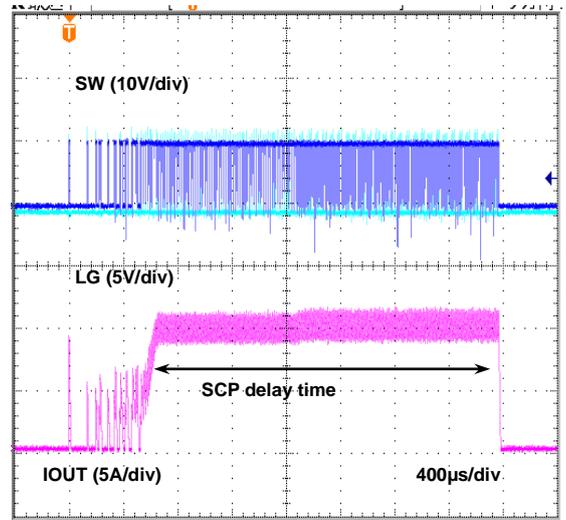


Figure 13. OCP & SCP

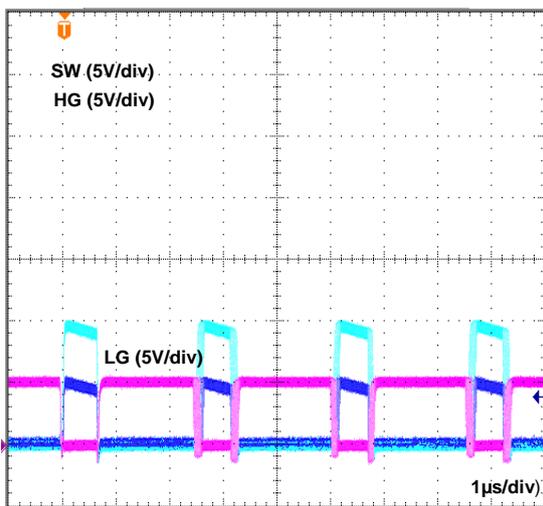


Figure 14. Switching Waveform ($V_{IN}=5V$, $I_{OUT}=18A$)

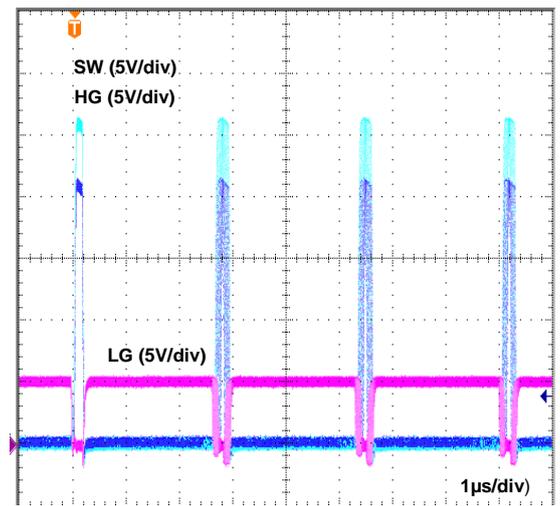


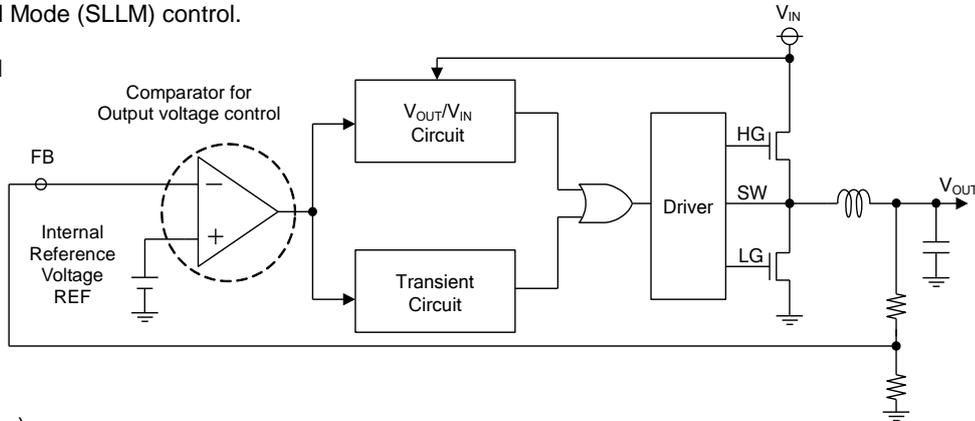
Figure 15. Switching Waveform ($V_{IN}=21V$, $I_{OUT}=18A$)

Description of Blocks

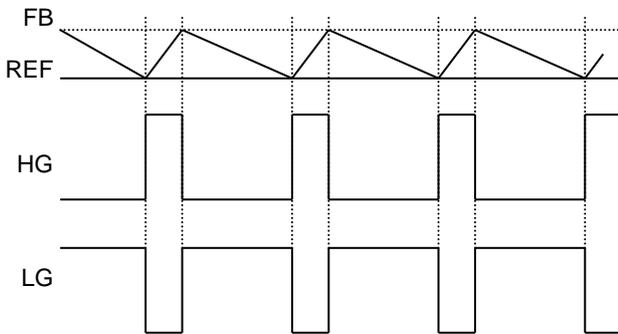
BD95601MUV-LB is a single channel synchronous buck regulator using H³Reg™, Rohm's latest constant on-time controller technology. Fast load response is achieved by controlling the output voltage using a comparator without relying on the switching frequency.

When V_{OUT} drops due to a rapid load change, the system quickly restores V_{OUT} by extending the t_{ON} time interval. Thus, it serves to improve the regulator's transient response. Activating the light load mode further increases efficiency by using Simple Light Load Mode (SLLM) control.

H³Reg™ Control



(Normal operation)

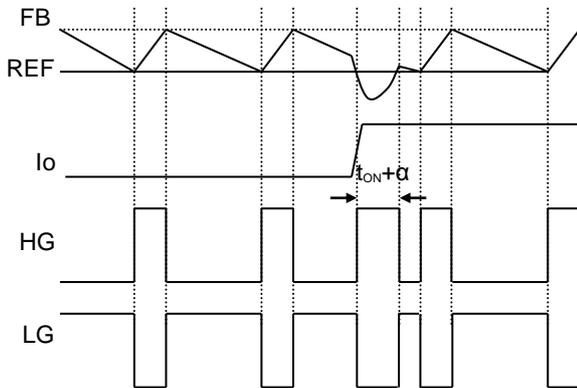


When FB falls to a reference voltage (REF), the drop is detected, activating the H³Reg™ control system

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \text{ [sec]} \dots (1)$$

HG output on-time is determined by the formula (1). When HG is off, LG is on until the output voltage becomes FB= REF.

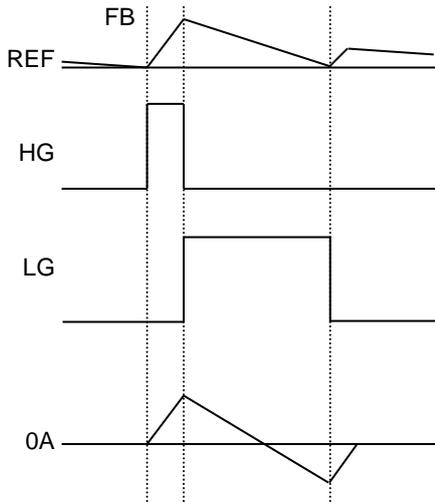
(V_{OUT} drops due to a rapid load change)



When V_{OUT} drops due to a rapid load change, and the voltage remains below the output setting following the programmed t_{ON} time, the system quickly restores V_{OUT} by extending the t_{ON} time, thus improving the transient response. Once V_{OUT} is restored, the controller continues normal operation.

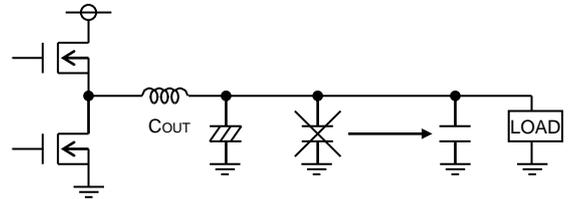
Description of Blocks - continued

(Light Load Control)



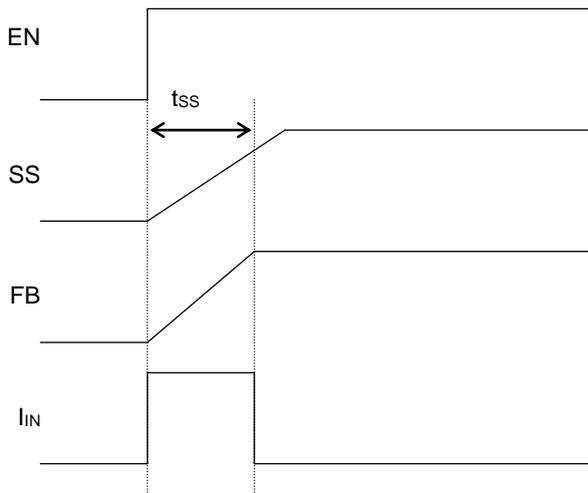
In SLLM (EN/SLLM = 4.5V to 5.5V), SLLM function will operate when the LG pin is off and the coil current is lower than 0A (the current goes from V_{OUT} to SW). When the FB input is lower than REF voltage again, HG will be enabled once again.

*Attention: To affect the rapid transient response, the H³Reg™ control monitors the current from the output capacitor to the load using the ESR of the output capacitor. Do not use ceramic capacitors on C_{OUT} side of power supply. Ceramic bypass capacitors can be used near the individual loads if desired.



Timing Chart

Soft-start function



The Soft start function is exercised when the EN/SLLM input is set to high. Current control takes effect at startup enabling a moderate output voltage “ramping.” Soft start timing and incoming current are calculated with the following formulas (2) and (3) below.

Soft start time

$$t_{ss} = \frac{0.75(\text{Typ}) \times C_{SS}}{2\mu\text{A}(\text{Typ})} \text{ [sec]} \dots (2)$$

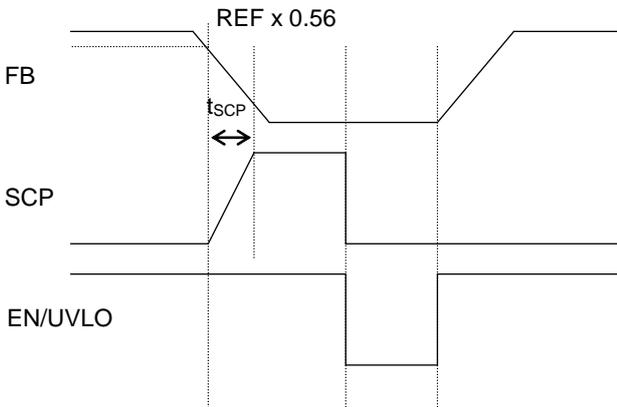
C _{SS} (pF)	Soft start time(ms)
12000	5
27000	10
51000	20

Inrush current

$$I_{IN} = \frac{C_o \times V_{OUT}}{t_{ss}} \times \frac{V_{OUT}}{V_{IN}} \text{ [A]} \dots (3)$$

(C_{SS}: Soft start capacitor C_o: Output capacitor)

Timer Latch Type Short Circuit Protection



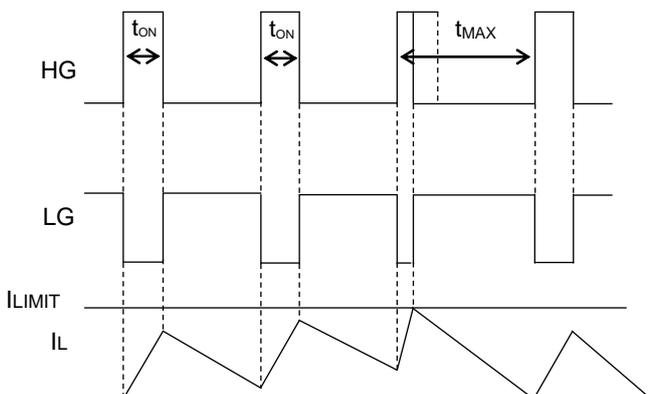
Short circuit protection is enabled when FB falls to or below REF X 0.56.

Once the programmed time period has elapsed, the output is latched off to prevent destruction of the circuit.

Output voltage can be restored either by cycling the EN pin or disabling UVLO.

Short circuit protection time is programmed at 2.5msec (Typ).

Over Current Voltage Protection

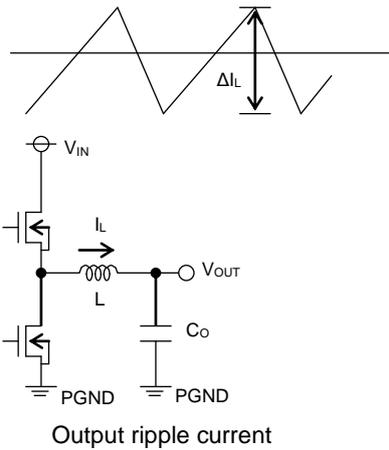


During normal operation, if FB is less than REF, HG is high during the time t_{ON}, but when the coil current exceeds the I_{LIMIT} threshold, HG is set to off.

The next pulse returns to normal operation if the output voltage drops after the maximum on-time or I_L becomes lower than I_{LIMIT}.

Selection of Components Externally Connected

1. Inductor (L) Selection



The inductor value is a major influence on the output ripple current. As formula (4) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} [A] \dots (4)$$

Generally, lower inductance values offer faster response times but also result in increased output ripple and lower efficiency.

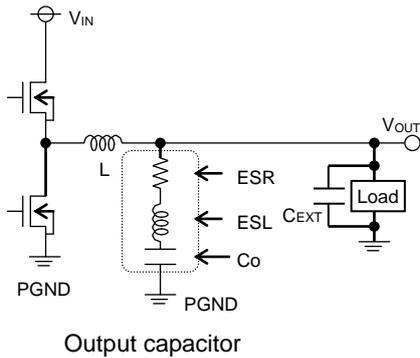
0.47μH to 2.2μH are a recommended range of values.

The peak current rating of the coil is approximated by formula (5). Please select an inductor equal to or higher than this value.

$$I_{LPEAK} = I_{OUTMAX} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times V_{IN} \times f} [A] \dots (5)$$

- *Passing a current larger than inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. When selecting the inductor, be sure to allow enough margin to assure that peak currents do not exceed the inductor rated current value.
- *To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2. Output Capacitor (Co) Selection



The output capacitor should be determined by equivalent series resistance and equivalent series inductance so that the output ripple voltage is 30mV or more. The rating of the capacitor is set with sufficient margin given the output voltage.

$$\Delta V_{OUT} = ESR \times \Delta I_L + ESL \times \Delta I_L / t_{ON} \dots (6)$$

- ΔIL: Output ripple current
- ESR: Equivalent series resistance,
- ESL: Equivalent series inductance

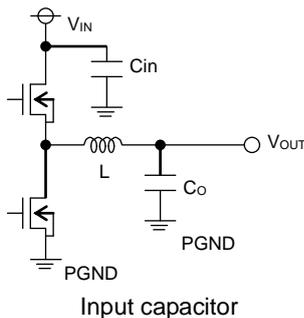
Please give due consideration to the conditions in formula (7) below for the output capacitor, bearing in mind that the output start-up time must be established within the soft start timeframe. Capacitors used as bypass capacitors are connected to the load side affect the overall output capacitance (CEXT, figure above). Please set the soft start time or over-current detection value, regarding these capacities.

$$C_O + C_{EXT} \leq \frac{t_{SS} \times (Limit - I_{OUT})}{V_{OUT}} \dots (7)$$

t_{SS}: Soft start time
Limit: Over current detection

If an inappropriate capacitor is used, OCP may be detected during activation and may cause startup malfunctions.

3. Input Capacitor (Cin) Selection



The input capacitor selected must have low enough ESR to fully support high output ripple so as to prevent extreme over current conditions. The formula for ripple current IRMS is given in (8) below.

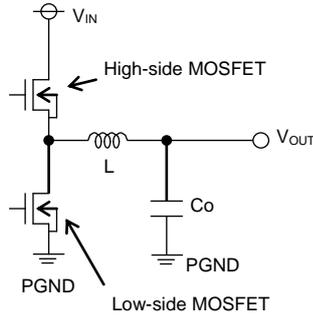
$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} (V_{IN} - V_{OUT})}}{V_{IN}} [A] \dots (8)$$

Where $V_{IN} = 2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A ceramic capacitor is recommended to reduce ESR loss and maximize efficiency.

Selection of Components Externally Connected - continued

4. MOSFET selection



The High-side and Low-side drivers are designed to activate N channel MOSFETs having low on-resistance. The chosen MOSFET may result in the loss described below, please select a proper FET for each considering the input-output and load current.

< Loss of High-side MOSFET >

$$P_{High-side} = P_{RON} + P_{TRAN}$$

$$= \frac{V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + \frac{(Tr+Tf) \times V_{IN} \times I_{OUT} \times f}{6} \dots (9)$$

(Ron: On-resistance of FET, f: Switching frequency, Tr: Rise time, Tf: Fall time)

< Loss of High-side MOSFET >

$$P_{Low-side} = P_{RON}$$

$$= \frac{V_{IN} - V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 \dots (10)$$

The High-side MOSFET generates loss when switching, along with the loss due to on-resistance. Good efficiency is achieved by selecting a MOSFET with low on-resistance and low Qg (gate total charge amount). Recommended MOSFETs for various current values are as follows:

Output current	High-side MOSFET	Low-side MOSFET
to 5A	RQ3E080GN	RQ3E080GN
5 to 8A	RQ3E120GN	RQ3E150GN
8 to 10A	RQ3E150GN	RQ3E180GN

5. Set Point Output Voltage

This IC operates such that output voltage is REF = FB.

<Output Voltage>

$$V_{OUT} = \frac{(R1+R2)}{R2} \times REF(0.75V)$$

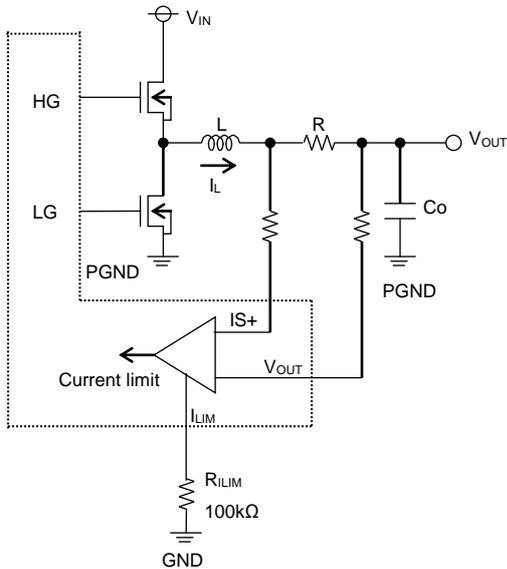
Setting resistance are selected from 10kΩ to 50kΩ, because of external Noise resistant and feedback current. Please refer to constant the following for typical output voltage.

Output voltage	R1	R2
1.0V	10kΩ	30kΩ
1.2V	18kΩ+1.8kΩ	33kΩ
1.35V	24kΩ	30kΩ
1.5V	24kΩ	12kΩ(30kΩ//20kΩ)
1.8V	39kΩ+3kΩ	30kΩ
2.0V	36kΩ+0.68kΩ	22kΩ

Selection of Components Externally Connected - continued

6. Selecting resistance for over current setting

(A) High-precision current detection circuit (use a low value resistor)

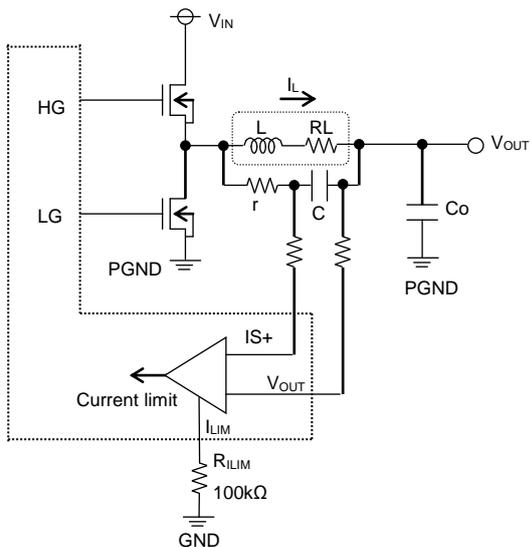


$$I_{LIMIT} = \frac{0.1}{R} \quad [A] \dots (11)$$

(R: Detection resistor)

Please make sure that 100kΩ is used for R_{ILIM}.

(B) Low loss current detection circuit (Use DCR of L)



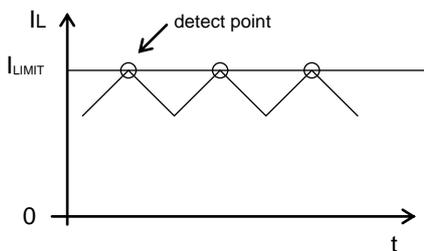
$$I_{LIMIT} = 0.1 \times \frac{r \times C}{L} \quad [A] \dots (12)$$

$$\text{However, } RL = \frac{L}{r \times C}$$

(RL: DCR value of inductor)

Must be adjusted so that the power dissipation into the r. About 47kΩ to 330kΩ.

Please make sure that 100kΩ is used for R_{ILIM}.



As shown in the diagram to the left, if the voltage between IS+ and V_{OUT} exceed the I_{LIMIT}, the High-side FET gate is set low. Because the peak value of inductor current is detected and corresponds to the saturation time of inductor, the reliability of the system is improved.

Application Example

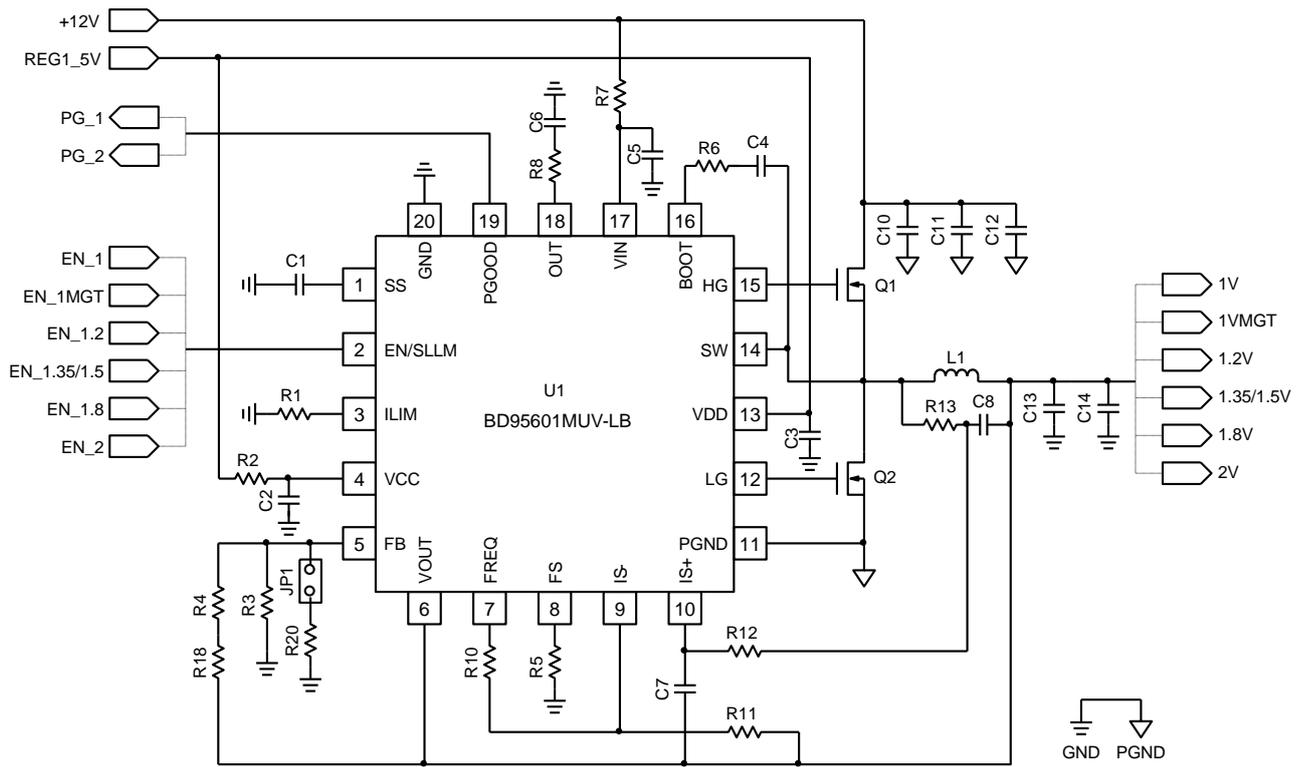


Figure 16. BD95601MUV-LB Basic Application Circuit

Bills of Materials

Reference Designator	Type	Value	Description	Manufacturer Part Number	Manufacturer	Configuration (mm)
C1	Ceramic Capacitor	0.022µF	25V, X7R, ±10%	GRM155R71E223KA61	MURATA	1005
C2	Ceramic Capacitor	1µF	10V, X5R, ±10%	GRM188R61A105KA61	MURATA	1608
C3	Ceramic Capacitor	10µF	25V, X5R, ±10%	GRM32DR61E106KA12	MURATA	3225
C4	Ceramic Capacitor	0.47µF	10V, X5R, ±10%	GRM188R61A474KA61	MURATA	1608
C5, C6	Ceramic Capacitor	0.01µF	25V, X7R, ±10%	GRM155R71E103KA01	MURATA	1005
C7	Ceramic Capacitor	10pF	50V, CH, ±5%	GRM1552C1H100JA01	MURATA	1005
C8	Ceramic Capacitor	1000pF	50V, X5R, ±10%	GRM155R61H102KA01	MURATA	1005
C10	Ceramic Capacitor	0.1µF	50V, X5R, ±10%	GRM155R61E104KA87	MURATA	1005
C11, C12	Ceramic Capacitor	10µF	35V, X5R, ±10%	GRM32ER6YA106KA12	MURATA	3225
L1	Inductor	0.56µH	±20%, 14.2A(L=-20%), DCR=3.2mΩmax	FDU0650-H-R56M	TOKO	7667
Q1	MOSFET	-	N-ch, Vdss 30V, Id 15A, Ron 4.7mΩ	RQ3E150GN	ROHM	3333
Q2	MOSFET	-	N-ch, Vdss 30V, Id 18A, Ron 3.3mΩ	RQ3E180GN	ROHM	3333
R1	Resistor	100kΩ	1/16W, 50V, 5%	MCR01MZPJ104	ROHM	1005
R2	Resistor	10Ω	1/16W, 50V, 5%	MCR01MZPJ100	ROHM	1005
R5	Resistor	36kΩ	1/16W, 50V, 5%	MCR01MZPJ363	ROHM	1005
R6	Resistor	3.3Ω	1/16W, 50V, 5%	MCR01MZPJ3R3	ROHM	1005
R7	Resistor	1kΩ	1/16W, 50V, 5%	MCR01MZPJ102	ROHM	1005
R8	Resistor	2.7kΩ	1/16W, 50V, 5%	MCR01MZPJ272	ROHM	1005
R10	Resistor	510Ω	1/16W, 50V, 5%	MCR01MZPJ511	ROHM	1005
R11, R12	Resistor	100Ω	1/16W, 50V, 5%	MCR01MZPJ101	ROHM	1005
R13	Resistor	100kΩ	1/16W, 50V, 5%	MCR01MZPJ104	ROHM	1005
U1	IC	-	Buck DC/DC Controller	BD95601MUV-LB	ROHM	VQFN020V4040

VOUT=1.0V, IOU=6A

Reference Designator	Type	Value	Description	Manufacturer Part Number	Manufacturer	Configuration (mm)
C13, C14	POSCAP	470 μ F	2.5V, \pm 20%, ESR 6m Ω max	2R5TPF470M6L	SANYO	7343
JP1	Jumper	n/a	Not applicable	-	-	-
R3	Resistor	30k Ω	1/16W, 50V, 0.5%	MCR01MZPD3002	ROHM	1005
R4	Resistor	10k Ω	1/16W, 50V, 0.5%	MCR01MZPD1002	ROHM	1005
R18	Resistor	0 Ω	Jumper, 1A, 50m Ω max	MCR01MZPJ000	ROHM	1005
R20	Resistor	n/a	Not applicable	-	-	-

VOUT=1.2V, IOU=4A

Reference Designator	Type	Value	Description	Manufacturer Part Number	Manufacturer	Configuration (mm)
C13, C14	POSCAP	470 μ F	2.5V, \pm 20%, ESR 6m Ω max	2R5TPF470M6L	SANYO	7343
JP1	Jumper	n/a	Not applicable	-	-	-
R3	Resistor	30k Ω	1/16W, 50V, 0.5%	MCR01MZPD3002	ROHM	1005
R4	Resistor	18k Ω	1/16W, 50V, 0.5%	MCR01MZPD1802	ROHM	1005
R18	Resistor	0 Ω	Jumper, 1A, 50m Ω max	MCR01MZPJ000	ROHM	1005
R20	Resistor	n/a	Not applicable	-	-	-

VOUT=1.8V, IOU=6A

Reference Designator	Type	Value	Description	Manufacturer Part Number	Manufacturer	Configuration (mm)
C13, C14	POSCAP	470 μ F	2.5V, \pm 20%, ESR 6m Ω max	2R5TPF470M6L	SANYO	7343
JP1	Jumper	n/a	Not applicable	-	-	-
R3	Resistor	30k Ω	1/16W, 50V, 0.5%	MCR01MZPD3002	ROHM	1005
R4	Resistor	39k Ω	1/16W, 50V, 0.5%	MCR01MZPD3902	ROHM	1005
R18	Resistor	3k Ω	1/16W, 50V, 5%	MCR01MZPJ302	ROHM	1005
R20	Resistor	n/a	Not applicable	-	-	-

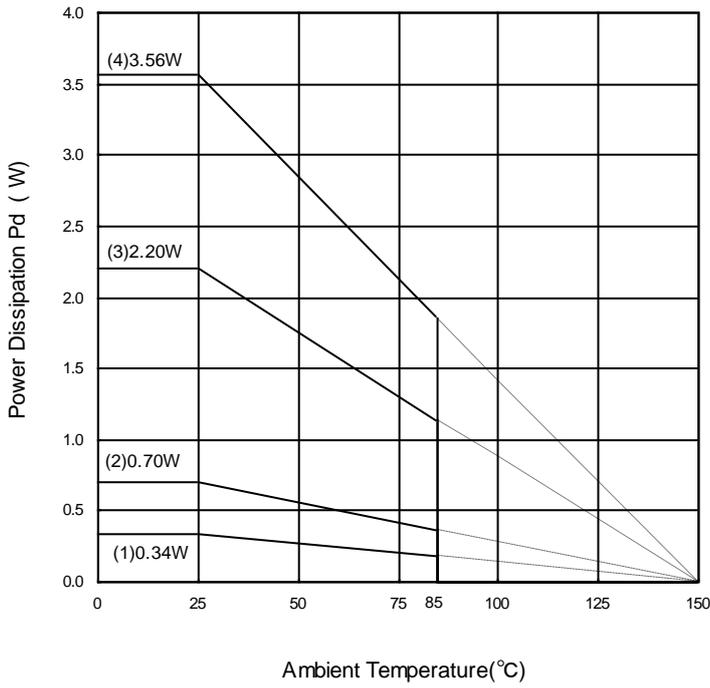
VOUT=1.35V, IOU=4A

Reference Designator	Type	Value	Description	Manufacturer Part Number	Manufacturer	Configuration (mm)
C13, C14	POSCAP	470 μ F	2.5V, \pm 20%, ESR 6m Ω max	2R5TPF470M6L	SANYO	7343
JP1	Jumper	-	0: 1.35V, 1: 1.5V	-	-	-
R3	Resistor	30k Ω	1/16W, 50V, 0.5%	MCR01MZPD3002	ROHM	1005
R4	Resistor	24k Ω	1/16W, 50V, 0.5%	MCR01MZPD2402	ROHM	1005
R18	Resistor	0 Ω	Jumper, 1A, 50m Ω max	MCR01MZPJ000	ROHM	1005
R20	Resistor	120k Ω	1/16W, 50V, 0.5%	MCR01MZPD1203	ROHM	1005

VOUT=2.0V, IOU=2A

Reference Designator	Type	Value	Description	Manufacturer Part Number	Manufacturer	Configuration (mm)
C13, C14	POSCAP	330 μ F	6.3V, \pm 20%, ESR 18m Ω max	6TPE330MIL	SANYO	7343
JP1	Jumper	n/a	Not applicable	-	-	-
R3	Resistor	18k Ω	1/16W, 50V, 0.5%	MCR01MZPD1802	ROHM	1005
R4	Resistor	30k Ω	1/16W, 50V, 0.5%	MCR01MZPD3002	ROHM	1005
R18	Resistor	0 Ω	Jumper, 1A, 50m Ω max	MCR01MZPJ000	ROHM	1005
R20	Resistor	n/a	Not applicable	-	-	-

Power Dissipation



PCB size: 74.2mm×74.2mm×1.6mm
 Substrate(1): IC only
 Substrate(2): 1-layer (copper foil density 0mm²)
 Substrate(3): 4-layer (copper foil density 10.29 mm²)
 2,3-layer (copper foil de density 5505mm²)
 Substrate(4): 4-layer (copper foil density 5505 mm²)

Substrate(1) : $\theta_{ja}=367.6^{\circ}\text{C/W}$
 Substrate(2) : $\theta_{ja}=178.6^{\circ}\text{C/W}$
 Substrate(3) : $\theta_{ja}=56.6^{\circ}\text{C/W}$
 Substrate(4) : $\theta_{ja}=35.1^{\circ}\text{C/W}$

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.
When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

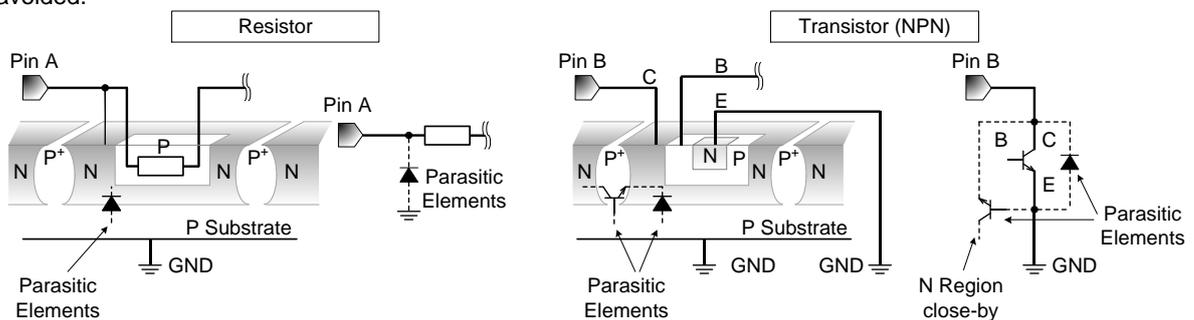


Figure 17. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

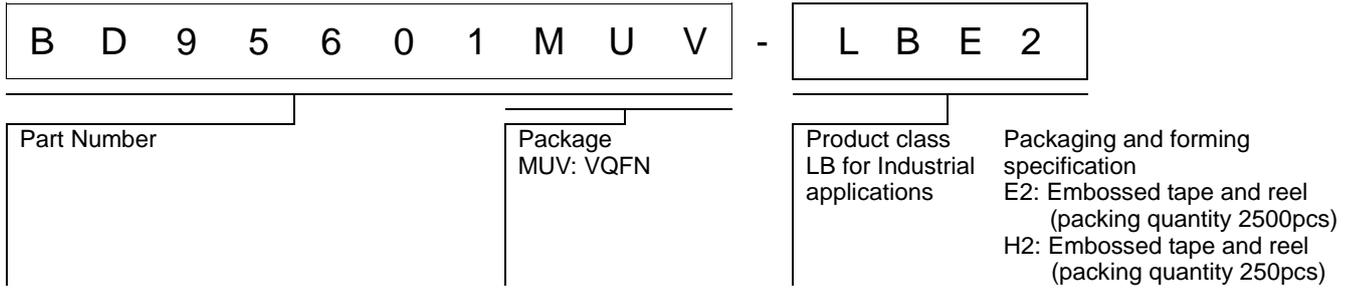
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

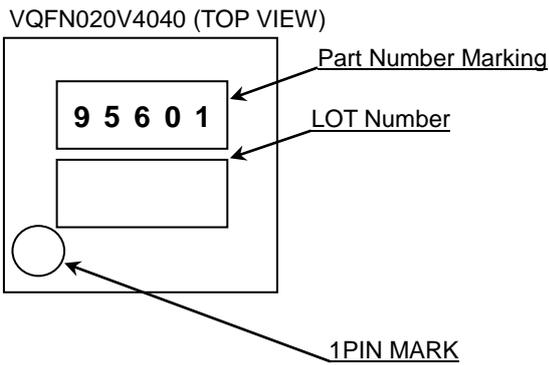
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information



Marking Diagrams



Revision History

Date	Revision	Changes
6.Sep.2013	001	New Release
1.Apr.2014	002	Delete sentence "and log life cycle" in General Description and Futures. Change "Packaging and forming specification" from E2 to H2.
02.Aug.2016	003	Modify some typo

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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