

RQK0204TGDQA

Silicon N Channel MOS FET
Power Switching

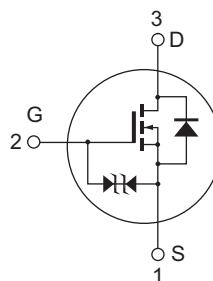
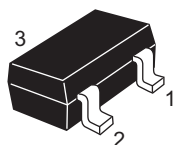
R07DS0304EJ0500
Rev.5.00
Jan 10, 2014

Features

- Low on-resistance
 $R_{DS(on)} = 100 \text{ m}\Omega$ typ ($V_{GS} = 4.5 \text{ V}$, $I_D = 1.2 \text{ A}$)
- Low drive current
- High speed switching
- 2.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is "TG".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	± 12	V
Drain current	I_D	2.3	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	8.0	A
Body - drain diode reverse drain current	I_{DR}	2.3	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4: 40 x 40 x 1 mm)

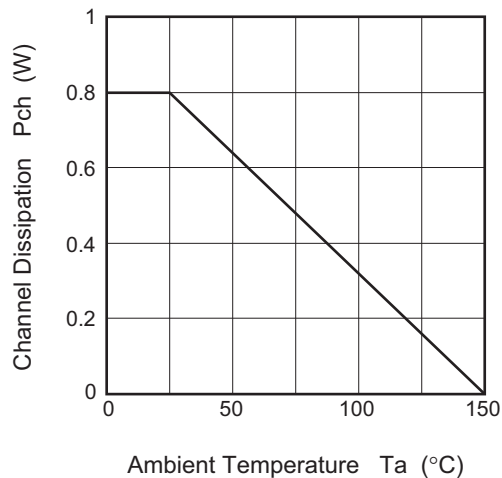
Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 12	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 10 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	1	μA	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	100	130	$\text{m}\Omega$	$I_D = 1.2 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	146	204	$\text{m}\Omega$	$I_D = 1.2 \text{ A}$, $V_{GS} = 2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	1.5	3.0	—	S	$I_D = 1.2 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	127	—	pF	$V_{DS} = 10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	33	—	pF	
Reverse transfer capacitance	C_{rss}	—	14	—	pF	
Turn - on delay time	$t_{d(on)}$	—	11	—	ns	$I_D = 1.2 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 8.3 \text{ }\Omega$ $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	28	—	ns	
Turn - off delay time	$t_{d(off)}$	—	24	—	ns	
Fall time	t_f	—	7	—	ns	
Total gate charge	Q_g	—	1.5	—	nC	$V_{DD} = 10 \text{ V}$ $V_{GS} = 5 \text{ V}$ $I_D = 2.3 \text{ A}$
Gate to source charge	Q_{gs}	—	0.3	—	nC	
Gate to drain charge	Q_{gd}	—	0.4	—	nC	
Body - drain diode forward voltage	V_{DF}	—	0.85	1.1	V	$I_F = 2.3 \text{ A}$, $V_{GS} = 0$ ^{Note3}

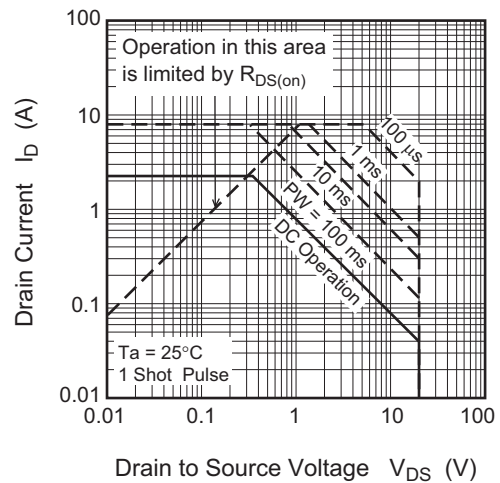
Notes: 3. Pulse test

Main Characteristics

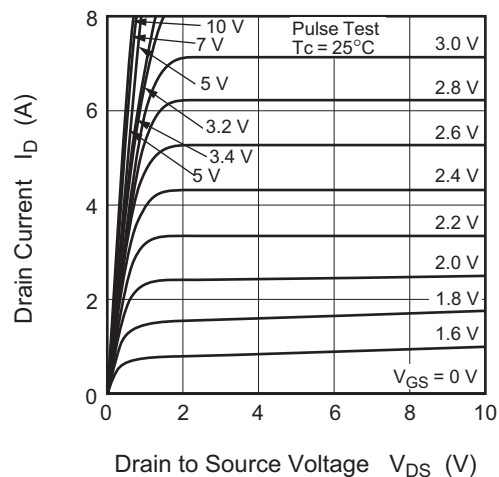
Maximum Channel Power
Dissipation Curve

*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

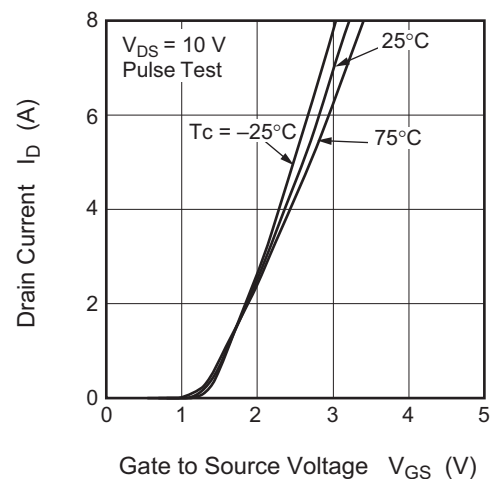
Maximum Safe Operation Area



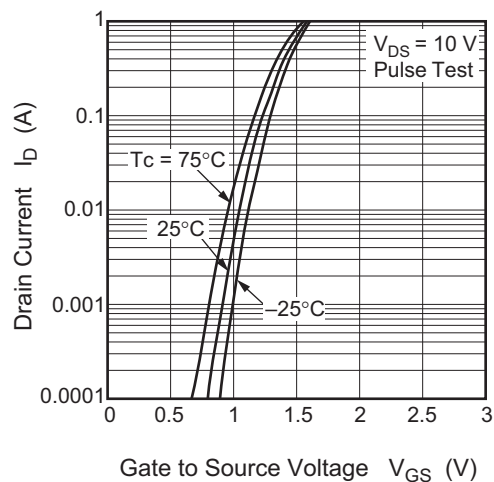
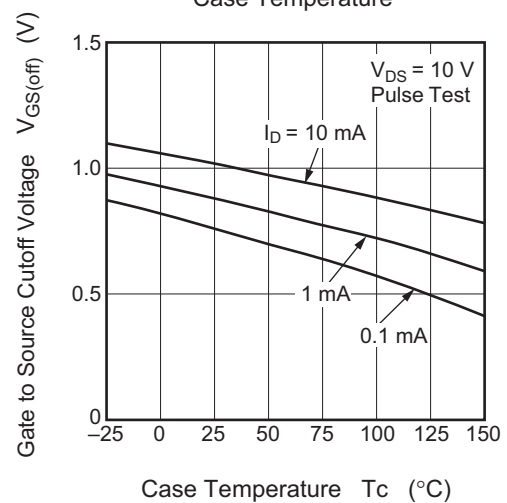
Typical Output Characteristics

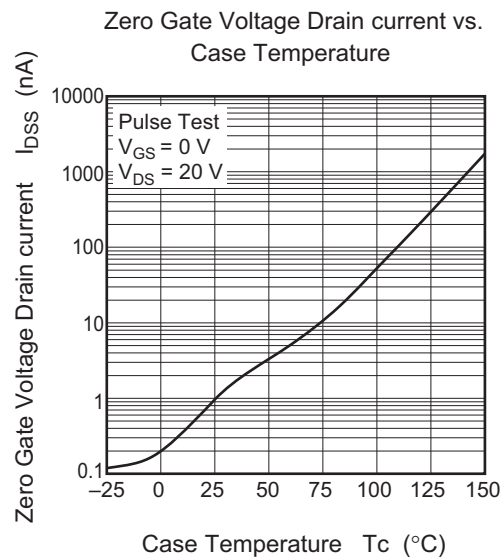
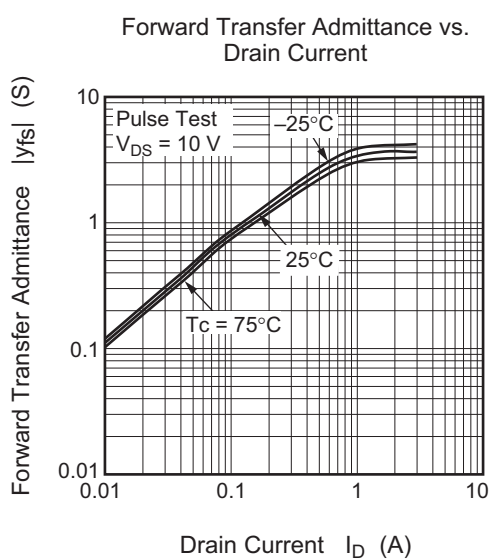
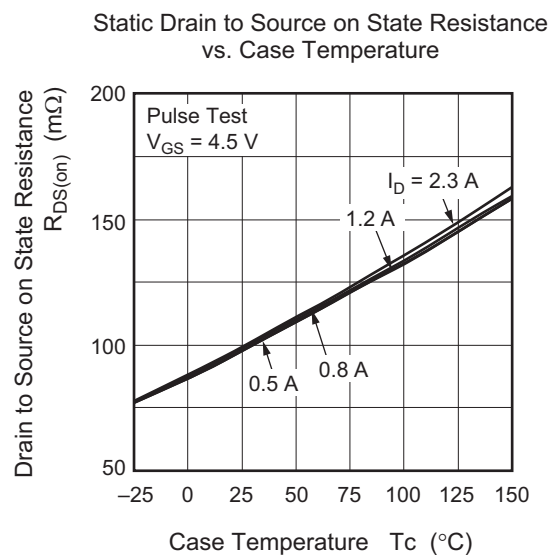
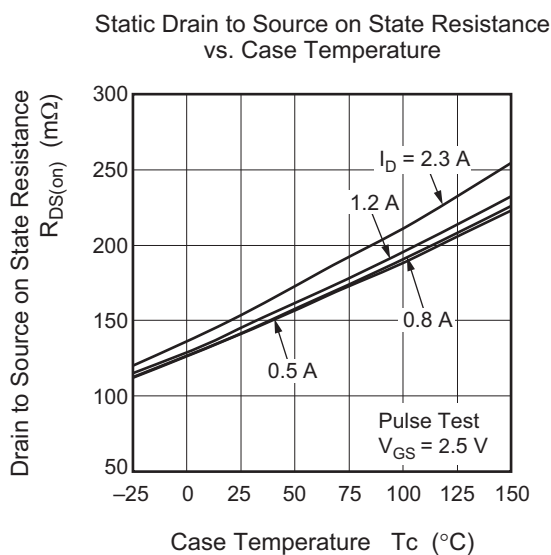
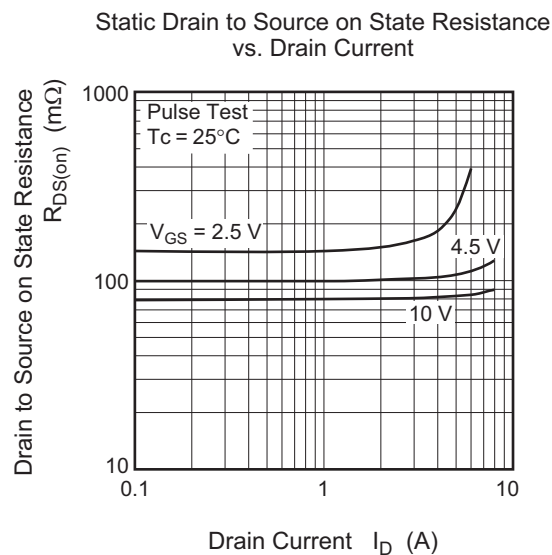
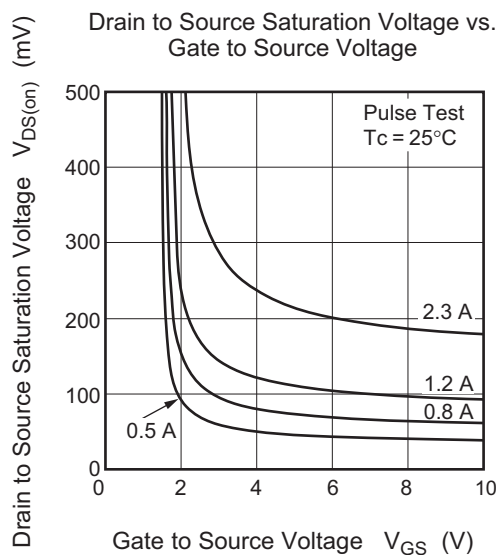


Typical Transfer Characteristics (1)

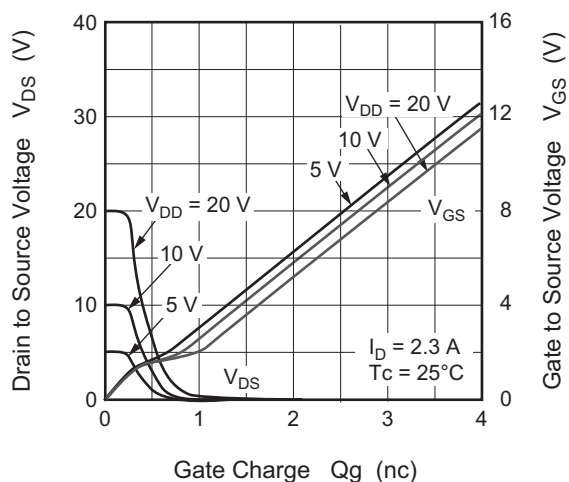


Typical Transfer Characteristics (2)

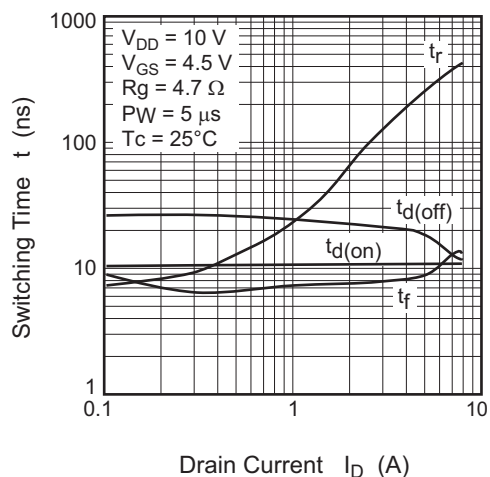
Gate to Source Cutoff Voltage vs.
Case Temperature



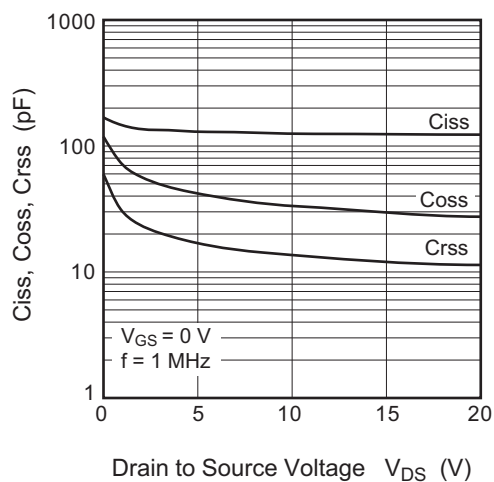
Dynamic Input Characteristics



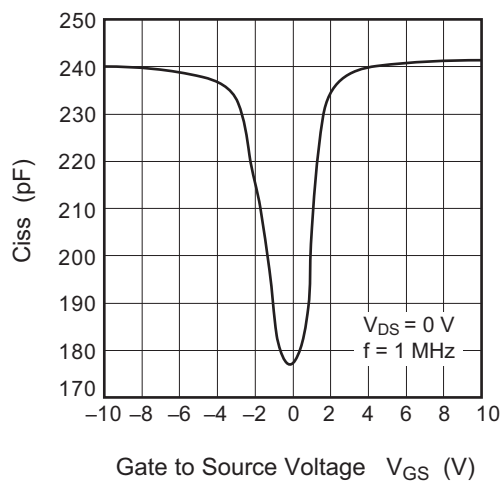
Switching Characteristics



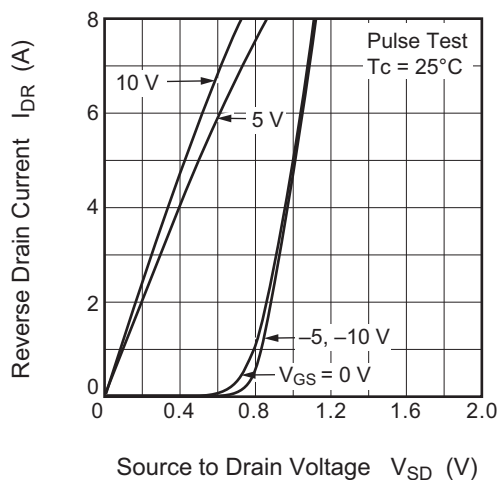
Typical Capacitance vs. Drain to Source Voltage



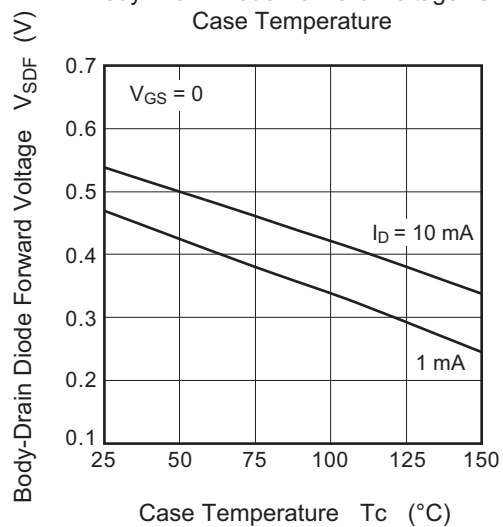
Input Capacitance vs. Gate to Source Voltage



Reverse Drain Current vs. Source to Drain Voltage

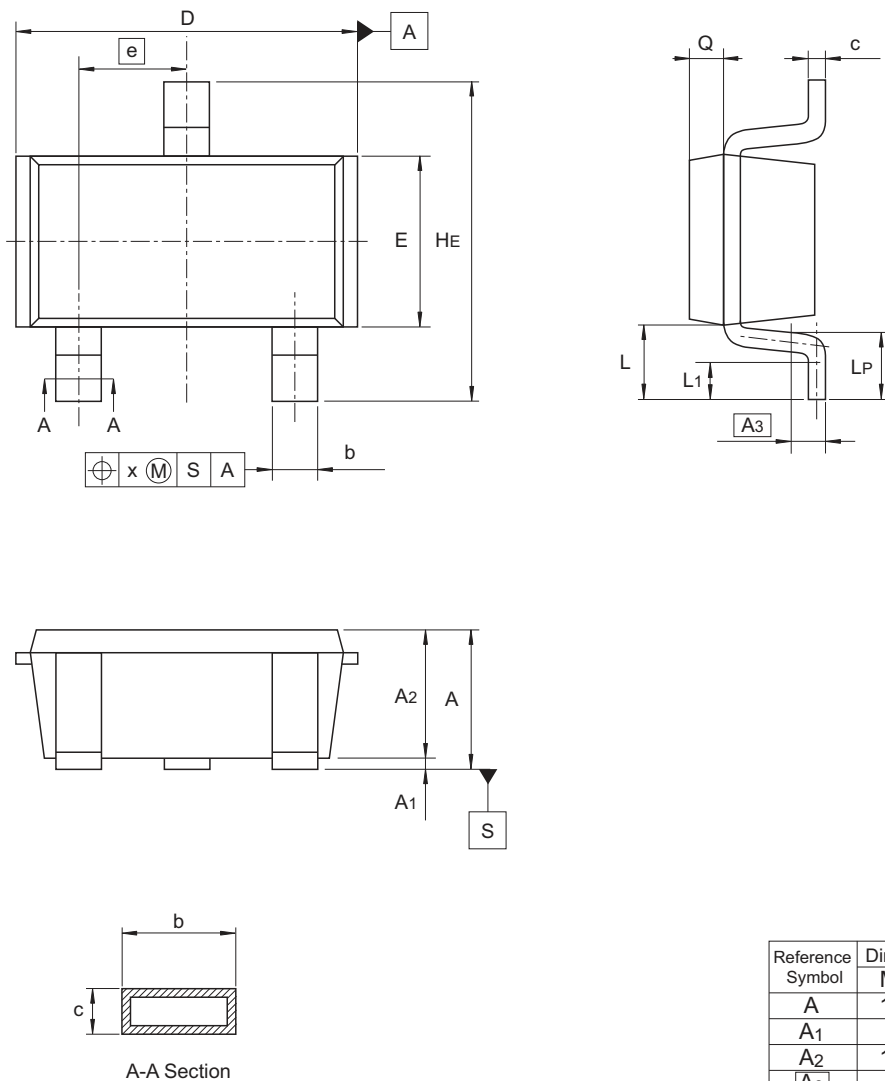


Body-Drain Diode Forward Voltage vs. Case Temperature



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A ₁	0	—	0.1
A ₂	1.0	1.1	1.2
A ₃	—	0.25	—
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
e	—	0.95	—
HE	2.2	2.8	3.0
L	0.35	—	0.75
L ₁	0.15	—	0.55
LP	0.25	—	0.65
x	—	—	0.05
Q	—	0.3	—

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Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQK0204TGDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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