# Tiny Package, High Performance, Regulated Charge Pump

## General Description

The RT9394 is a high performance charge pump DC-DC converter that produces a regulated 5V output. No external inductor is required for operation. The operating voltage range is 2.8V to $V_{OUT}$. Internal soft-start circuitry effectively reduces the in-rush current both while start-up and mode change.

The RT9394 features very low quiescent current, over-current protection and short circuit protection.

The RT9394 is available in WDFN-6SL 2x2 package.

## Ordering Information

RT9394 □□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QW : WDFN-6SL 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Features

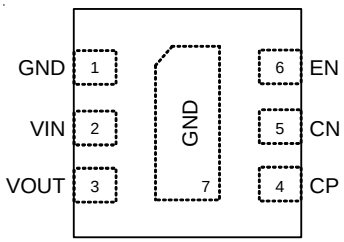
- **Input Voltage Range : 2.8V to $V_{OUT}$**
- **Internal Soft-Start Function**
- **5V Fixed Output Voltage**
- **Over-Current Protection Function**
- **Short Circuit Protection Function**
- **RoHS Compliant and 100% Lead (Pb)-Free**

## Applications

- Mobile Phone, Smart Phone LED Backlight
- Camera Flash White LED
- LCD Display Supply

## Pin Configuration

(TOP VIEW)




WDFN-6SL 2x2

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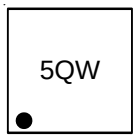
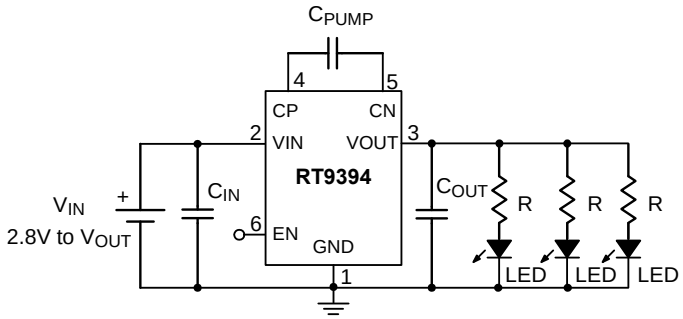
## Marking Information




5Q : Product Code

W : Date Code

## Typical Application Circuit




| Part No. | Application Configuration | $C_{IN}$ (µF) | $C_{PUMP}$ (µF) | $C_{OUT}$ (µF) |
|---|---|---|---|---|
| RT9394 | $I_{OUT}$ < 60mA @ $V_{IN}$ > 3.2V | 1 or 2.2 | 0.22 | 1 or 2.2 |
| | $I_{OUT}$ < 110mA @ $V_{IN}$ > 3.2V | 10 | 1 | 10 |

## Functional Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1,<br>7 (Exposed Pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |
| 2 | VIN | Power input voltage. |
| 3 | VOUT | Output voltage. |
| 4 | CP | Flying capacitor positive terminal. |
| 5 | CN | Flying capacitor negative terminal. |
| 6 | EN | Chip enable (active high). |

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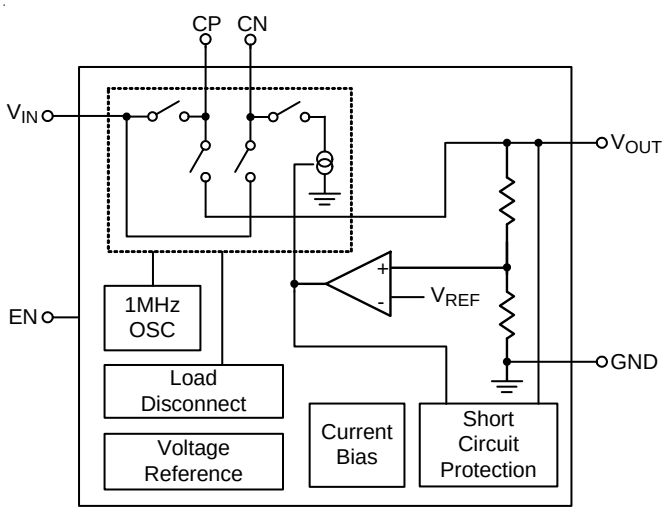
## Functional Block Diagram

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## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 6V
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  WDFN-6SL 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  WDFN-6SL 2x2, $\theta_{JA}$ ---------- 165°C/W
  WDFN-6SL 2x2, $\theta_{JC}$ ---------- 8.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV

## Recommended Operating Conditions (Note 4)

- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

## Electrical Characteristics

($T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operation Voltage Range | $V_{IN}$ | $V_{IN}$ = 3.17V, $V_{OUT}$ = 5V | 2.8 | -- | $V_{OUT}$ | V |
| Output Voltage | $V_{OUT}$ | $V_{IN}$ = 3.17V to 3.43V, $I_{OUT} \leq$ 55mA | 4.83 | 5 | 5.2 | V |
| | | $V_{IN}$ = 5V, $I_{OUT}$ < 70mA | 4.8 | 5 | 5.2 | |
| Quiescent Current | $I_Q$ | $V_{IN}$ = 5V, $I_{OUT}$ = 0 | -- | 2 | 4 | mA |
| Maximum Output Current | $I_{OUT}$ | $V_{IN}$ = 3V, $C_{PUMP}$ = 1μF (Note 5) | 110 | -- | -- | mA |
| OCP | $I_{OCP}$ | $V_{IN}$ = 3V | 250 | 350 | 500 | mA |
| Short Circuit Current | | $V_{IN}$ = 3V, During start-up period | -- | 75 | 110 | mA |
| Output Ripple | | $V_{IN}$ = 3V,$I_{OUT}$ = 60mA, $C_{OUT}$ = 1μF | -- | 30 | -- | mV |
| Shut Down Current | $I_{SHDN}$ | $V_{IN}$ = 5V, $V_{EN}$ = 0.42V | -- | 0.1 | 1 | μA |
| Operation Frequency | $f_{OSC}$ | $V_{IN}$ = 5V | 0.8 | 1 | 1.3 | MHz |
| Digital Input High Level | $V_{IH}$ | $V_{IN}$ = 3V | 1.5 | -- | -- | V |
| Digital Input Low Level | $V_{IL}$ | $V_{IN}$ = 5V, $V_{EN}$ = 0.42V | -- | -- | 0.4 | V |
| EN Pin Leakage Current | $I_{EN}$ | $V_{IN}$ = 5V | -- | -- | 0.2 | μA |

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. $\theta_{JC}$ is measured at the exposed pad of the package.

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**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Maximum Output Current ability is defined in $V_{OUT}$ (5V) ready.

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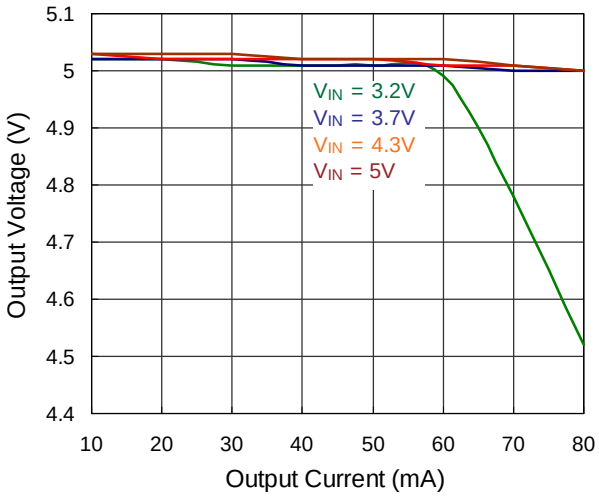
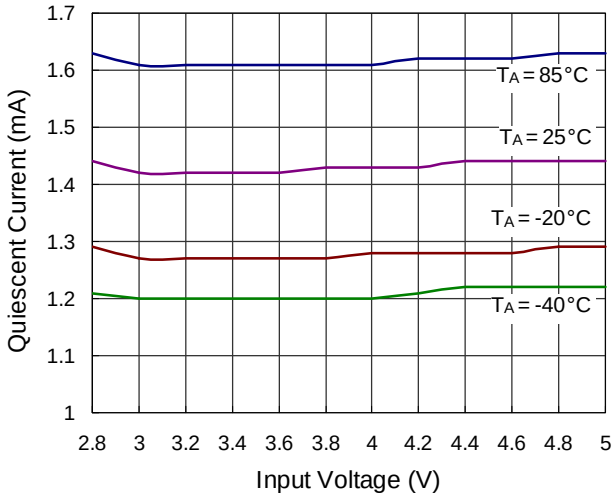
## Typical Operating Characteristics

($C_{IN}$ = $C_{OUT}$ = 2.2µF, $C_{PUMP}$ = 0.22µF, $T_A$ = 25°C, unless otherwise specified )

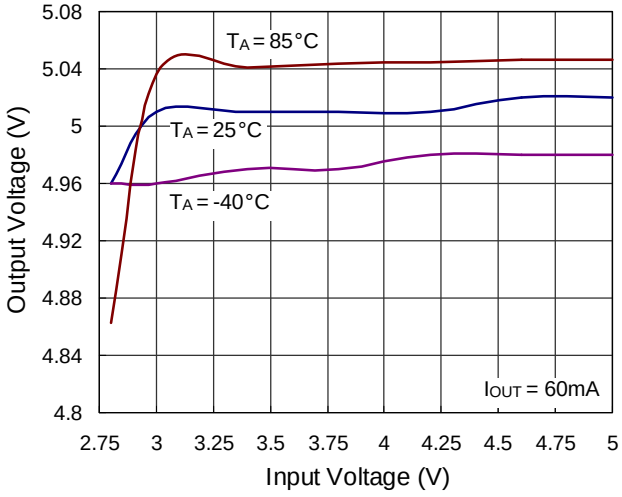
**Output Voltage vs. Output Current**



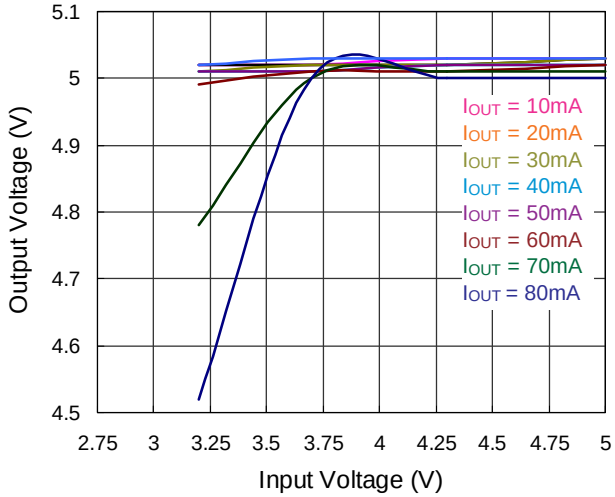

**Quiescent Current vs. Input Voltage**



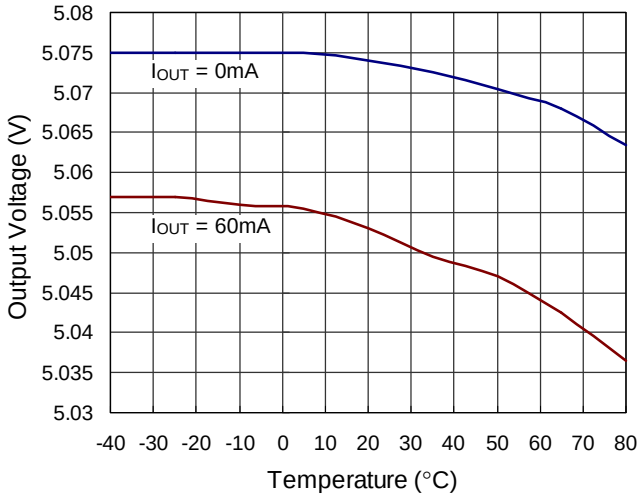

**Output Voltage vs. Input Voltage**



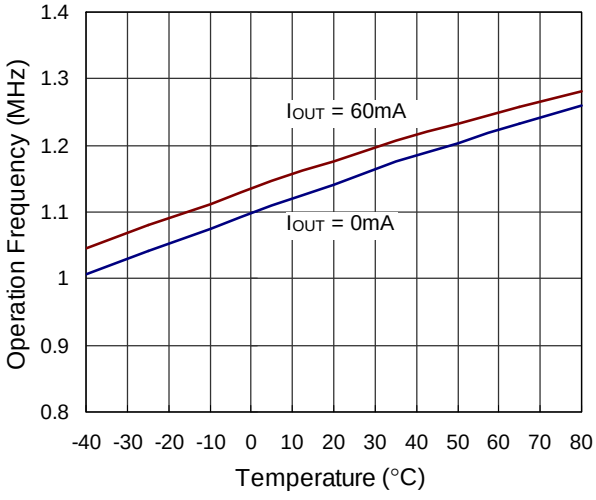

**Output Voltage vs. Input Voltage**




**Output Voltage vs. Temperature**




**Operation Frequency vs. Temperature**

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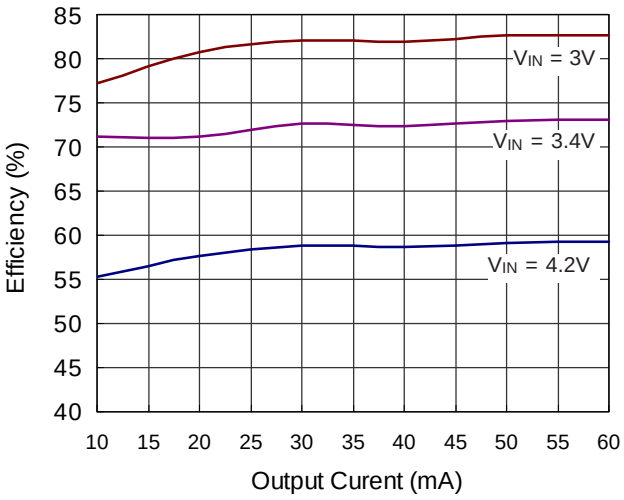
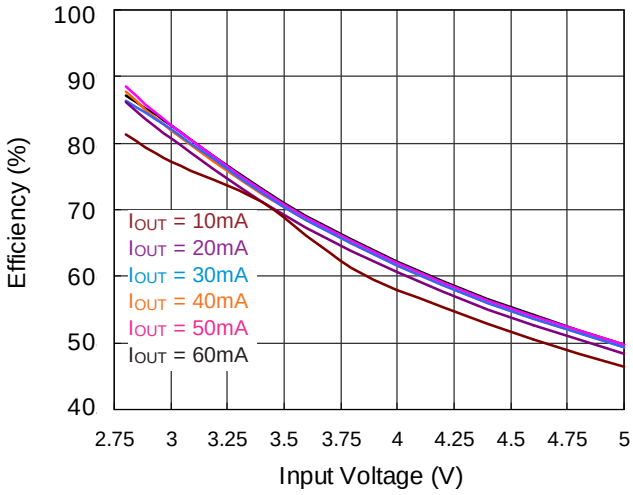
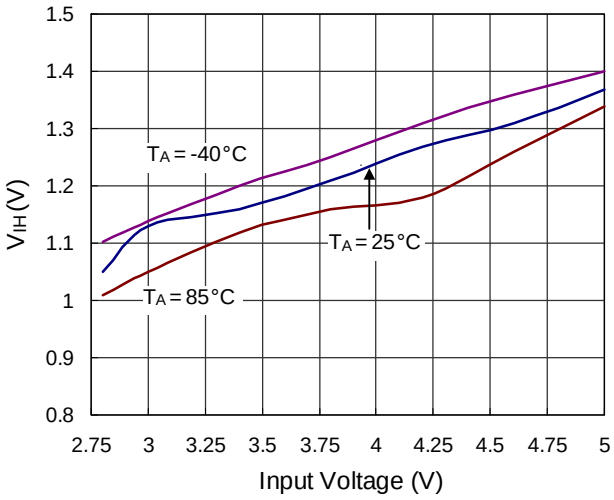
**Efficiency vs. Output Curent**



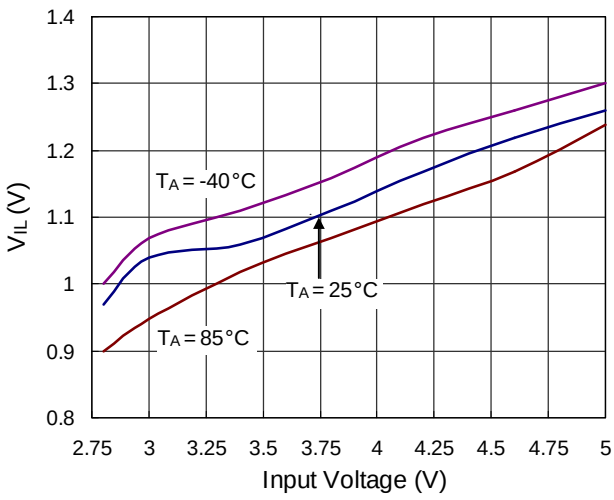

**Efficiency vs. Input Voltage**



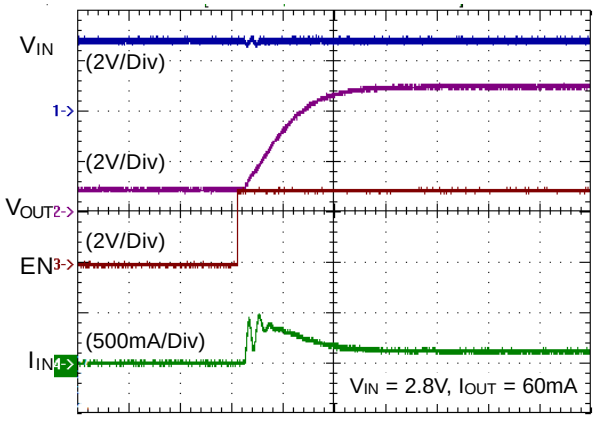

**$V_{IH}$ vs. Input Voltage**



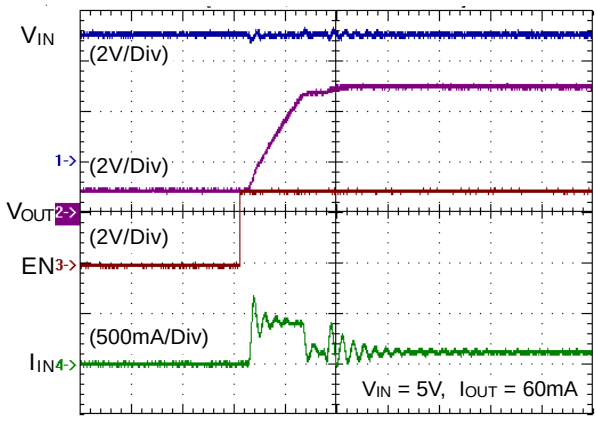

**$V_{IL}$ vs. Input Voltage**




**Inrush Current**




**Inrush Current**

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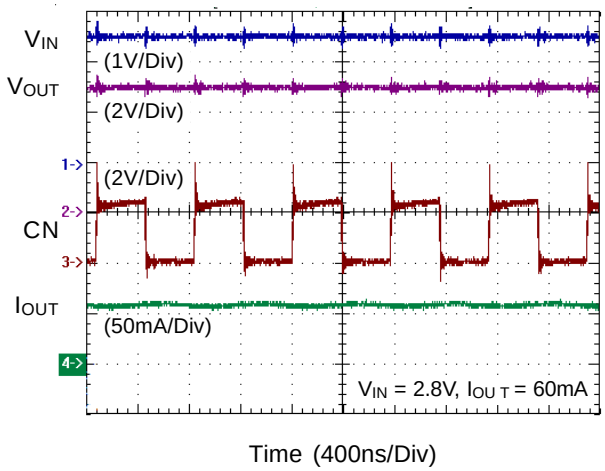
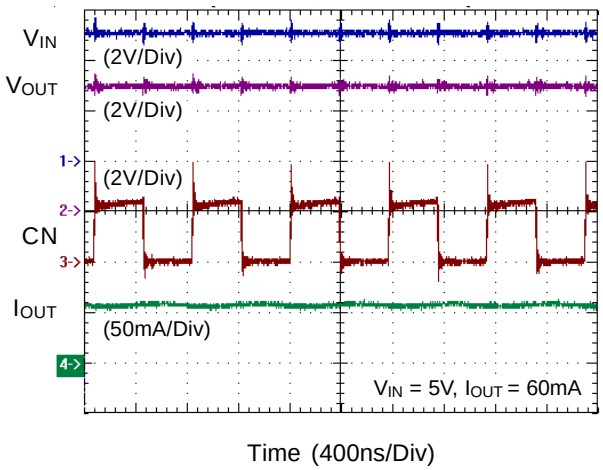
**Normal Operation**



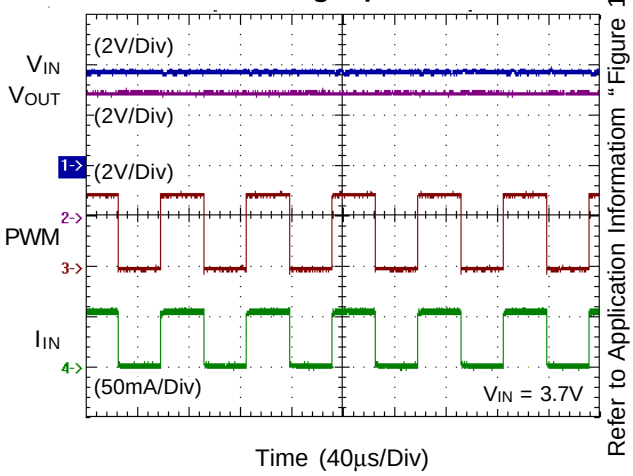

Time (400ns/Div)

**Normal Operation**



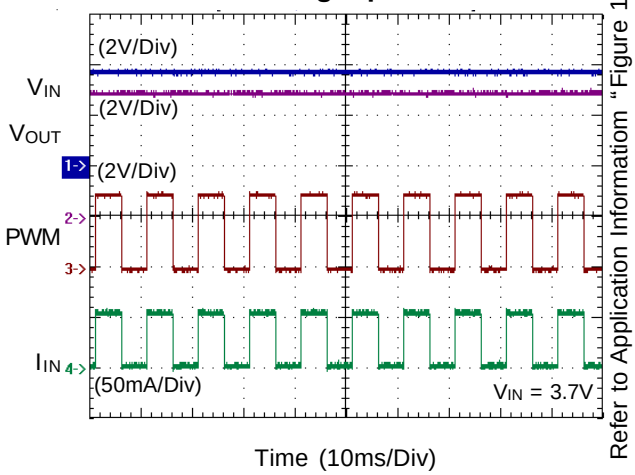

Time (400ns/Div)

**Dimming Operation**



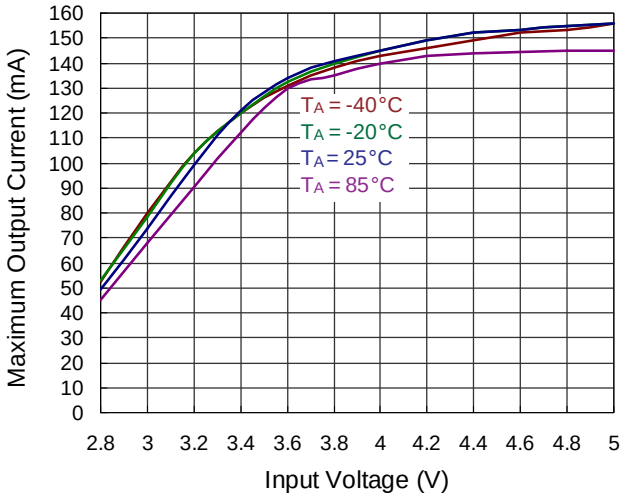

Time (40µs/Div)

**Dimming Operation**




Time (10ms/Div)

**Maximum Output Current vs. Input Voltage**

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## Application Information

### Capacitor Selection

Careful selection of the three external capacitors $C_{IN}$, $C_{OUT}$ and $C_{PUMP}$ is very important because they will affect ramp-up time, output ripple and transient performance. Optimum performance will be obtained when low ESR (<100mΩ) ceramic capacitors are used for $C_{IN}$ and $C_{OUT}$ and $C_{PUMP}$. In general, low ESR may be defined as less than 100mΩ. In all cases, X7R or X5R dielectric are recommended. For particular application, low ESR Tantalum capacitors may be substituted; however optimum output ripple performance may not be realized. Aluminum electrolytic capacitors are not recommended for using with the RT9394 due the their inherent high ESR characteristic.

In general, lower values for $C_{IN}$, $C_{OUT}$ and $C_{PUMP}$ may be utilized for light load current applications (<60mA). Drawing a load current of 60mA or less may use a $C_{IN}$ and $C_{OUT}$ capacitor value as low as 2.2µF and a $C_{PUMP}$ value of 0.22µF. $C_{IN}$ and $C_{OUT}$ may range from 1µF for light loads to 10µF for heavy output load conditions (<110mA). $C_{PUMP}$ may range from 0.22µF for light loads to 1µF for heavy output load conditions. If $C_{PUMP}$ is increased, $C_{OUT}$ should also be increased by the same ratio to minimize output ripple. As a basic rule, the ratio between $C_{IN}$, $C_{OUT}$ and $C_{PUMP}$ should be approximately 10 to 1. Lowering the $C_{IN}$, $C_{OUT}$ and $C_{PUMP}$ value can decrease the ramp-up time of $V_{OUT}$, but it will increase the output ripple oppositely.

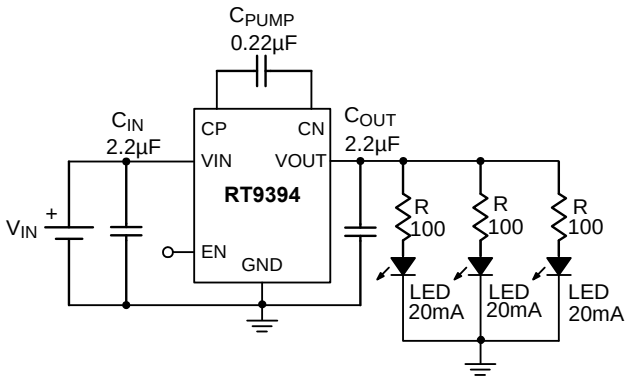


Figure 1. Application Circuits for Backlight Dimming

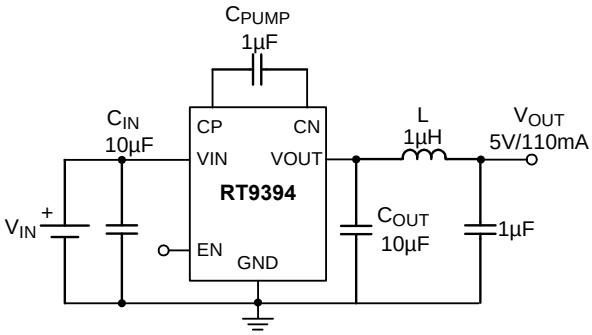


Figure 2. Application Circuits for Constant Load

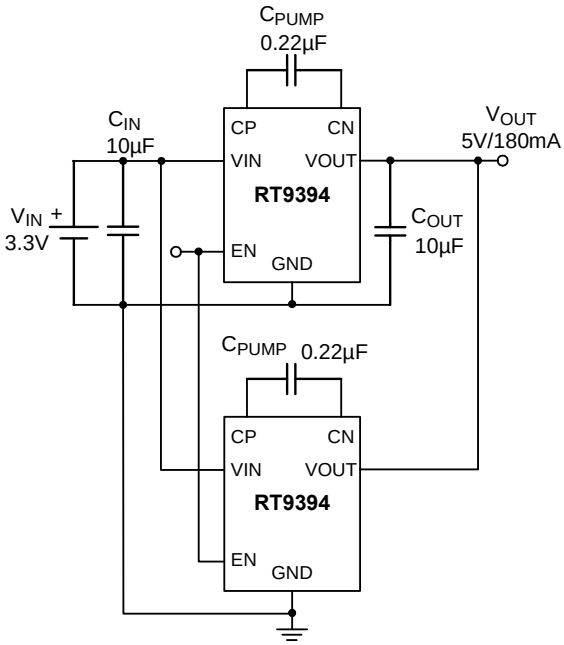


Figure 3. Application Circuits for Doubling the Output Current

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### Efficiency

The efficiency of the charge pump regulator varies with the output voltage version, the applied input voltage, the load current, and the internal operation mode of the device.

The approximate efficiency is given by :

$$\text{Efficiency (\%)} = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times 2I_{OUT}} \times 100$$

$$= \frac{V_{OUT}}{2V_{IN}} \times 100 - - - (\times 2 \text{ Charge Pump Operating Mode})$$

For a charge pump with an output of 5 volts and a nominal input of 3 volts, the theoretical efficiency is 83.33%. Due to internal switching losses and IC quiescent current consumption, the actual efficiency can be measured as 82.72%.

### Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a WDFN-6SL 2x2 package, the thermal resistance, $\theta_{JA}$, is 165°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (165°C/W) = 0.606W for a WDFN-6SL 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

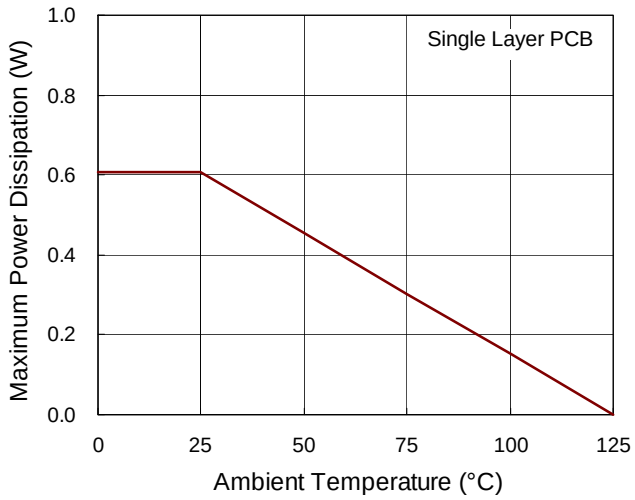


Figure 4. Derating Curve of Maximum Power Dissipation

### PCB Board Layout

The RT9394 is a high-frequency switched-capacitor converter, and therefore large transient currents will flow in $V_{IN}$ and $V_{OUT}$. For best performance and to minimize ripple, place all of the components as close to IC as possible. Besides a solid ground plane is recommended on the bottom layer of the PCB. The ground of $C_{IN}$ and $C_{OUT}$ should be connected together and as close to the IC as possible. Figure 5 and Figure 6 shows the typical PCB layout of RT9394 EVB board.

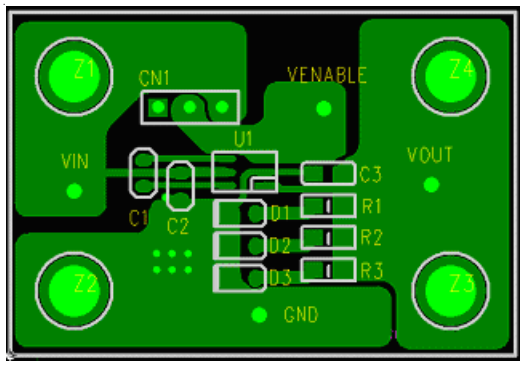


Figure 5

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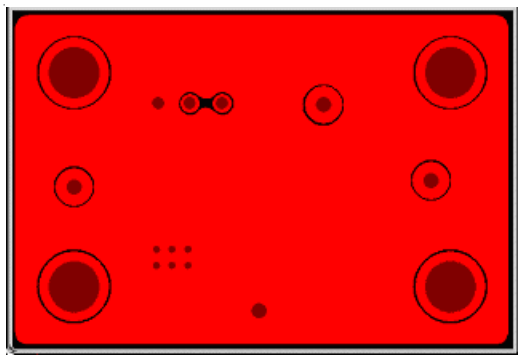

Figure 6

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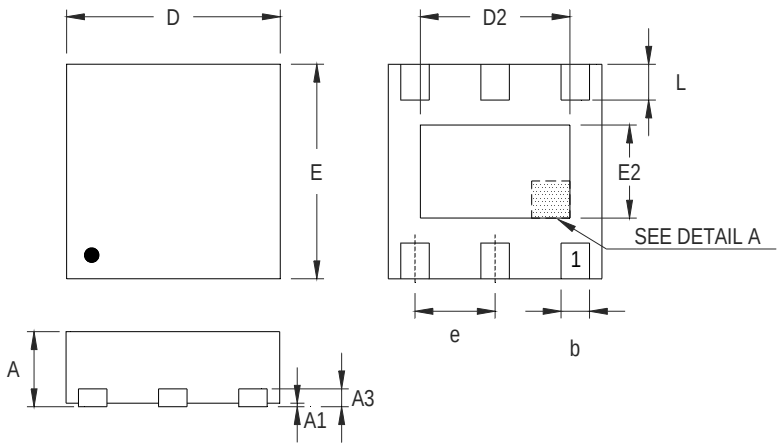
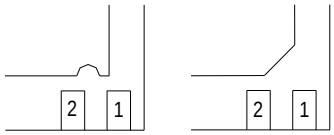
## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.200 | 0.350 | 0.008 | 0.014 |
| D | 1.900 | 2.100 | 0.075 | 0.083 |
| D2 | 1.550 | 1.650 | 0.061 | 0.065 |
| E | 1.900 | 2.100 | 0.075 | 0.083 |
| E2 | 0.950 | 1.050 | 0.037 | 0.041 |
| e | 0.650 | | 0.026 | |
| L | 0.200 | 0.300 | 0.008 | 0.012 |

**W-Type 6SL DFN 2x2 Package**

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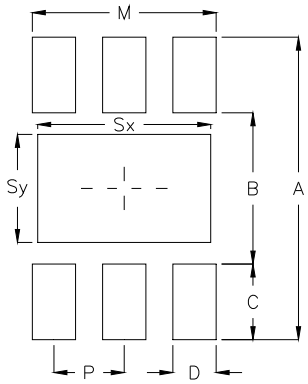
## Footprint Information




| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|
| | | P | A | B | C | D | Sx | Sy | M | |
| V/W/U/XDFN2x2-6S | 6 | 0.65 | 2.80 | 1.40 | 0.70 | 0.40 | 1.60 | 1.00 | 1.70 | ±0.05 |

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