

SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SDAS214D – DECEMBER 1982 – REVISED JULY 2001

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading

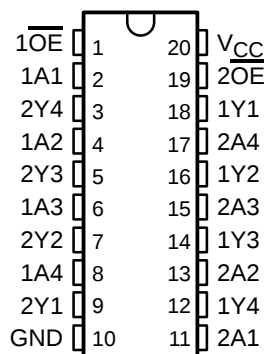
description

These octal buffers/drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. When these devices are used with the 'ALS241, 'AS241A, 'ALS244, and 'AS244A, the circuit designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs. These devices feature high fan-out and improved fan-in.

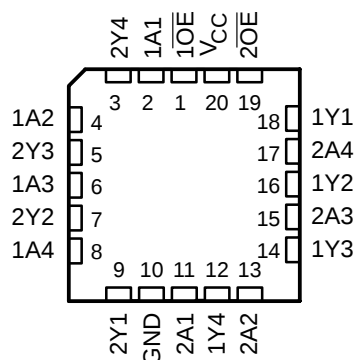
The -1 version of SN74ALS240A is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is 48 mA. There is no -1 version of the SN54ALS240A.

SN54ALS240A, SN54AS240A . . . J OR W PACKAGE
SN74ALS240A . . . DB, DW, OR N PACKAGE
SN74AS240A . . . DW OR N PACKAGE

(TOP VIEW)



SN54ALS240A, SN54AS240A . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS240AN	SN74ALS240AN
			SN74AS240AN	SN74AS240AN
	SOIC – DW	Tube	SN74ALS240ADW	ALS240A
			SN74AS240ADW	AS240A
		Tape and reel	SN74ALS240ADWR	ALS240A
			SN74AS240ADWR	AS240A
–55°C to 125°C	SSOP – DB	Tape and reel	SN74ALS240ADBR	G240A
	CDIP – J	Tube	SNJ54ALS240AJ	SNJ54ALS240AJ
			SNJ54AS240AJ	SNJ54AS240AJ
	CFP – W	Tube	SNJ54ALS240AW	SNJ54ALS240AW
			SNJ54AS240AW	SNJ54AS240AW
	LCCC – FK	Tube	SNJ54ALS240AFK	SNJ54ALS240AFK
			SNJ54AS240AFK	SNJ54AS240AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

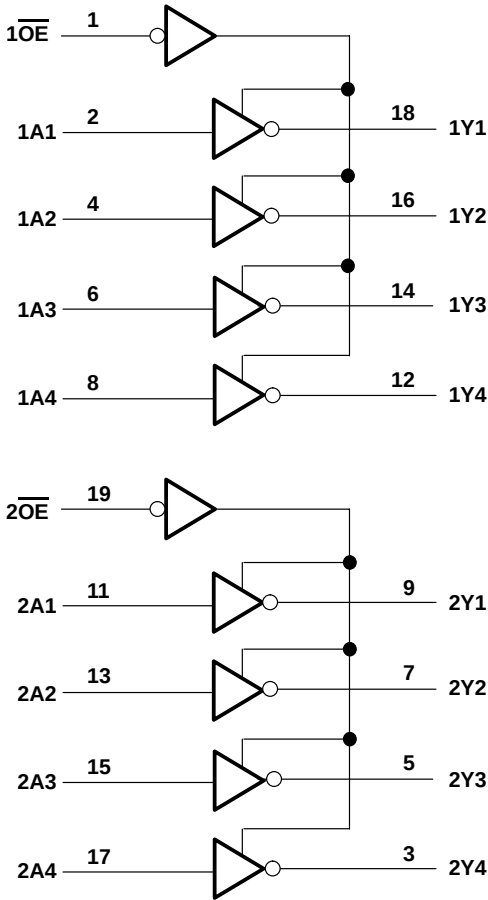
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FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	L
L	L	H
H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DB package	70°C/W
DW package	58°C/W
N package	70°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage	SN54ALS240A		0.7	V
		SN74ALS240A, 'AS240A		0.8	
I_{OH}	High-level output current	SN54ALS240A, SN54AS240A		-12	mA
		SN74ALS240A, SN74AS240A		-15	
I_{OL}	Low-level output current	SN54ALS240A		12	mA
		SN74ALS240A		24	
				48 [†]	
		SN54AS240A		48	
T_A	Operating free-air temperature	SN54ALS240A, SN54AS240A		-55	°C
		SN74ALS240A, SN74AS240A		0	

[†] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS240A			SN74ALS240A			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} − 2			V _{CC} − 2			V
	V _{CC} = 4.5 V	I _{OH} = −3 mA	2.4	3.2	2.4	3.2			
		I _{OH} = −12 mA	2						
		I _{OH} = −15 mA			2				
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25 0.4		0.25 0.4		V		
		I _{OL} = 24 mA			0.35 0.5				
		I _{OL} = 48 mA [†]			0.35 0.5				
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20			20			μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	−20			−20			μA	
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	−0.1			−0.1			mA	
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	−20	−112		−30	−112		mA	
I _{CC}	V _{CC} = 5.5 V	Outputs high	4	11	4	11		mA	
		Outputs low	13	23	13	23			
		Outputs disabled	14	25	14	25			

[†] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS240A			SN74AS240A			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$				-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
		$I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -12 \text{ mA}$	2.4						
		$I_{OH} = -15 \text{ mA}$				2.4			
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 48 \text{ mA}$	0.27	0.55					V
		$I_{OL} = 64 \text{ mA}$				0.31	0.55		
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$				50			50	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$				-50			-50	μA
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$				0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$				20			20	μA
I_{IL}	A inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-1			-1	mA
	$\overline{OE}$ inputs				-0.5			-0.5	
$I_O^{\ddagger}$	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$		-50		-150	-50		-150	mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	11	17		11	17		mA
		Outputs low	51	75		51	75		
		Outputs disabled	24	38		24	38		

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS240A		SN74ALS240A		
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	2	22	2	9	ns
t _{PHL}			2	11	2	9	
t _{PZH}	$\overline{\text{OE}}$	Y	4	34	5	13	ns
t _{PZL}			5	26	5	18	
t _{PHZ}	$\overline{\text{OE}}$	Y	1	15	2	10	ns
t _{PLZ}			3	24	3	12	

^{\S} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX [†]				UNIT
			SN54AS240A		SN74AS240A		
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1	7	1	6.5	ns
t _{PHL}			1.2	6.5	1.2	6.5	
t _{PZH}	$\overline{\text{OE}}$	Y	1	7	1	6.4	ns
t _{PZL}			1.1	9.5	1.1	9	
t _{PHZ}	$\overline{\text{OE}}$	Y	1.2	5.5	1.2	5	ns
t _{PLZ}			1.5	12.5	1.5	9.5	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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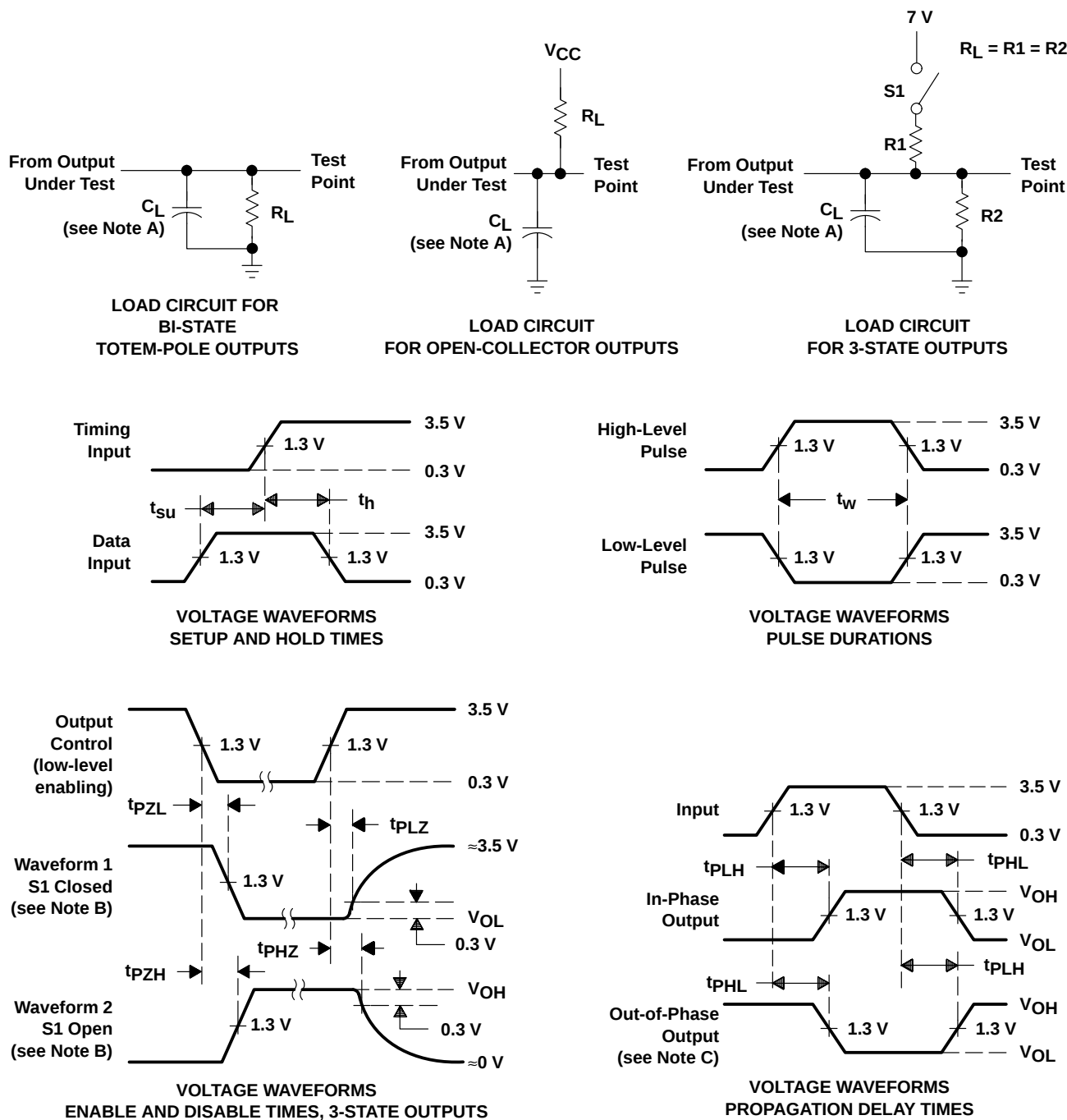
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PARAMETER MEASUREMENT INFORMATION

SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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