



MICROCHIP

PIC16(L)F145X

14/20-Pin, 8-Bit Flash USB Microcontroller Product Brief

High-Performance RISC CPU:

- C Compiler Optimized Architecture
- Only 49 Instructions
- Up to 14 Kbytes Linear Program Memory Addressing
- Up to 1024 bytes Linear Data Memory Addressing
- Operating Speed:
 - DC – 48 MHz clock input
 - DC – 83 ns instruction cycle
 - Selectable 3x or 4x PLL for specific frequencies
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
 - Two full 16-bit File Select Registers (FSRs) capable of accessing both Data or Program memory
 - FSRs can read program and data memory

Special Microcontroller Features:

- Operating Voltage Range:
 - 1.8V to 3.6V (PIC16LF145X)
 - 2.3V to 5.5V (PIC16F145X)
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Programmable Low-Power Brown-Out Reset (LPBOR)
- Extended Watchdog Timer (WDT):
 - Programmable period from 1 ms to 256s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Power-Saving Sleep mode:
 - Low-Power Sleep mode
 - Low-Power BOR (LPBOR)
- Integrated Temperature Indicator

Universal Serial Bus (USB) Features:

- Clock Recovery from USB host (eliminates need for external crystal)
- USB V2.0 Compliant SIE
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 8 Bidirectional Endpoints
- 512-byte Dual Access RAM for USB
- Input Interrupt-on-Change (IOC) on D+/D- for USB host detection
- Configurable internal pull-up resistors for use with USB

Low-Power Features

(PIC16(L)F145X with nanoWatt XLP):

- Standby Current:
 - 20 nA @ 1.8V, typical
- Watchdog Timer Current:
 - 300 nA @ 1.8V, typical
- Operating Current:
 - 30 μ A/MHz @ 1.8V, typical
- Timer1 Oscillator:
 - 600 nA @ 32 kHz, 1.8V, typical

Flexible Oscillator Structure:

- 48 MHz Internal Oscillator Block:
 - Factory calibrated to $\pm 1\%$, typical
 - Software selectable frequency range from 48 MHz to 31 kHz
 - USB tune to 0.25%, typical
- 31 kHz Low-Power Internal Oscillator
- Clock Switching with run from:
 - Primary Oscillator
 - Secondary Oscillator (SOSC)
 - Internal Oscillator
- Clock Reference Output:
 - Clock Prescaler
 - CLKOUT

Peripheral Features:

- Analog-to-Digital Converter (ADC)⁽¹⁾:
 - 10-bit resolution
 - Up to 9 external channels
 - 3 internal sources:
 - Fixed Voltage Reference channel
 - DAC output channel⁽¹⁾
 - Temperature Indicator channel
 - Auto acquisition capability
 - Conversion available during Sleep
- 2 Comparators⁽¹⁾:
 - Rail-to-rail inputs
 - Power mode control
 - Software controllable hysteresis
- Voltage Reference module:
 - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
 - Up to 1 rail-to-rail resistive 5-bit DAC with positive and negative reference selection
- Up to 15 I/O Pins and 3 Input-only Pins:
 - High current sink/source 25 mA/25 mA
 - Individually programmable weak pull-ups
 - Individually programmable interrupt-on-change (IOC) pins

Note: Not available on PIC16(L)F1454 devices.

PIC16(L)F145X

Peripheral Features (Continued):

- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Gate Input mode
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler⁽¹⁾
- Two 10-bit PWM modules⁽¹⁾
- Master Synchronous Serial Port (MSSP) with SPI and I²C™ with:
 - 7-bit address masking
 - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
 - RS-232, RS-485 and LIN compatible
 - Auto-baud detect
 - Auto-wake-up on Start
- Complementary Waveform Generator (CWG)⁽¹⁾:
 - Up to 4 selectable signal sources
 - Selectable falling and rising edge dead-band control
 - Polarity control
 - Up to 4 auto-shutdown sources
 - Multiple input sources: PWM, Comparators

Note: Not available on PIC16(L)F1454 devices.

PIC16(L)F145X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	I/O's ⁽²⁾	10-bit ADC (ch)	Comparators	DAC	Timers (8/16-bit)	PWM	EUSART	MSSP (I ² C™/SPI)	CWG	USB	Clock Reference	Debug ⁽¹⁾	XLP
PIC16(L)F1454	(1)	4096	512	12	—	—	—	1/1	—	1	1	—	1	1	H	Y
PIC16(L)F1455	(2)	8192	1024	12	5	2	1	2/1	2	1	1	1	1	1	H	Y
PIC16(L)F1458	(3)	4096	512	18	9	2	1	2/1	2	1	1	1	1	1	H	Y
PIC16(L)F1459	(4)	8192	1024	18	9	2	1	2/1	2	1	1	1	1	1	I/H	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

- 1: Future Product PIC16(L)F1454 Data Sheet, 14-Pin Flash, 8-bit Microcontrollers.
- 2: Future Product PIC16(L)F1455 Data Sheet, 14-Pin Flash, 8-bit Microcontrollers.
- 3: Future Product PIC16(L)F1458 Data Sheet, 20-Pin Flash, 8-bit Microcontrollers.
- 4: Future Product PIC16(L)F1459 Data Sheet, 20-Pin Flash, 8-bit Microcontrollers.

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP DIAGRAM FOR PIC16(L)F1454/5

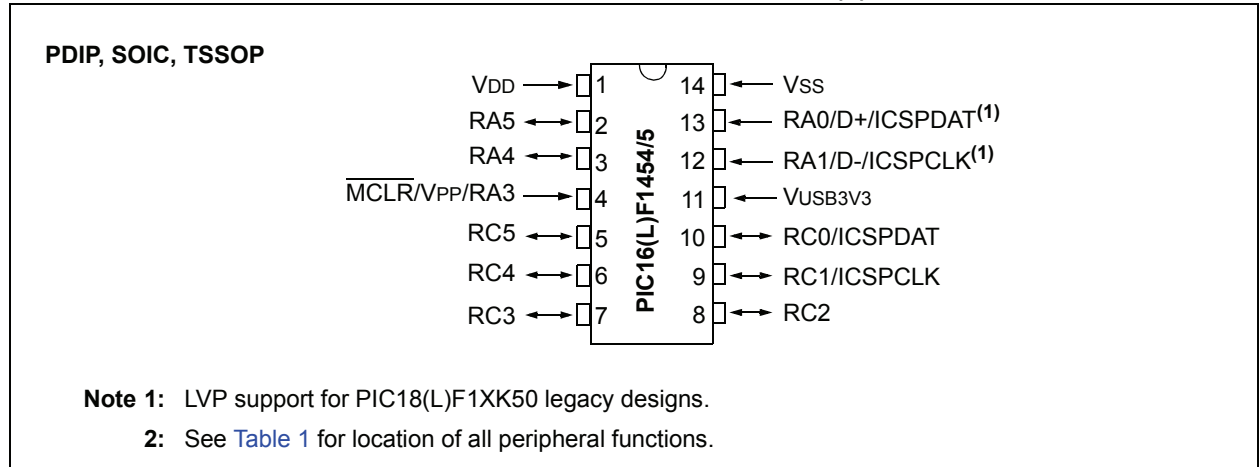
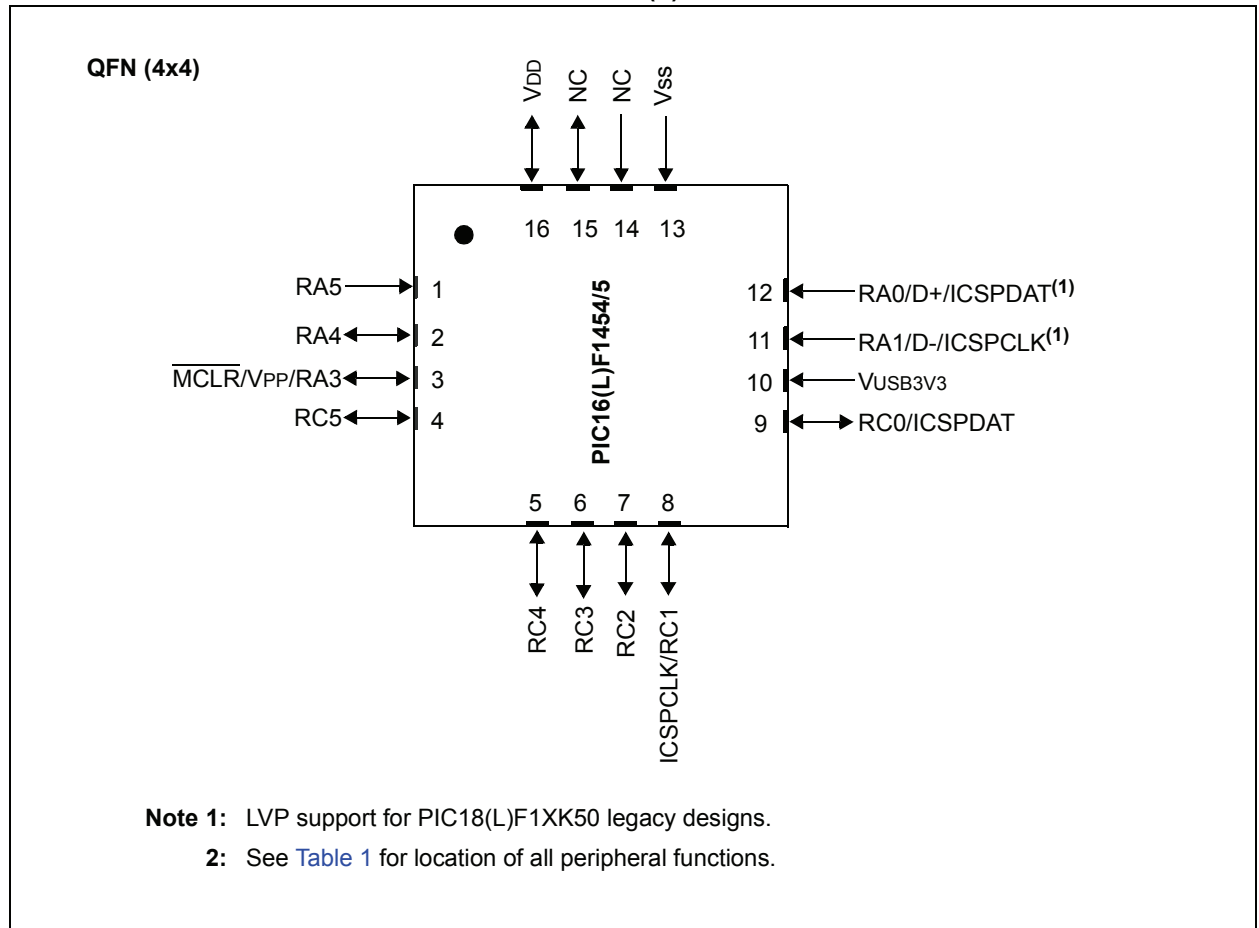


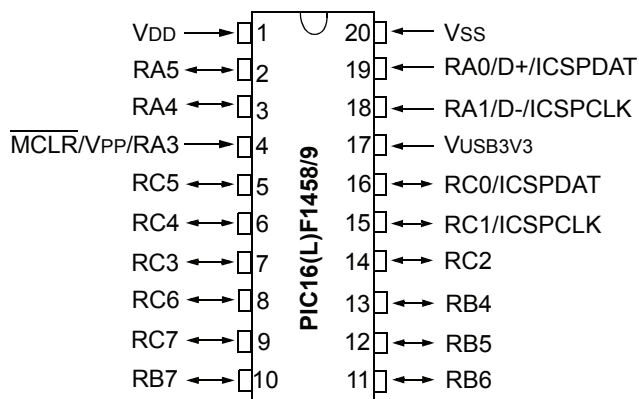
FIGURE 2: 16-PIN QFN DIAGRAM FOR PIC16(L)F1454/5



PIC16(L)F145X

FIGURE 3: 20-PIN PDIP, SOIC, SSOP PACKAGE DIAGRAM FOR PIC16(L)F1458/9

PDIP, SOIC, SSOP

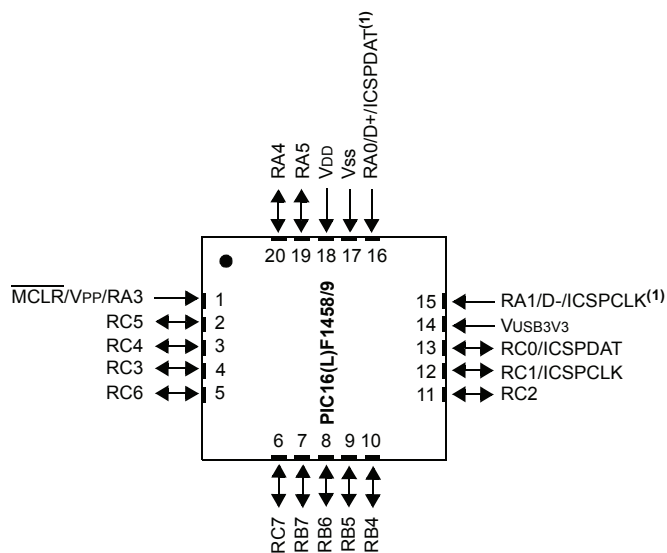


Note 1: LVP support for PIC18(L)F1XK50 legacy designs.

2: See [Table 1](#) for location of all peripheral functions.

FIGURE 4: 20-PIN QFN DIAGRAM FOR PIC16(L)F1458/9

QFN (4x4)



Note 1: LVP support for PIC18(L)F1XK50 legacy designs.

2: See [Table 1](#) for location of all peripheral functions.

TABLE 1: 14-PIN ALLOCATION TABLE (PIC16(L)F1454/5)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	ADC	Reference	Comparator	Timer	CWG	USB	EUSART	PWM	MSSP	Interrupt	Basic
RA0	13	12	—	—	—	—	—	D+	—	—	—	IOC	ICSPDAT ⁽³⁾
RA1	12	11	—	—	—	—	—	D-	—	—	—	IOC	ICSPCLK ⁽³⁾
RA2	—	—	—	—	—	—	—	—	—	—	—	—	—
RA3	4	3	—	—	—	SOSCO T1G ⁽²⁾	—	—	—	—	SS ⁽²⁾	IOC	MCLR V _{PP}
RA4	3	2	AN3	—	—	SOSCI T1G ⁽¹⁾	—	—	—	—	SDO ⁽²⁾	IOC	CLKOUT OSC2 CLKR ⁽¹⁾
RA5	2	1	—	—	—	T1CKI	—	—	—	PWM2 ⁽²⁾	—	IOC	CLKIN OSC1
RC0	10	9	AN4	VREF+ DAC VREF+ ADC	C1IN+ C2IN+	—	—	—	—	—	SCL SCK	—	ICSPDAT
RC1	9	8	AN5	—	C1IN1- C2IN1-	—	CWGFLT	—	—	—	SDA SDI	INT	ICSPCLK
RC2	8	7	AN6	DACOUT1	C1IN2- C2IN2-	—	—	—	—	—	SDO ⁽¹⁾	—	—
RC3	7	6	AN7	DACOUT2	C1IN3- C2IN3-	—	—	—	—	PWM2 ⁽¹⁾	SS ⁽¹⁾	—	CLKR ⁽²⁾
RC4	6	5	—	—	C1OUT C2OUT	—	CWG1B	—	TK CK	—	—	—	—
RC5	5	4	—	—	—	T0CKI	CWG1A	—	RX DT	PWM1	—	—	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	VSS
VUSB3V3	11	10	—	—	—	—	—	VUSB3V3	—	—	—	—	—

- Note**
- 1: Default location for peripheral pin function. Alternate location can be selected using the APFCON register.
 - 2: Alternate location for peripheral pin function selected by the APFCON register.
 - 3: LVP support for PIC18(L)F1XK50 legacy designs.

PIC16(L)F145X

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16(L)F1458/9)

I/O	20-Pin PDIP/SOIC/MSOP/DFN	20-Pin QFN	ADC	Reference	Comparator	Timer	CWG	USB	EUSART	PWM	MSSP	Interrupt	Basic
RA0	19	16	—	—	—	—	—	D+	—	—	—	IOC	ICSPDAT ⁽³⁾
RA1	18	15	—	—	—	—	—	D-	—	—	—	IOC	ICSPCLK ⁽³⁾
RA2	—	—	—	—	—	—	—	—	—	—	—	—	—
RA3	4	1	—	—	—	T1G ⁽²⁾	—	—	—	—	$\overline{\text{SS}}$ ⁽²⁾	IOC	$\overline{\text{MCLR}}$ VPP
RA4	3	20	AN3	—	—	SOSCO T1G ⁽¹⁾	—	—	—	—	—	IOC	OSC2 CLKOUT CLKR ⁽¹⁾
RA5	2	19	—	—	—	SOSCI T1CKI	—	—	—	—	—	IOC	OSC1 CLKIN
RB4	13	10	AN10	—	—	—	—	—	—	—	SDA SDI	IOC	—
RB5	12	9	AN11	—	—	—	—	—	RX DX	—	—	IOC	—
RB6	11	8	—	—	—	—	—	—	—	—	SCL SCK	IOC	—
RB7	10	7	—	—	—	—	—	—	TX CK	—	—	IOC	—
RC0	16	13	AN4	VREF+ DAC VREF+ ADC	C1IN+ C2IN+	—	—	—	—	—	—	—	ICSPDAT
RC1	15	12	AN5	—	C1IN1- C2IN1-	—	$\overline{\text{CWGFLT}}$	—	—	—	—	INT	ICSPCLK
RC2	14	11	AN6	DACOUT1	C1IN2- C2IN2-	—	—	—	—	—	—	—	—
RC3	7	4	AN7	DACOUT2	C1IN3- C2IN3-	—	—	—	—	—	—	—	CLKR ⁽²⁾
RC4	6	3	—	—	C1OUT C2OUT	—	CWG1B	—	—	—	—	—	—
RC5	5	2	—	—	—	T0CKI	CWG1A	—	—	PWM1	—	—	—
RC6	8	5	AN8	—	—	—	—	—	—	PWM2	$\overline{\text{SS}}$ ⁽¹⁾	—	—
RC7	9	6	AN9	—	—	—	—	—	—	—	SDO	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	VSS
VUSB3V3	17	14	—	—	—	—	—	VUSB3V3	—	—	—	—	—

- Note**
- 1: Default location for peripheral pin function. Alternate location can be selected using the APFCON register.
 - 2: Alternate location for peripheral pin function selected by the APFCON register.
 - 3: LVP support for PIC18(L)F1XK50 legacy designs.

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ISBN: 978-1-61341-918-2

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