GENNUM CORPORATION

GENLINX™ GS9001
EDH Coprocessor

DATA SHEET

FEATURES

- **Error Detection and Handling (EDH) according to SMPTE RP165**
- **EDH insertion and extraction in one device**
- **autostandard operation**
- **I²C Serial communications interface for access to error flags and device configuration**
- **available stand alone mode**
- **error flags available on dedicated outputs**
- **field, vertical, horizontal timing signals, ancillary data indication and TRS indication**
- **video standard and invalid data indication**
- **reserved words readable and writeable**
- **21 bit Errored Fields counter**
- **passthrough mode to bypass EDH packet insertion**
- **true 8-bit compatibility**
- **40 MHz operating frequency**
- **Pb-free and Green**

APPLICATIONS

- 4$f$sc, 4:2:2 and 360 Mb/s serial digital interfaces
- Source and destination equipment
- Distribution equipment
- Test equipment

DESCRIPTION

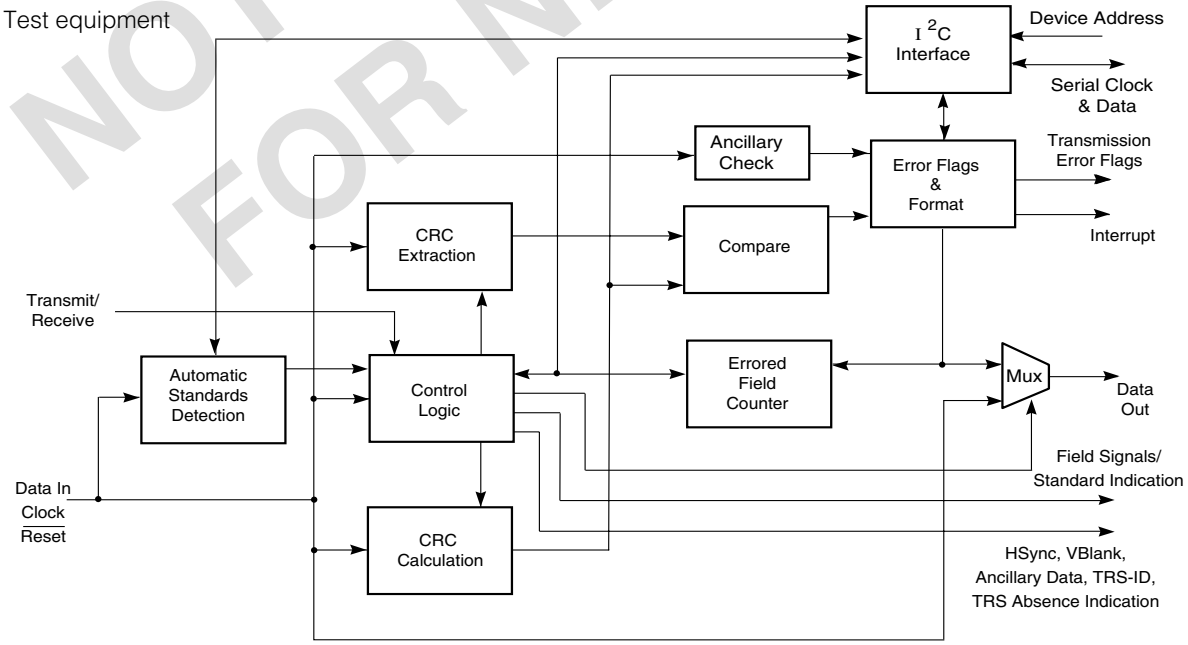
The GS9001 implements error detection and handling (EDH) functions according to SMPTE RP165. Interfacing to the parallel port of either the GS9002/GS9022 serial digital encoders or GS9000 decoder, the GS9001 provides EDH insertion and extraction for 4$f$sc NTSC, 4$f$sc PAL and 4:2:2 component standards up to 18 MHz luminance sampling. The GS9001 also generates timing signals such as horizontal sync, vertical blanking, field ID and ancillary data identification. The ancillary data identification aids the extraction of ancillary data from the data stream.

The device has an I²C (Inter-Integrated Circuit) serial interface bus for communication with a microcontroller. The device can be programmed as an I²C slave transmitter or receiver by the microcontroller. This interface can be used to read the complete set of error flags and override the flag status prior to re-transmission. The device automatically determines the operating standard which can be overridden through the I²C interface. Timing signals and transmission error flags are also available on dedicated outputs.

ORDERING INFORMATION

Part Number	Package	Temperature	Pb-Free and Green
GS9001-CQM	44 PQFP	o°C to 70°C	No
GS9001-CQME3	44 PQFP	o°C to 70°C	Yes

NOT RECOMMENDED FOR NEW DESIGNS



BLOCK DIAGRAM

I²C is a registered Trademark of Philips

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage (V_S=V_{DD}-V_{SS})	7 V
Input Voltage Range (any input)	-0.3 to (V_{DD}+0.3) V
DC Input Current (any one input)	±10 µA
Power Dissipation	800 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	260°C

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



ELECTRICAL CHARACTERISTICS

DC Parameters @ V_{DD} = 5V, V_{SS} = 0V, T_A = 0ºC - 70ºC unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_S	Operating range	4.75	5.00	5.25	V
Supply Current	I_S	Operating range	-	85	100	mA
TTL Compatible	V_{IHmin}	T_A=25ºC	2.00	-	-	V
CMOS Inputs	V_{ILmax}	T_A=25ºC	-	-	0.80	V
Input Leakage	I_{IN}	V_{IN}=V_{DD} or V_{SS}	-	-	±10	µA
TTL Compatible	V_{OHmin}	T_A=25ºC	2.40	4.50	-	V
CMOS Outputs	V_{OLmax}	T_A=25ºC	-	0.20	0.40	V
	I_{OL}	T_A=25ºC	-	-	-4	mA
	I_{OH}	T_A=25ºC	-	-	4	mA

AC Parameters @ V_{DD} = 5V, V_{SS} = 0V, T_A = 0ºC - 70ºC unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Clock Frequency	f_{clk}		-	-	40	MHz
Input & Output Data Rates	f_{data}		-	-	40	Mb/s
Input Data & Clock						
Rise Time	t_{ir}		-	1	-	ns
Setup Time	t_{set}	T_A=25ºC	2	-	-	ns
Hold Time	t_{hold}		2	-	-	ns
Input Clock to Output data	t_P	C_L < 30pF	3	5.5	8.5(1)	ns
Output data rise/fall time	t_{or}	T_A=25ºC	2	3	4	ns
SCL Clock Frequency	f_{SCL}		-	100	400(2)	kHz

(1) T_A = 70°c, V_{DD} = 4.75V

(2) Determined by I²C bus specification

NOT RECOMMENDED FOR NEW DESIGNS

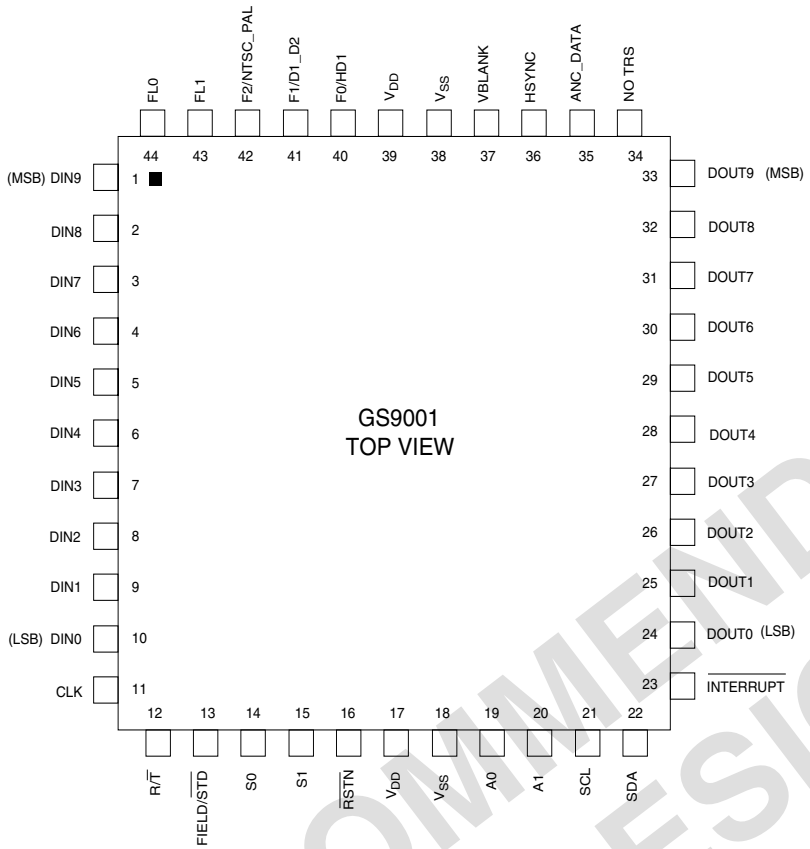


Fig. 1 GS9001 EDH Coprocessor Pin Connections

Table 1. Selection of Field and Video standard signals on F2, F1, F0 pins

Input Field/$\overline{\text{Std}}$	Output F2	Output F1	Output F0
0	NTSC (0) / PAL (1)	D1 (0) / D2 (1)*	13.5 MHz Y (0) / 18 MHz Y (1)
1	Field Bit 2	Field Bit 1	Field Bit 0

*D1: 4:2:2 sampling
D2: $4f_{sc}$ sampling

Table 2. Selection of Error status flags to display

Input S1	Input S0	Output FL1	Output FL0
0	0	***EDA*** Full Field	***EDH*** Full Field
0	1	***UES*** (See Note)	***EDH*** Active Picture
1	0	***EDA*** Ancillary	***EDH*** Ancillary
1	1	***IDA*** (See Note)	***IDH*** (See Note)

NOTE: The UES, IDH and IDA flags that appear on pins FL0 and FL1 as shown in Table 2, represent the sum of each corresponding flag for active picture, full field and ancillary. UES indication can also be used to identify the absence of EDH implementation in the upstream equipment.

NOT RECOMMENDED FOR NEW DESIGNS

GS9001 PIN DESCRIPTIONS

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1-10	DIN[9..0]	I	Parallel digital video data inputs
11	CLK	I	Parallel clock input.
12	R/$\overline{T}$	I	Receive or Transmit mode select. High - CRC extraction, recalculation, comparison, error indication, re-insertion. Low - CRC calculation, insertion, clears error flags
13	FIELD/$\overline{STD}$	I	Field or Standard indication select. High - Field signals on F0, F1, F2. Low - Standard indication on F0, F1,F2. (Refer to Table 1)
14,15	S0, S1	I	Error flag select inputs. Select type of error flag to output on FL0, FL1. (Refer to Table 2)
16	$\overline{RSTN}$	I	Master Reset. Active low input, which provides option to initialise internal circuitry. The GS9001 contains power on reset circuitry that automatically initialises all internal states including the I^2C Interface.
19,20	A0,A1	I	Device address select pins for I^2C interface bus. (Refer to Table 3)
21	SCL	I	Serial Clock for I^2C Interface bus. SCL and SDA must be connected to GND if there is no I^2C interface connected to the device.
22	SDA	I/O	Serial Data for I^2C Interface bus.
23	$\overline{INTERRUPT}$	O	Programmable interrupt for error flag indication. Active low, open drain output. Interrupt can be made sensitive to specific or all error flags (described in I^2C WRITE format section). Default is sensitive to all error flags. This output stays active until a word is read from the device.
24-33	DOUT[0..9]	O	Parallel digital video data outputs
34	NO TRS	O	Indicates presence of invalid input data, containing no timing reference signal (TRS). Active high output which signals absence of seven consecutive valid TRSs in the incoming data. Returns to low state after seven consecutive valid TRSs occur. A valid input CLK must be present for this to operate.
35	ANC DATA	O	Ancillary data presence indication. Active high output, indicates data presence from ANC data header word to checksum word. Can be programmed through the I^2C interface to also indicate presence of TRS-ID (3FF,000,000) blocks. In this mode, output stays high for 5 words during composite video TRS-ID and 4 words during component EAV, SAV. In stand alone operation mode without I^2C Interface, this feature can be forced on ANC DATA pin by selecting address 0,1 on A1,A0 pins. (NOTE: SCL and SDA must be connected to GND when I^2C Interface is not used)
36	HSYNC	O	Horizontal sync indication. Active high, extends from EAV to SAV for component video, indicates TRS-ID location for composite video.
37	V BLANK	O	Vertical blanking interval indication. Active high during this period.
40-42	F0/HD1 F1/D1_D2, F2/NTSC_PAL	O	Field or standard indication pins. Field signals output when FIELD/$\overline{STD}$ pin is high, Video standard when FIELD/$\overline{STD}$ is low.
43,44	FL1,FL0	O	Error Flag Status. Active high outputs programmed via S0, S1 to indicate various transmission and hardware related error flags. Output flags stay active for one field.
17,39	V_{DD}	P	Power Supply. Most positive power supply connection. (+5V)
18,38	V_{SS}	P	Power Supply. Most negative power supply connection. (GND)

NOT RECOMMENDED FOR NEW DESIGNS

GS9001 - DETAILED DEVICE DESCRIPTION.

The GS9001 contains all functional blocks required to implement Error Detection and Handling according to SMPTE RP165. It also provides Field, Vertical, and Horizontal timing information as well as Ancillary Data and TRS-ID indication. The device offers standard independent operation and an I^2C serial communications interface to allow reading/writing of error flags, device configuration and video standards format. The device can also be operated in stand alone mode without the I^2C interface with error flags available on dedicated output pins. In all modes, the device latency is four clock cycles.

Automatic Standards Detection

This block analyses the incoming 8 or 10 bit data to determine whether it is component or composite. In total, six standards are automatically detected. For composite data conforming to SMPTE 259M, the Timing Reference Signal and Identification (TRS-ID) packet contains line and field information used to detect the format. For component data conforming to SMPTE 125M, the TRS-ID packets for End of Active Video (EAV)and Start of Active Video (SAV) are used to determine the format. The TRS information is then used to determine whether the composite signal is NTSC or PAL, or whether the component signal has 13.5 MHz or 18 MHz luminance samples.

Noise immunity has also been included, to ensure that momentary signal interruption does not affect the auto-standards detection function. This built in noise immunity results in delayed switching time between standards. Delays range from as little as eight lines when switching between component standards to as much as four frames when switching between PAL and NTSC composite standards. The latter delay is due to the method used to differentiate PAL and NTSC, which counts the number of lines per frame and requires four sequential frames before switching standards. Manual override of the auto-standard feature is provided via the I^2C interface, for applications where the standards recognition delay is intolerable. Standards indication is provided on multiplexed output pins or via the I^2C interface.

Control Logic

The control logic coordinates operation and extracts timing signals such as vertical blanking, horizontal sync, field ID, ancillary data indication and TRS-ID indication.

The vertical blanking interval signal is active during the digital vertical blanking period for all signal formats. The horizontal sync signal is provided as a pulse with a duration of one clock period for every TRS-ID occurrence in composite video. For component video, the horizontal sync is a positive going pulse which starts at EAV and ends at SAV. Three field ID bits (pins 40, 41, 42) indicate the two fields for component video standards, the four colour fields for composite NTSC or eight colour fields for composite PAL.

The ancillary data indication allows external circuitry to identify ancillary data in the data stream for extraction or masking.

The presence of ancillary data is indicated by a logic high that extends from the Data ID word to the Checksum word of each ancillary packet. These timing signals are available on dedicated output pins and through the I^2C communications interface.

The control logic also verifies incoming data validity by checking the occurrence of consecutive TRS-IDs. If the absence of seven consecutive TRS-IDs is detected, a “NO TRS” flag is output on pin 34. This flag is reset once seven consecutive TRS-IDs occur.

CRC Calculation

A cyclic redundancy check (CRC) is calculated for each video field according to the CRC-CCITT polynomial $X^{16}+X^{12}+X^5+1$. Separate CRCs are calculated for active picture and full field to provide an indication that active video is still intact despite possible full field errors. This allows the user to distinguish between different classes of data errors, which yields the best compromise in error detection for all types of equipment. In order to provide compatibility between 8 bit and 10 bit systems, all data words with values between $3FC_H$ and $3FF_H$ inclusive, are recoded as $3FF_H$ at the input of the polynomial generator. Start and end points for the CRC calculation are as defined in RP165 and depend on the standard and check field being calculated. Calculated CRC words can be read through the I^2C interface.

CRC Comparison

The GS9001 can be configured for transmit or receive mode. In receive mode, the calculated CRC is checked against the incoming CRC embedded in the error data packet. Any mismatch will generate status error flags to indicate transmission related error flags in either active picture, full field or both. The error flags resulting from CRC mismatch are full field error detected here (*EDH*) and active picture *EDH*.

Ancillary Checksum Verification

The ancillary data checksums are also verified to ensure data integrity. Ancillary data is preceded by the Data Header, Data ID, Block Number and Data Count. The Data Count shows the number of ancillary words contained in each ancillary data packet. A checksum is calculated for each incoming ancillary data packet and compared with the transmitted checksum. Any difference is reported as an error via the ancillary *EDH* error flag. A separate *ANC EXT* error flag is also provided to indicate corruption of the EDH data packet.

Error Flags and Formatting

This block performs the functions of error flag reporting and recoding, EDH data packet construction, programmable interrupt generation and interface with the I^2C communication block.

NOT RECOMMENDED FOR NEW DESIGNS

Error Reporting

Error reporting is meant to provide the information necessary to allow system diagnostics. There are fifteen error flags in total, which are used to identify specific error types. All flags are available to be read or overwritten via the I^2C interface. The definition of these flags and an explanation of how the device handles these flags are described below.

The acronyms used are:

EDA Error Detected Already

EDH Error Detected Here

IDH Internal device error Detected Here

IDA Internal device error Detected Already

UES Unknown Error Status

AP Active Picture

FF Full Field

1. *EDH* for AP and FF

   If the incoming CRC checkword is different from the calculated CRC checkword, the *EDH* flag is set.

2. *EDH* for Ancillary

   If the checksum for the ancillary data does not match the calculated checksum, this flag is set.

3. *EDA* for AP and FF

   This flag is generated by summing the incoming *EDA* flag with the product of the incoming *EDH* flag and the valid CRC bit. As a result, if the incoming *EDH* flag is set and the *EDA* flag has not been set, the *EDH* flag will be recoded to *EDA* and then cleared. If the incoming CRC is invalid, then the outgoing *EDA* flag will be determined by the incoming *EDA* flag only. This is to support devices in the transmission path that do not generate valid CRC,yet pass only the *EDA* flags.

4. *EDA* for Ancillary

   This flag is the sum of the in-coming *EDH* and *EDA* flags for ancillary data.

5. *IDH* for AP, FF and Ancillary

   These flags are set by the user through the I^2C serial interface. They can be used to indicate any internal device errors in the vicinity of the device. Examples could be local hardware errors such as a RAM failure or a system diagnostics failure on power-up.

6. *IDA* for AP, FF and Ancillary

   This flag is the sum of the incoming *IDH* and *IDA* flags for AP, FF and ancillary data.

7. *UES* for AP, FF and Ancillary

   UES is set if the incoming *UES* is set. Also, if the incoming data does not have an error data packet, this flag is set. This is to inform the down-stream devices that the data being sent has not been previously checked for data errors.

In addition to error flag access through the I^2C interface, selected *EDH, EDA, IDH, IDA* and *UES* flags are available on two user programmable output pins. Table 2 (on page 3) shows these error flags and the corresponding input addresses.

These flags are available for applications where access to the I^2C interface via microcontroller is not possible or cost effective. These flags give the user immediate warning of transmission related errors either locally or from upstream equipment.

In situations where the upstream equipment does not support EDH, a new error data packet is inserted in the data stream as specified in RP165. In this case the *UES* flag is set for active picture, full field and ancillary data. The *EDH*, *EDA* and *IDA* flags are reset for active picture and full field. For ancillary data, the *EDH* flag is still reported if there are any checksum errors and the *EDA* and *IDA* flags are reset. This is done since the checksums for ancillary data may still be valid without the presence of an error data packet in the data stream.

Transmit vs Receive Modes

The preceding description refers to the device in Receive mode. In Transmit mode, valid CRC-check words for active picture and full field are inserted and all error flags are reset.

Flag Masking

Any of the fifteen error flags can be set/reset or made transparent using the I^2C interface. Transparent flags are updated on the occurrence of data errors. Flag masking can be done only when the device is in the receive mode. During transmit mode all error flags are reset. The transmit mode would be used for source equipment and equipment that modifies or processes the data before re-serializing.

Programmable Interrupt

The interrupt output can be made sensitive to any specific or all error flags. This function is programmed using the sensitivity flags SANC, SFF and SAP as described in the section for I^2C interface WRITE format.

Errored Field Counter

This 21 bit counter can be used to count the number of fields in which data errors occur. The same set of sensitivity flags used for the programmable interrupt, also control the incrementing of this counter. This counter can be made to increment on the occurrence of any specific type of error flag in a field.

NOT RECOMMENDED FOR NEW DESIGNS

The counter can be programmed either to clear automatically when the counter status is read via the interface, or to clear when forced through the interface.

I²C Serial Communications Interface

The serial communications interface allows access to all error flags and other internal programmable functions. The Inter-Integrated Circuit (I²C) protocol is used. For information on the GS9001 I²C protocol, refer to Document 521 - 59 "Using the GS9001 EDH Coprocessor".

The slave addresses for the I²C interface are given in Table 3. Data formats for the I²C interface READ and WRITE operations are given in Tables 4 and 5.

During the stand-alone mode of operation, flag masking, video standard override and programmable interrupt features are disabled. The user can still monitor the video standard and the error flags through dedicated pins as shown in Table 2.

EDH Passthrough Mode

An EDH passthrough mode is available to aid in system diagnostics. This mode is selected by address 1,0 on A1, A0 pins. In this mode, the GS9001 will not insert a new EDH packet into the data stream. Input data is bypassed to output without modification. Error flag status available through the I²C interface and output pins, is now invalid. However, valid CRC words can be read through the I²C interface every field, for a static picture.

Table 3. I²C Slave Addresses

I²C Address is 00011A_1 A_0		
A1	A0	Function
0	0	Available Device Address
0	1	Available Device Address
1	0	EDH Passthrough Mode
1	1	Test Mode

NOTE: If an I²C interface is not used, address 0, 1 will force TRS-ID indication on the ancillary data pin. This is to facilitate applications in which TRS-ID is desired, but an I²C interface is not used. In this case, the SCL clock line must be connected to the most negative supply.

NOT RECOMMENDED FOR NEW DESIGNS

Table 4. I²C - Interface: Data Format for READ 15 Words

Word Address	Databits B7	B6	B5	B4	B3	B2	B1	B0	Comments
1	AP IDH	AP EDA	AP EDH	ANC UES	ANC IDA	ANC IDH	ANC EDA	ANC EDH	15 Error Flags (according to SMPTE RP165) see note below for flag ANC EXT
2	ANC EXT	FF UES	FF IDA	FF IDH	FF EDA	FF EDH	AP UES	AP IDA	
3	Error counter b20	b19	b18	b17	b16	NTSC PAL	HD1 D1	D1 D2	Video standard & error counter
4	Error counter b15	b14	b13	b12	b11	b10	b9	b8	Error counter 21 bits wide
5	Error counter b7	b6	b5	b4	b3	b2	b1	b0	
6	Active Picture CRC b15	b14	b13	b12	b11	b10	b9	b8	Active picture CRC 16 bits wide
7	Active Picture CRC b7	b6	b5	b4	b3	b2	b1	b0	
8	Full Field CRC b15	b14	b13	b12	b11	b10	b9	b8	Full Field CRC 16 bits wide
9	Full Field CRC b7	b6	b5	b4	b3	b2	b1	b0	
10	RW2 b3	RW2 b2	RW1 b7	RW1 b6	RW1 b5	RW1 b4	RW1 b3	RW1 b2	Bits 2 to 7 for reserved words 1 to 7
11	RW3 b5	RW3 b4	RW3 b3	RW3 b2	RW2 b7	RW2 b6	RW2 b5	RW2 b4	Example: Bit number 4 of reserved word 2 is denoted as RW2 b4
12	RW4 b7	RW4 b6	RW4 b5	RW4 b4	RW4 b3	RW4 b2	RW3 b7	RW3 b6	
13	RW6 b3	RW6 b2	RW5 b7	RW5 b6	RW5 b5	RW5 b4	RW5 b3	RW5 b2	
14	RW7 b5	RW7 b4	RW7 b3	RW7 b2	RW6 b7	RW6 b6	RW6 b5	RW6 b4	
15	0	0	0	0	0	0	RW7 b7	RW7 b6	

NOT RECOMMENDED FOR NEW DESIGNS

NOTES: The error counter is 21 bits wide and counts the number of fields that had errors. This counter can be made to increment only upon the occurrence of a specific type of flag in a field. This sensitivity is programmable through SANC,SFF & SAP class of flags (see WRITE section). ANC EXT is a flag defined to indicate any checksum error in the EDH packet.

Reserved Words 1 to 7 in an EDH packet are both readable and writable. Only bits 2 to 7 of each reserved word are available. During Write operation for every reserved word, Even Parity is added as bit 8 and bit 9 is the logical inverse of bit 8. Bits 0 and 1 are zero to maintain compatibility with 8 bit systems.

16 bit Active Picture CRC and Full Field CRC words are available for every field, through the I²C interface.

˘Table 5. I²C - Interface: Data Format for WRITE 12 Words

Word Address	Databits								Comments
	B7	B6	B5	B4	B3	B2	B1	B0	
1	AP IDH	AP EDA	AP EDH	ANC UES	ANC IDA	ANC IDH	ANC EDA	ANC EDH	15 Error Flags (according to SMPTE RPI65)
2	STICKY FLAGS	FF UES	FF IDA	FF IDH	FF EDA	FF EDH	AP UES	AP IDA	
3	MAP IDH	MAP EDA	MAP EDH	MANC UES	MANC IDA	MANC IDH	MANC EDA	MANC EDH	Mask Status for the 15 Error Flags (see Note 1)
4	MASK RW	MFF UES	MFF IDA	MFF IDH	MFF EDA	MFF EDH	MAP UES	MAP IDA	
5	SAP IDH	SAP EDA	SAP EDH	SALL UES	SANC IDA	SANC IDH	SANC EDA	SANC EDH	Sensitivity Status for the15 Error Flags (see Note 2)
6	AUTO CLR	CLR CNT	TRS SEL	SFF IDA	SFF IDH	SFF EDA	SFF EDH	SAP IDA	
7	RW1 b3	RW1 b2	0	0	SEL STD	NTSC PAL	HD1 D1	D1 D2	Standard Select (see Note 3)
8	RW2 b5	RW2 b4	RW2 b3	RW2 b2	RW1 b7	RW1 b6	RW1 b5	RW1 b4	Bits 2 to 7 for reserved words 1 to 7 Example: Bit number 4 of reserved word 2 is denoted as RW2 b4
9	RW3 b7	RW3 b6	RW3 b5	RW3 b4	RW3 b3	RW3 b2	RW2 b7	RW2 b6	
10	RW5 b3	RW5 b2	RW4 b7	RW4 b6	RW4 b5	RW4 b4	RW4 b3	RW4 b2	
11	RW6 b5	RW6 b4	RW6 b3	RW6 b2	RW5 b7	RW5 b6	RW5 b5	RW5 b4	
12	RW7 b7	RW7 b6	RW7 b5	RW7 b4	RW7 b3	RW7 b2	RW6 b7	RW6 b6	

NOTES: 1. Mask status is used for flag masking.
MASK RW is 1 to overwrite Reserved Words.
Bit STICKY FLAGS will make the flags sticky. (Flag stays set until read by I²C interface)

2. Sensitivity status defines the interrupt & error counter sensitivity. Please note for *UES* flag sensitivity, there is only one bit which is the SALL *UES* bit. This covers the *UES* bit for Ancillary, Active Picture and Full Field classes.

3. Bit SEL STD: 1 to overwrite video standard, 0 for auto standard selection
Bit NTSC/PAL: 1 for PAL (625/50) standard, 0 for NTSC (525/60) standard
Bit HD1/D1: 1 for Component 4:2:2 standard with 18Mhz Luminance, 0 for Component 4:2:2 standard with 13.5 MHz Luminance
Bit D1/D2: 1 for $4f_{SC}$ composite standard, 0 for Component 4:2:2 standard
Bit TRS SEL: 1 to force TRS-ID indication in addition to ancillary data indication on the Ancillary Data pin, (pin 35)
0 to force only ancillary indication on the ancillary data pin (pin 35)
Bit CLR CNT: 1 to clear the 'errored field counter'. 0 to let the counter count the errored fields
Bit AUTO CLR: 1 to automatically clear the 'errored field counter' after every reading of the counter status through the interface, 0 to disable this automatic clear feature
Default Status: On power-up all bits are set to zero except for the sensitivity flags which are set to one.
Stand-Alone Operation: All bits will stay at power-up initial conditions, as described above, when there is no interface connected to the device, except for the bit TRS-SEL, which can be set to one by connecting the A1and A0 pins to 0,1 respectively.

NOT RECOMMENDED FOR NEW DESIGNS

Reset and Interrupt Characteristics (V_{CC} = 5V, 0°C < T_A < 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Minimum Rest Pulse Duration	tr(min)	100	-	nS
External to Internal Reset Delay	tr_{d1}	-	12	nS
	tr_{d2}	-	3	µS
Interrupt Delay after $\overline{RSTN}$	ti_d	-	12	nS

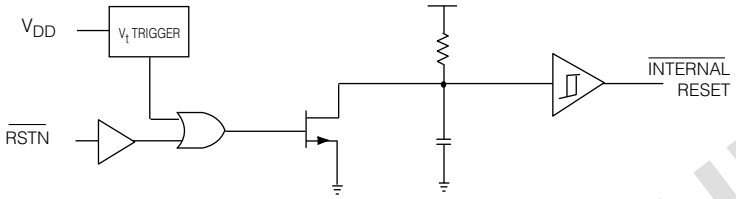


Fig. 2a GS9001 Internal Reset Circuit

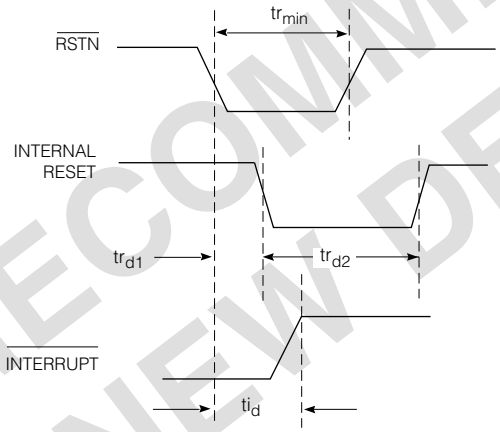
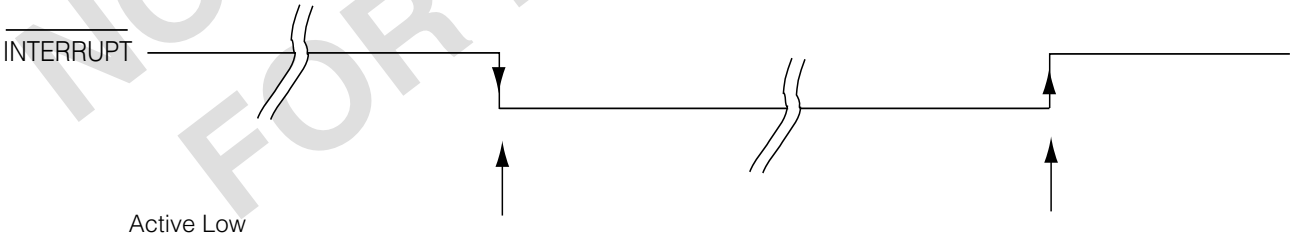


Fig. 2b Reset and Interrupt Timing



Line 11/272 - Sample 1456 - NTSC (525/60) 4:2:2
Line 11/272 - Sample 1936 - NTSC (525/60) 4:2:2,16 x 9
Line 11/272 - Sample 806 - NTSC (525/60) 4$f$sc

Line 7/320 - Sample 1456 - PAL (625/50) 4:2:2
Line 7/320 - Sample 1936 - PAL (625/50) 4:2:2,16 x 9
Line 7/320 - Sample 983 - PAL (625/50) 4$f$sc

I^2C READ
AFTER SECOND WORD
(Interrrupt is inactive after second word of the I^2C packet is read)

Fig. 2c Interrupt Timing

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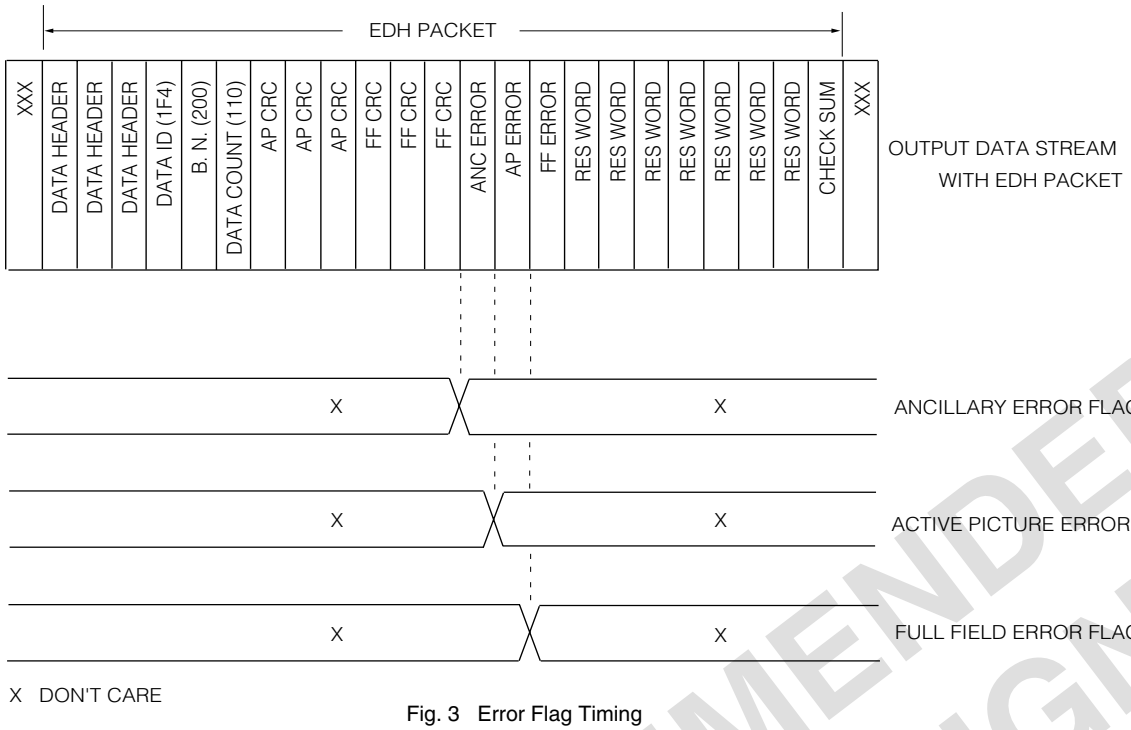


Fig. 3 Error Flag Timing

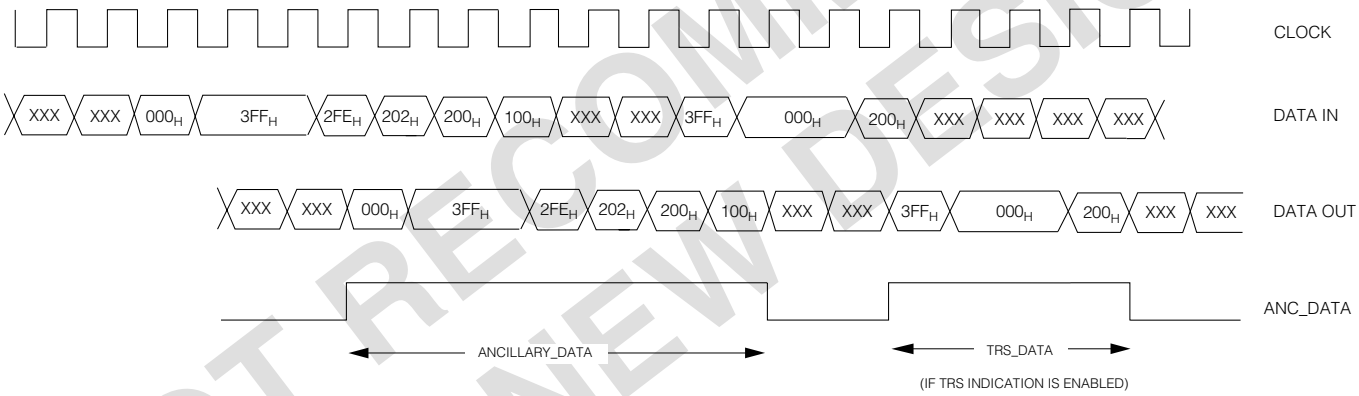


Fig. 4 Ancillary Data Indication Timing

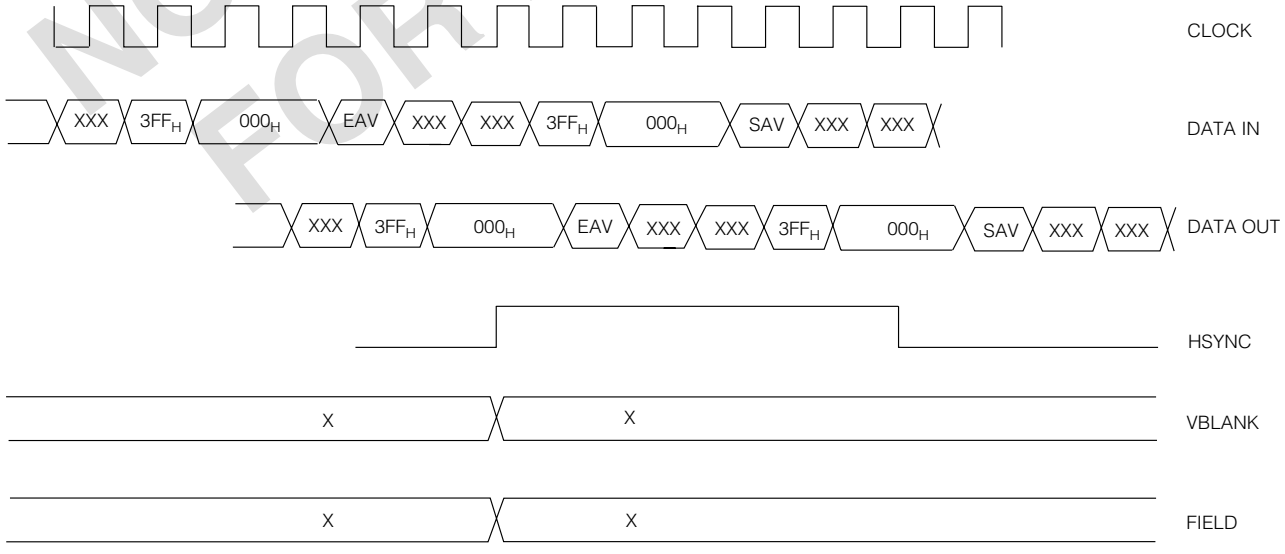


Fig. 5 Component Timing Signals

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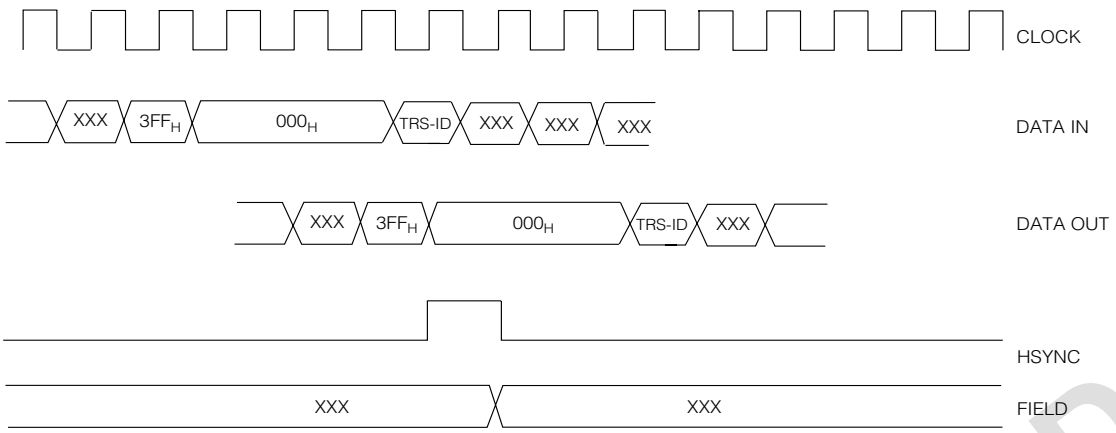
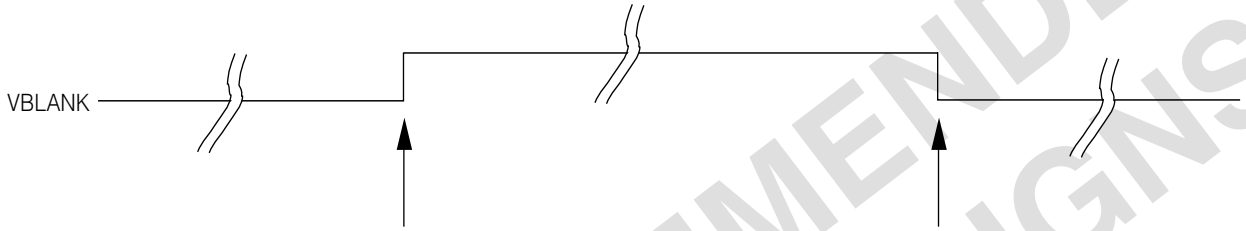


Fig. 6 Composite Timing Signals



Line 525	Sample 765 ←	(525/60) Odd Fields	→ Line 9 Sample 764
Line 263	Sample 310 ←	(525/60) Even Fields	→ Line 272 Sample 764
Line 623	Sample 379 ←	(625/50) Odd Fields	→ Line 5 Sample 944
Line 310	Sample 945 ←	(625/50) Even Fields	→ Line 317 Sample 944

Note: All sample numbers are with respect to output data.

Fig. 7 Composite VBLANK Timing

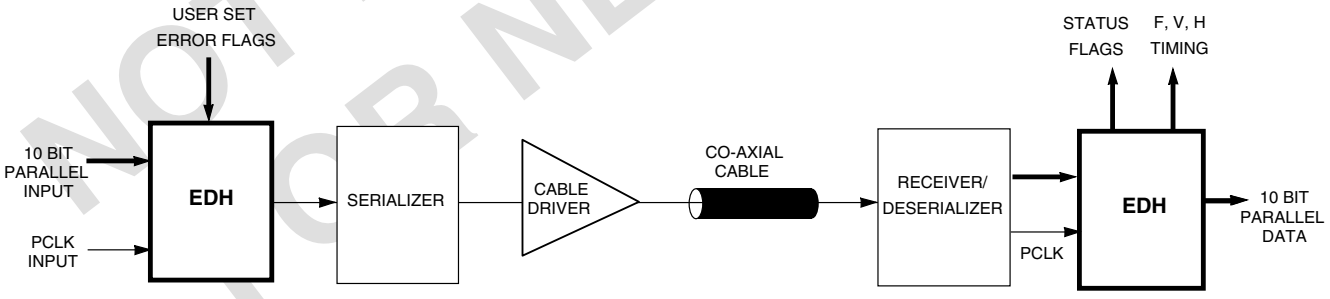


Fig. 8 GS9001 System Placement

APPLICATIONS

The GS9001 can be used on either the transmit or receive side of the serial digital interface. As shown in Figure 8, it is used as the last stage prior to serialization and immediately after deserialization.

The nature of the EDH error flags and the flexibility of use with an I^2C interface or in stand alone operation, make the GS9001 suitable for most system applications.

Conformance to SMPTE standards for EDH and digital video, ensures compatibility with any piece of source, destination or routing equipment.

Complete, System-Wide Implementation of EDH

Figure 9 shows a typical system implementation using EDH , where both equipment fault errors and transmission errors occur.

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These errors result in the transmission error flags ***EDH*** and ***EDA*** and the non-transmission related flags ***IDH*** and ***IDA***.

In Figure 9, the AES/EBU audio encoder has generated an error during the audio formatting process and reported an ***IDH*** (Internal device error Detected Here) error.

The signal from the audio encoder then experiences degradation from a faulty cable, before it reaches the router.

In this case, the cable is marginal and is producing random infrequent errors. A GS9001 device in the router flags these errors as ***EDH*** (Error Detected Here) for Active Picture, Full Field or both. Incoming ***IDH*** flags are also recoded as ***IDA*** (Internal device error Detected Already).

The next device in the chain is a distribution amplifier (DA) which is receiving its input from the router. The GS9001 device in the DA will recode the incoming ***EDH*** flag as ***EDA*** (Error Detected Already) and pass the ***IDA*** flag.

An additional transmission error occurs between the DA and the production switcher which is flagged as ***EDH***. The GS9001 in the production switcher now has a list of error flags that can be reported locally or through a communications interface to a central maintenance station.

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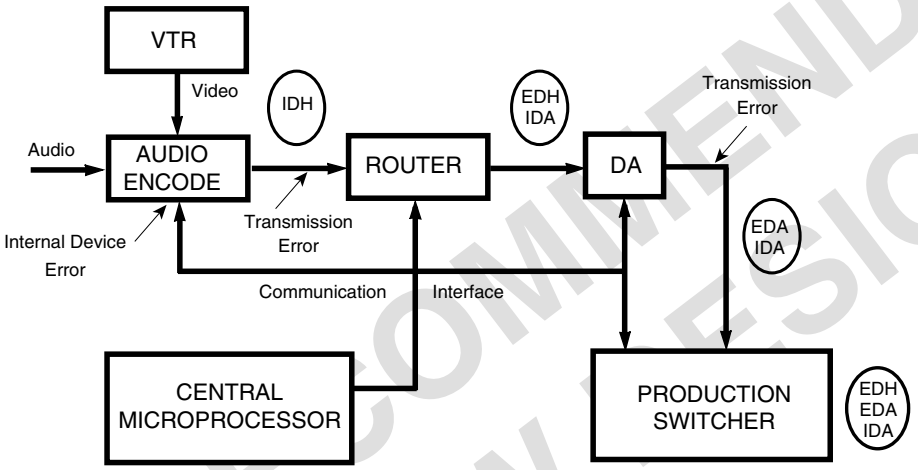


Fig. 9

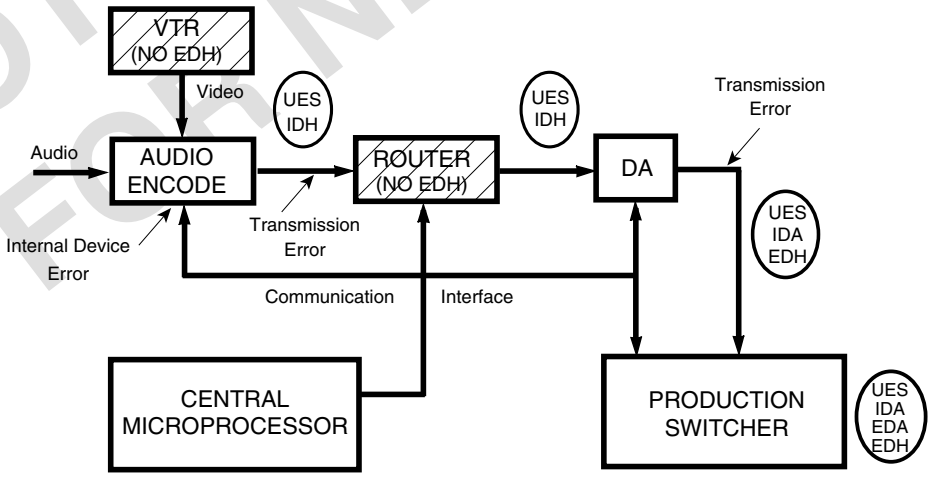


Fig. 10

Partial EDH System Implementation

In real system implementations not all equipment will have EDH capability. EDH is still useful in this environment. Figure 10 shows the same system implementation as Figure 9 except the VTR and router do not have EDH capability.

With reference to Figure 10, the audio encoder will detect the lack of imbedded EDH in the incoming video, create the EDH Packet and assert the ***UES*** (Unknown Error Status) flag.The system will now have EDH monitoring for all downstream transmission and equipment errors.

The router, without EDH, will simply pass the EDH packet unmodified to the DA which has EDH capability. Any errors reported at the DA could have occurred:

1. on the link between the audio encoder and the router,
2. in the router, or
3. on the link from the router to the DA.

Although this does not provide ideal coverage, the source of errors can still be isolated to allow the required maintenance.

Data Modification and *EDH*

It is often necessary to modify the data stream after the initial generation of the CRC words. This would occur in applications such as vertical interval timecode (VITC) or audio insertion.

If the modifying equipment employs EDH on the output, a new CRC will be calculated and inserted. If, however, the equipment has no EDH capability, the original CRC would be passed through. This would result in incorrect CRC comparison and erroneous error flag generation by the next piece of equipment.

This problem can be mitigated if the downstream equipment has the ability to override specific error flags. Unfortunately, there is no way for the downstream equipment to determine if errors were caused by data modification or transmission errors. It is therefore important that the equipment which modified the video data either implement EDH properly or remove the full field EDH packets from the data stream. Removing these packets will cause the ***UES*** flag to be asserted but this is preferable to reporting false errors.

As shown in Figure 11, the preferred way to implement EDH in equipment which modifies the data is to have an EDH coprocessor at both the input and output. The input EDH coprocessor validates the integrity of the input data. The output EDH coprocessor, set to receive mode, will pass any error flags that may have been generated upstream and recalculate any CRCs that need to be changed due to data modification. Flag masking is then enabled in this output EDH coprocessor to avoid flagging an erroneous full field error due to CRC mismatch in the modified data.

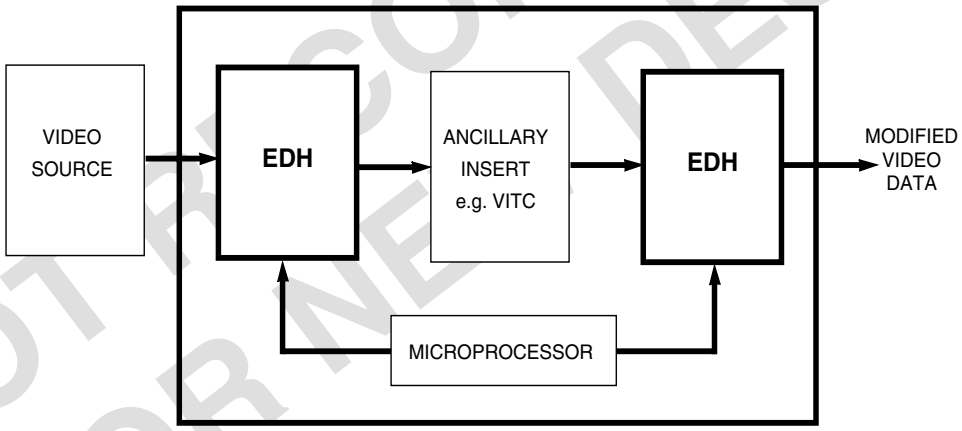


Fig. 11

NOT RECOMMENDED FOR NEW DESIGNS

References:

1. Singar Bala, Eric Fankhauser and Paul Moore,
An IC Implementation of SMPTE RP165: Error Detection and Handling,
SMPTE Journal, Volume 104, Number 7, July 1995, pp 459 - 464.

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