

TPS53685 Dual-Channel ($N + M \leq 8$ phase) D-CAP+™, Step-Down, Multiphase Controller with AMD-SVI3 and PMBus Interfaces

1 Features

- Input voltage range: 4.5 V to 17 V
- Output voltage range: 0.25 V to 5.5 V
- Dual output supporting $N+M \leq 8$ phases, $M \leq 4$ phases
- Native trans-inductor voltage regulator (TLVR) topology support
- AMD® SVI3 compliant
- Enhanced D-CAP+™ control to provide superior transient performance with excellent dynamic current sharing
- Programmable loop compensations
- Flexible phase-firing sequencing
- Individual phase current calibrations and reports
- Dynamic phase shedding with programmable current threshold for optimizing efficiency at light and heavy loads
- Fast phase-adding for undershoot reduction
- Driverless configuration for efficient high-frequency switching
- Fully compatible with TI NexFET™ power stages for high-density solutions
- Accurate, adjustable voltage positioning
- Patented AutoBalance™ phase current balancing
- Selectable per-phase current limit
- PMBus™ system interface for telemetry of voltage, current, power, temperature, and fault conditions
- 5.00 × 5.00 mm, 40-pin, 0.4 mm pitch, QFN package

2 Applications

- [Rack server](#)
- [Microserver and tower server](#)
- [High performance computing](#)
- [Baseband unit \(BBU\)](#)

3 Description

The TPS53685 is a fully AMD SVI3 compliant step-down controller with trans-inductor voltage regulator (TLVR) topology support, dual channels, built-in non-volatile memory (NVM), PMBus™ interface, and full compatible with TI NexFET™ smart power stages. Advanced control features such as D-CAP+™ architecture with undershoot reduction (USR) provide fast transient response and good current sharing, minimizing output capacitance requirements. The device also provides a novel phase interleaving strategy and dynamic phase shedding for efficiency improvements at different loads. Adjustable control of V_{CORE} slew rate and voltage positioning work with the AMD SVI3 features. In addition, the device supports the PMBus communication interface for reporting the telemetry of voltage, current, power, temperature, and fault conditions to the systems. All programmable parameters can be configured by the PMBus interface and can be stored in NVM as the new default values to minimize the external component count.

The TPS53685 device is offered in a thermally enhanced 40-pin QFN packaged and is rated to operate from -40°C to 125°C .

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
TPS53685	QFN (40)	5.00 × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

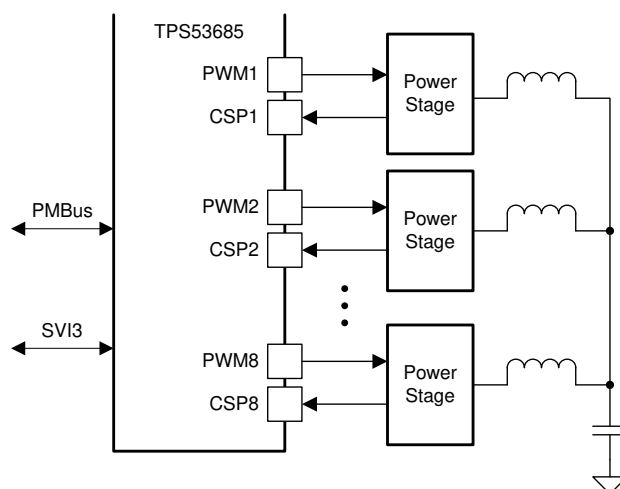


Figure 3-1. Simplified Example Application



Table of Contents

1 Features	1	5.3 Support Resources.....	3
2 Applications	1	5.4 Trademarks.....	3
3 Description	1	5.5 Electrostatic Discharge Caution.....	3
4 Revision History	2	5.6 Glossary.....	3
5 Device and Documentation Support	3	6 Mechanical, Packaging, and Orderable Information	4
5.1 Documentation Support.....	3	6.1 Tape and Reel Information.....	4
5.2 Receiving Notification of Documentation Updates.....	3		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2022	*	Initial release

5 Device and Documentation Support

5.1 Documentation Support

5.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Dual channel DCAP+ multiphase controllers: TPS53685, TPS536C5 Technical Reference Manual SLUUCN5

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

5.4 Trademarks

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PMBus™ is a trademark of SMIF, Inc..

AMD® is a registered trademark of Advanced Micro Devices, Inc..

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5.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

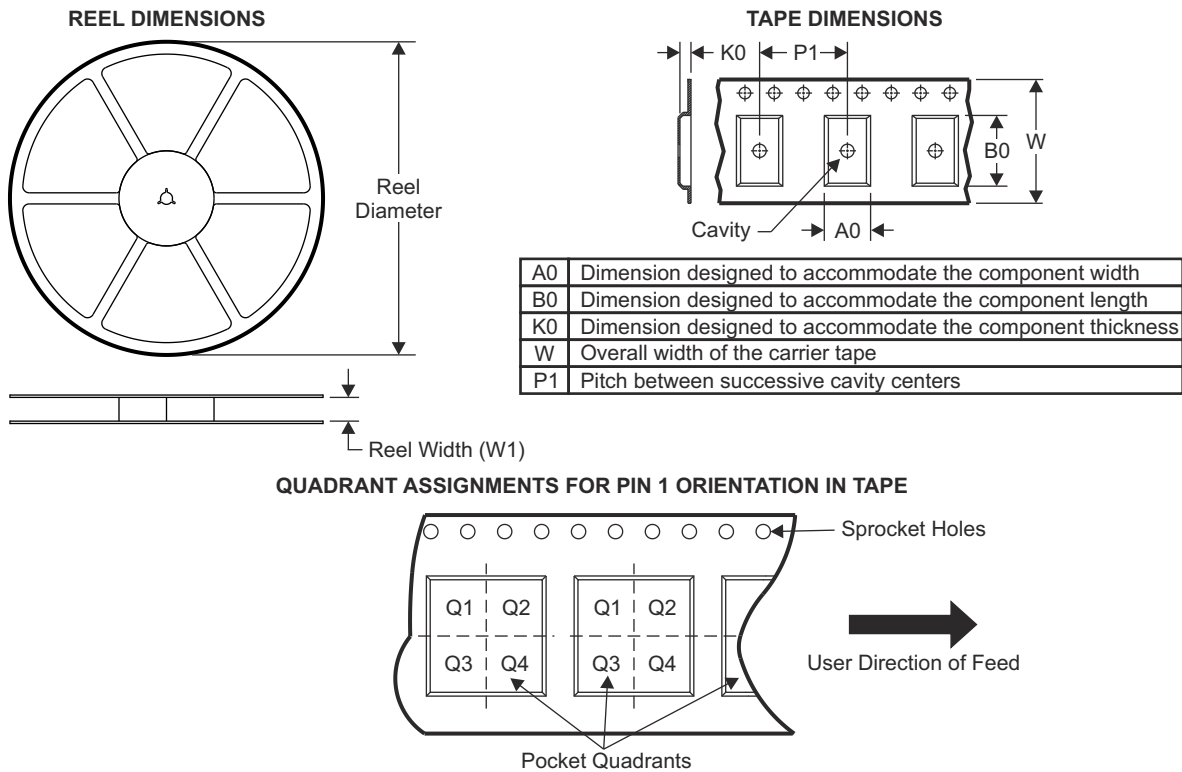
5.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

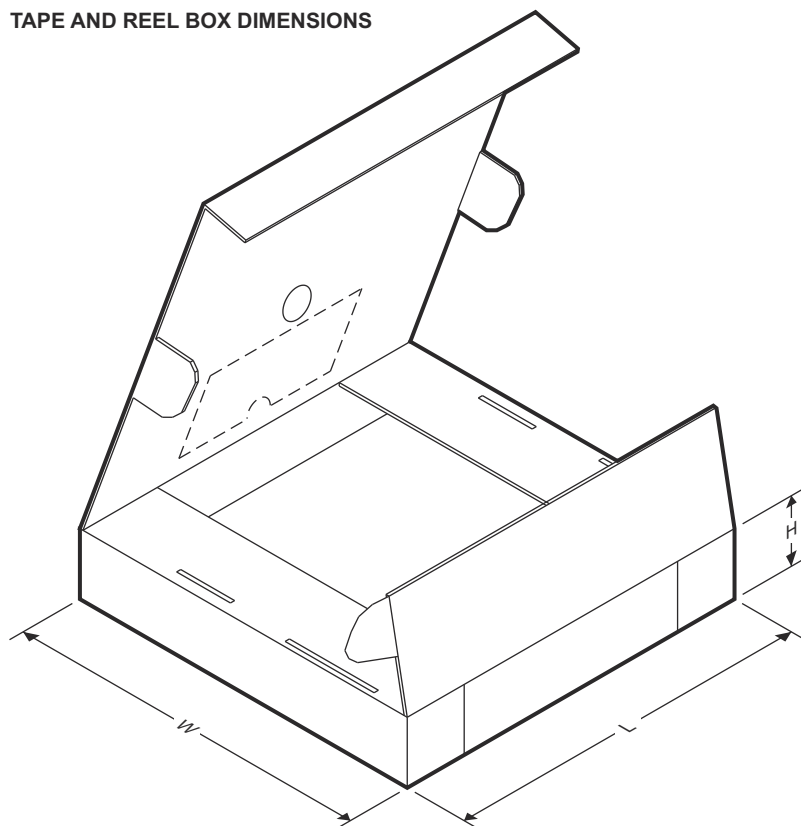
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Tape and Reel Information

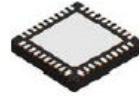


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53685RSBR	WQFN	RSB	40	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53685RSBR	WQFN	RSB	40	3000	338.0	355.0	50.0

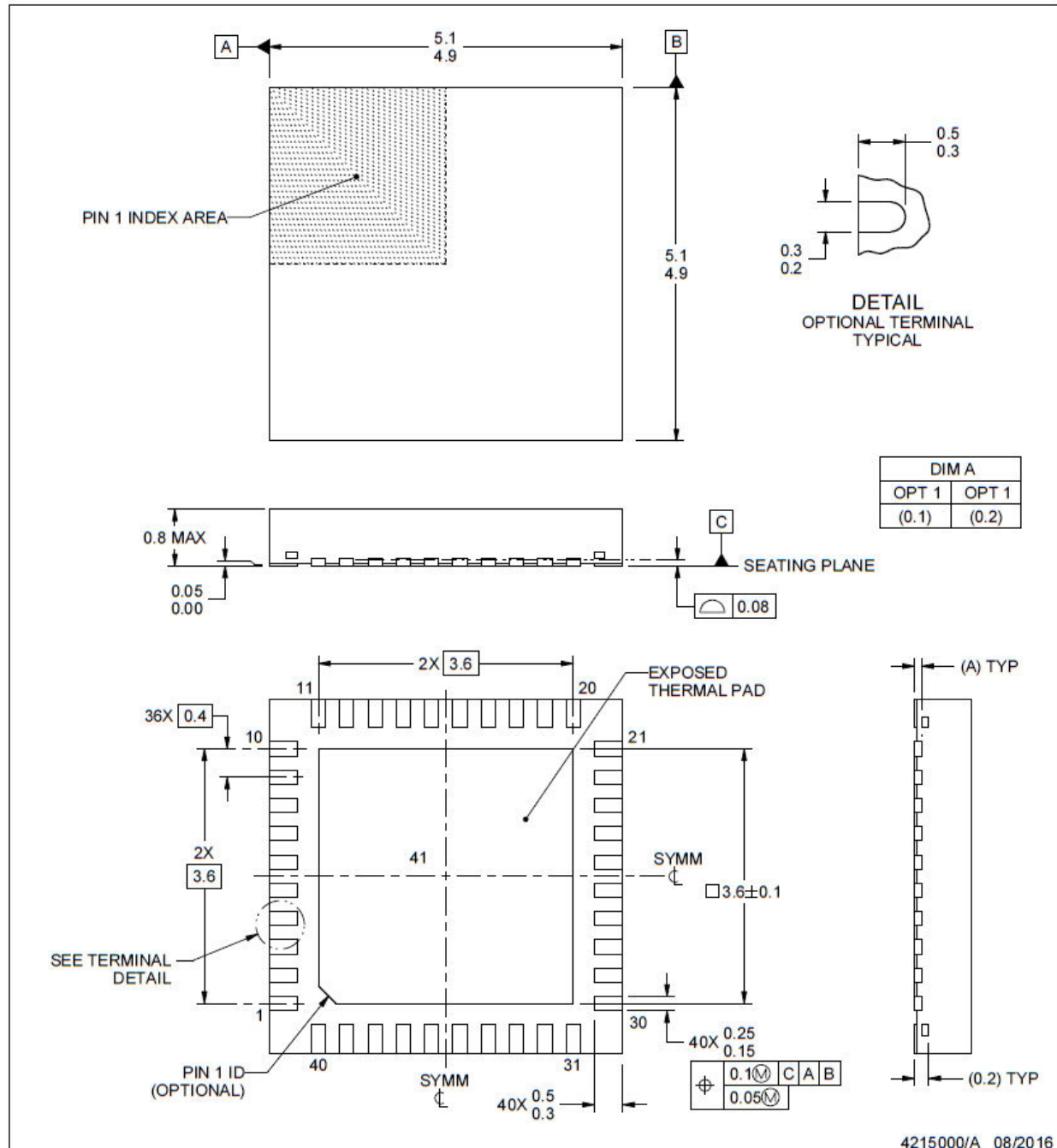


RSB0040A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

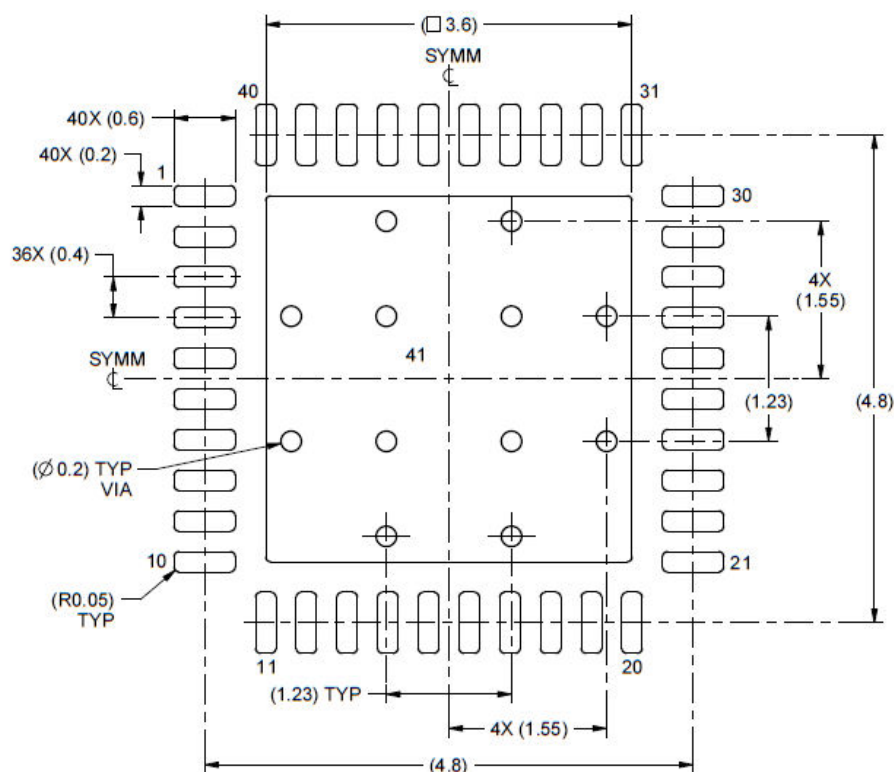
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

BOARD LAYOUT

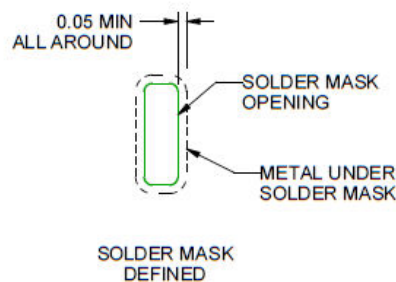
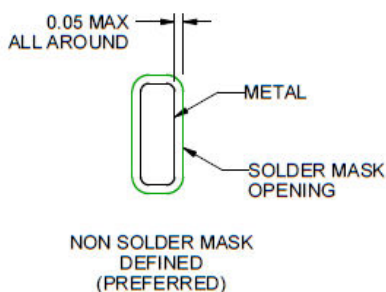
RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN
SCALE:15X



SOLDER MASK DETAILS

4215000/A 08/2016

NOTES: (continued)

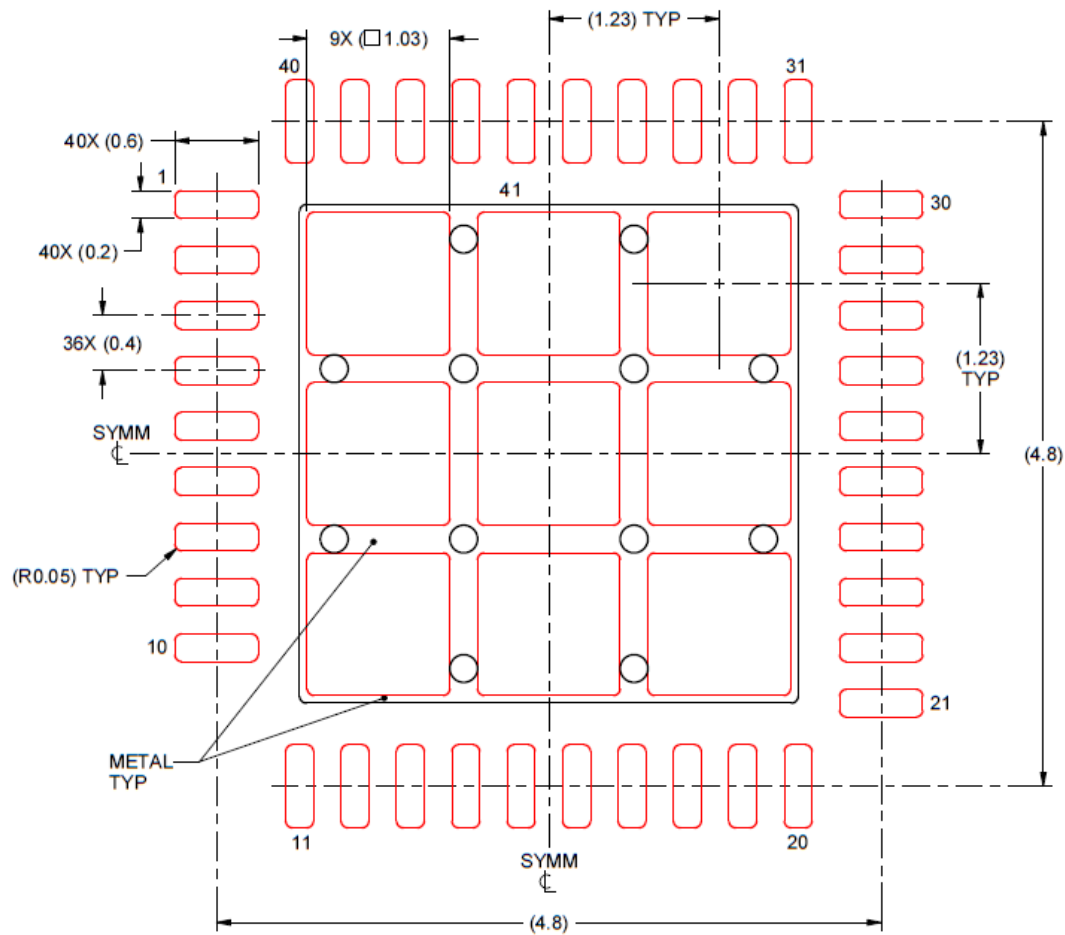
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

STENCIL DESIGN

RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4215000/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53685RSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	TPS 53685	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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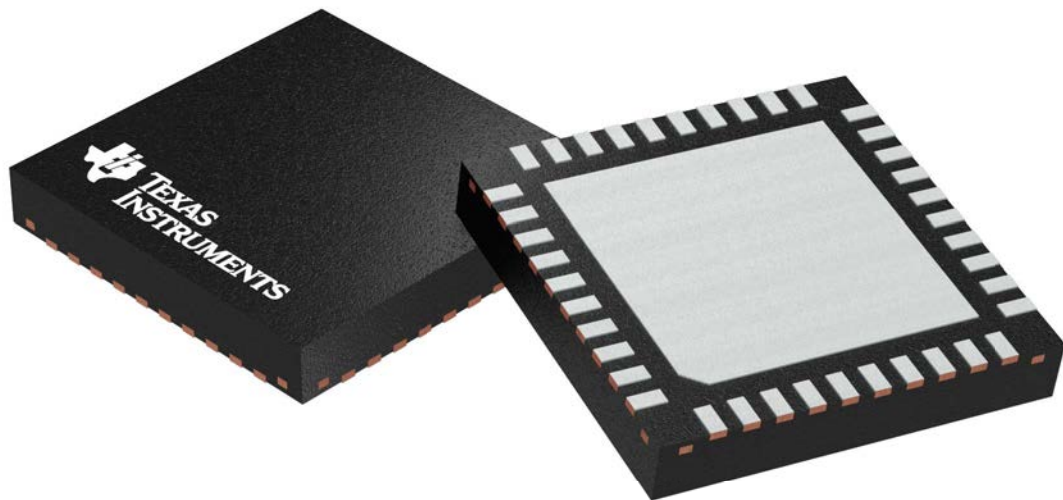
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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