

HALOGEN

FREE



8-Channel, Triple 2-Channel Multiplexers

DESCRIPTION

The DG9451, and DG9453 are high precision single and dual supply CMOS analog multiplexers. DG9451 is an 8-channel multiplexer, and the DG9453 is a triple 2-channel multiplexer or triple SPDT.

Designed to operate from a ± 2.7 V to ± 12 V single supply or from a ± 2.5 V to ± 5 V dual supplies, the DG9451, and DG9453 are fully specified at ± 12 V, ± 5 V and ± 5 V. All control logic inputs have guaranteed 1.4 V high limit when operating from ± 5 V or ± 5 V supplies and 1.65 V when operating from a ± 12 V supply.

The DG9451, and DG9453 are precision multiplexers of low leakage, low charge injection, and low parasitic capacitance. They conduct equally well in both directions, offer rail to rail analog signal handling and can be used both as multiplexers as well as de-multiplexers.

The DG9451, and DG9453 operating temperature is specified from -40 $^{\circ}$ C to +85 $^{\circ}$ C and are available in 16 pin TSSOP and the ultra compact 1.8 mm x 2.6 mm miniQFN16 packages.

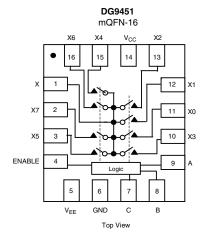
FEATURES

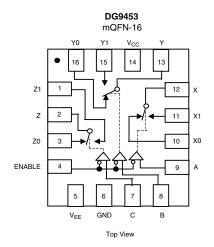
- +2.7 V to +12 V single supply operation
 ± 2.5 V to ± 5 V dual supply operation
- Fully specified at +12 V, +5 V, ± 5 V
- Low charge injection (< 0.5 pC typ.)
- High bandwidth: 270 MHz
- Low switch capacitance (C_{s(off)} 1 pF typ.)
- Good isolation and crosstalk performance (typ. -44 dB at 100 MHz)
- MiniQFN16 package (1.8 mm x 2.6 mm)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Data acquisition
- · Medical and healthcare devices
- · Control and automation equipments
- Test instruments
- Touch panels
- Consumer

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION







Device Marking: Yxx for DG9451 (miniQFN16) 4xx for DG9453 xx = Date/Lot Traceability Code

S14-2340-Rev. C, 08-Dec-14

Document Number: 65020

For technical questions, contact: powerictechsupport@vishay.com



TRUTH TA	TRUTH TABLE										
ENABLE		SELECT INPUTS		ON SWITCHES							
INPUT	С	В	Α	DG9451	DG9453						
Н	Х	X	Х	All Switches Open	All Switches Open						
L	L	L	L	X to X0	X to X0, Y to Y0, Z to Z0						
L	L	L	Н	X to X1	X to X1, Y to Y0, Z to Z0						
L	L	Н	L	X to X2	X to X0, Y to Y1, Z to Z0						
L	L	Н	Н	X to X3	X to X1, Y to Y1, Z to Z0						
L	Н	L	L	X to X4	X to X0, Y to Y0, Z to Z1						
L	Н	L	Н	X to X5	X to X1, Y to Y0, Z to Z1						
L	Н	Н	L	X to X6	X to X0, Y to Y1, Z to Z1						
L	Н	Н	Н	X to X7	X to X1, Y to Y1, Z to Z1						

ORDERING INFORMATION								
TEMP. RANGE PACKAGE PART NUMBER								
DG9451, DG9453								
-40 °C to +125 °C a	16-Pin miniQFN	DG9451EN-T1-E4						
-40 C to +125 C *	16-PIN MINIQEN	DG9453EN-T1-E4						

Note

a. -40 °C to +85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)								
PARAMETER		LIMIT	UNIT					
V+ to V-		14						
GND to V-		7	V					
Digital Inputs ^a , V _S , V _D		(V-) -0.3 to (V+) +0.3 or 30 mA, whichever occurs first						
Continuous Current (Any Terminal)		30	A					
Peak Current, S or D (Pulsed 1 ms, 10	0 % duty cycle)	100	- mA					
Storage Temperature		-65 to +150	°C					
Power Dissipation ^b	16-Pin miniQFN ^{c, d}	525	mW					
Thermal Resistance b	16-Pin miniQFN ^d	152	°C/W					
Latch-up (per JESD78)	•	> 300	mA					

Notes

- a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6.6 mW/°C above 70 °C.
- d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.



		TEST COMPLE	TIONIC			40.00+	. 105 00	40.00+	05.00	1
PARAMETER	SYMBOL	TEST CONDIT	E SPECIFIED	TEMP.b	TYP.°) +125 °C	-40 °C t	o +85 °C	UNI
TAIAMETER	OTTOL	$V_{CC} = +5 \text{ V}, V_{EE}$ $V_{IN(A, B, C \text{ AND ENABLE})} =$	_i = -5 V 1.4 V, 0.3 V ^a			MIN. d	MAX. d	MIN. d	MAX. d	0
Analog Switch		(, 5, 6, 115 2.11 (522)	<u> </u>			l	l.		l	l
Analog Signal Range e	V _{ANALOG}			Full	-	-5	5	-5	5	V
On Desistance			/ 0.1/ .0.1/	Room	66	-	100	-	100	
On-Resistance	R _{ON}	$I_S = I \text{ mA}, V_D = -3 \text{ N}$	$I_S = 1 \text{ mA}, V_D = -3 \text{ V}, 0 \text{ V}, +3 \text{ V}$		-	-	125	-	118	
On-Resistance Match	ΔR_{ON}	I _S = 1 mA, V _D =	- + 2 \/	Room	3	-	6	-	6	Ω
On-nesistance Match	ΔΠΟN	IS = I IIIA, VD =	- ± 3 V	Full	-	-	10	-	8	32
On-Resistance Flatness	R _{FLATNES}	$I_{S} = 1 \text{ mA}, V_{D} = -3 $	/ 0 \/ +3 \/	Room	10.2	-	16	-	16	
On resistance riatiless	S	15 - 1 111A, VD - 0 V	7,0 0, +0 0	Full	-	-	20	-	18	
	lo/-49			Room	± 0.02	-1	1	-1	1	
Switch Off	I _{S(off)}	V+ = 5.5 V, V- =		Full	-	-50	50	-5	5	
Leakage Current	I _{D(off)}	$V_D = \pm 4.5 \text{ V}, V_S =$	∓ 4.5 V	Room	± 0.02	-1	1	-1	1	n/
	·D(011)			Full	-	-50	50	-5	5	'"
Channel On	I _{D(on)}	V+ = 5.5 V, V- =	,	Room	± 0.02	-1	1	-1	1	
Leakage Current	·D(011)	$V_S = V_D = \pm 4$	1.5 V	Full	-	-50	50	-5	5	
Digital Control					1	ı		ı	1	
V _{IN(A, B, C and ENABLE)} Low	V_{IL}			Full	-	-	0.3	-	0.3	V
V _{IN(A, B, C and ENABLE)} High	V_{IH}			Full	-	1.4	-	1.4	-	
Input Current, V _{IN} Low	I _{IL}	V _{IN(A, B, C and ENABLE)} und		Full	0.01	-1	1	-1	1	μA
Input Current, V _{IN} High	I _{IH}	V _{IN(A, B, C and ENABLE)} und		Full	0.01	-1	1	-1	1	μ,
Input Capacitance e	C _{IN}	f = 1 MHz	Z	Room	3.4	-	-	-	-	рF
Dynamic Characteristics										
Transition Time	t _{TRANS}			Room	66	-	180	-	180	
Transition Time	t _{ON}	$R_L = 300 \Omega, C_L = 35 pF$		Full	-	-	218	-	207	ns
Enable Turn-On Time				Room	152	-	250	-	250	
Lilable fulli-Off fillie				Full	-	-	295	-	282	
Enable Turn-Off Time	t _{OFF}	see figure 1,	2, 3	Room	60	-	125	-	125	115
Lilable fulli-Oil fillie	OFF			Full	-	-	136	-	131	
Break-Before-Make	t _D			Room	32	-	-	-	-	
Time Delay	טי			Full	-	-	13	-	13	
	OIRR		f = 100 kHz	Room	< -90	-	-	-	-	
Off Isolation e			f = 10 MHz	Room	-65	-	-	-	-	
		$R_L = 50 \Omega, C_L = 15 pF$	f = 100 MHz	Room	-44	-	-	-	-	dE
Channel-to-Channel		11L = 30 32, OL = 10 pi	f = 100 kHz	Room	< -90	-	-	-	-	u L
Crosstalk e	X _{TALK}		f = 10 MHz	Room	-74	-	-	-	-	
			f = 100 MHz	Room	-44	-	-	-	-	
Bandwith, 3 dB	BW	$R_L = 50 \Omega$	DG9451	Room	270	-	-	-	-	МН
·			DG9453	Room	525	-	-	-	-	
Charge Injection e	Q	$V_g = 0 \text{ V}, R_g = 0 \Omega,$		Room	0.20	-	-	-	-	рC
Source Off Capacitance e	C _{S(off)}	f = 1 MHz	DG9451	Room	1	-	-	-	-	
Course on Supusitarios	9 5(011)	1 - 1 111112	DG9453	Room	1	-	-	-	-	
Drain Off Capacitance e	$C_{D(off)}$	f = 1 MHz	DG9451	Room	10	-	-	-	-	рF
Drain On Oapacitance	Ου(οπ)	1 – 1 1011 12	DG9453	Room	3	-	-	-	-	Pi
Channel On Capacitance e	C _{D(on)}	f = 1 MHz	DG9451	Room	16	-	-	-	-	
Chamiler on Supasitance	OD(on)		DG9453	Room	8	-	-	-	-	
Total Harmonic Distortion e	THD	Signal = 1 V_{RMS} , 20 Hz to 20 kHz, R_L = 600 Ω		Room	0.01	-	-	-	-	%
Dower Supplies		20 1 12 10 20 K112, F	ı_ — 000 <u>\$2</u>		<u> </u>					
Power Supplies		l		D	0.05					
Power Supply Current	l+			Room	0.05	-	10	-	10	
		., =	<i>5</i>	Full	- 0.05	-	10	-	10	
Negative Supply Current	l-	$V_{CC} = +5 \text{ V}, V_{EE}$	= -5 V = 0 V or 5 V	Room	-0.05	-1	-	-1	-	μA
,,		V _{IN(A, B, C and ENABLE)}	= U V Or 5 V	Full	-	-10	-	-10	-	μπ
Ground Current	I_{GND}			Room	-0.05	-1	-	-1	-	
	SITE			Full	-	-10	-	-10	-	l



	TEST CONDITIONS					-40 °C to	+125 °C	-40 °C to +85 °C		
PARAMETER	SYMBOL	UNLESS OTHERWISE SPECIFIED $V_{CC} = +5 \text{ V}, V_{EE} = 0 \text{ V}$ $V_{IN(A, B, C \text{ AND ENABLE})} = 1.4 \text{ V}, 0.3 \text{ V}^a$		TEMP.b	TYP. a	MIN. d	MAX. d	MIN. d	MAX. d	UNI
Analog Switch		IN(A, B, O AND LIVABLE)	,		L					l
Analog Signal Range e	V _{ANALOG}			Full	_	0	5	0	5	V
	ANALOG			Room	105	_	165	-	165	
On-Resistance	R _{ON}	$I_S = 1 \text{ mA}, V_D = 0 V,$	+3.5 V	Full	-	-	205	-	194	
				Room	3.2	-	8	-	8	
On-Resistance Match	ΔR_{ON}	$I_S = 1 \text{ mA}, V_D = +1$	3.5 V	Full	-	_	13	-	10	Ω
				Room	17	_	26	_	26	
On-Resistance Flatness	R _{FLATNESS}	$I_{S} = 1 \text{ mA}, V_{D} = 0 \text{ V}$	/, +3 V	Full	-	_	30	_	28	
				Room	± 0.02	-1	1	-1	1	
Switch Off	I _{S(off)}	V+ = +5.5 V, V- =	- 0 \/	Full	-	-50	50	-5	5	
Leakage Current		$V_D = 1 \text{ V}/4.5 \text{ V}, V_S = 4$		Room	± 0.02	-1	1	-1	1	
· ·	I _{D(off)}	, ,		Full	- 0.02	-50	50	-5	5	nA
Channel On		V	0.1/	Room	± 0.02	-1	1	-1	1	
Leakage Current	I _{D(on)}	V+ = +5.5 V, V- = V _D = V _S = 1 V/4.		Full	± 0.02	-50	50	-1 -5	5	
Digital Control		10 13 17 11		ruii		-30	30	-5	J 3	
				E. II	l <u>-</u>		0.0		0.0	l
V _{IN(A, B, C and ENABLE)} Low	V _{IL}			Full	-	- 1 1	0.3		0.3	V
V _{IN(A, B, C and ENABLE)} High	V _{IH}	V		Full		1.4	-	1.4	_	
Input Current, V _{IN} Low	IL .	V _{IN(A, B, C and ENABLE)} unde	Full	0.01	-1	1	-1	1	μΑ	
Input Current, V _{IN} High	IH	V _{IN(A, B, C and ENABLE)} unde	r test = 1.4 V	Full	0.01	-1	1	-1	1	
Dynamic Characteristics	<u>;</u>			_	T		T	Ī		ı
Transition Time	t _{TRANS}		Room	79	-	205	-	205		
	110410			Full	-	-	295	-	285	
Enable Turn-On Time	ton			Room	220	-	335	-	335	ns
	-010	$R_L = 300 \Omega, C_L = 35 pF$		Full	-	-	403	-	393	
Enable Turn-Off Time	t _{OFF}	See Figure 1, 2	Room	93	-	150	-	150		
Enable rum on mine	OFF		Full	-	-	173	-	163		
Break-Before-Make	+_			Room	36	-	-	-	-	
Time Delay	t _D			Full	-	-	20	-	20	
Charge Injection ^e	Q	$V_g = 0 \text{ V}, R_g = 0 \Omega, C$	C _L = 1 nF	Full	0.81	-	-	-	-	рС
Off Isolation e	OIRR	$R_L = 50 \Omega, C_L = 1$	E nE	Room	< -90	-	-	-	-	
Channel-to-Channel Crosstalk ^e	X _{TALK}	f = 100 kHz	5 pr	Room	< -90	ı	-	-	-	dB
Dynamic Characteristics	š									
Source Off Capacitance e	Ca., 10	f = 1 MHz	DG9451	Room	1	-	-	-	-	
Source On Capacitance	C _{S(off)}	1 = 1 101112	DG9453	Room	1	ı	-	-	-	
Drain Off Capacitance e		f = 1 MHz	DG9451	Room	11	-	-	-	-	
Drain On Capacitance	$C_{D(off)}$	I = I IVITZ	DG9453	Room	3	-	-	-	-	pF
		f _ 1 MU=	DG9451	Room	17	-	-	-	-	
Channel On Canacitance 6	. , .	f = 1 MHz DG9453		Room	9	-	-	-	-	
Channel On Capacitance e	C _{D(on)}		DG9433							
Channel On Capacitance e Power Supplies	G _{D(on)}		DG9433							
Power Supplies			DG9433	Room	0.05	-	1	-	1	
	C _{D(on)}		DG9433		0.05	- -	1 10	-	1 10	
Power Supplies Power Supply Current	I+			Room	0.05 - -0.05					_
Power Supplies		VIN(A, B, C and ENABLE) =		Room Full	-	-	10	-	10	μΑ
Power Supplies Power Supply Current	I+	V _{IN(A, B, C and ENABLE)} =		Room Full Room	- -0.05	- -1	10	- -1	10	μΑ



Name	SPECIFICATIONS FOR UNIPOLAR SUPPLIES										
Analog Switch Analog Switch Analog Switch Analog Switch Analog Switch Analog Signal Range * V _{ANALOG} I _S = 1 mA, V _D = 0.7 V, 6 V, 11.3 V Room 68 68 68 68 68 68 69 68 69 68 69 69							-40 °C to +125 °C		-40 °C to +85 °C		
Analog Signal Range Vanalog Rom R	PARAMETER	SYMBOL	$V_{CC} = +12 \text{ V}, V_{EE} = 0 \text{ V}$		TEMP.b	TYP. °	MAX. d	MIN. d	MIN. d		UNIT
On-Resistance Pon Is = 1 mA, Vb = 0.7 V, 6 V, 11.3 V Full - - 1.05 - 1.05	Analog Switch						,				
On-Resistance Pon Is = 1 mA, Vb = 0.7 V, 6 V, 11.3 V Full - - 1.05 - 1.05	Analog Signal Range e	V _{ANALOG}			Full	-	0	12	0	12	V
Con-Resistance Match AR _{ON} I _S = 1 mA, V _D = +0.7 V Full 143 7 7 7 7 7 7 7 7 7	On Posistance	_	L = 1 m/ \/- = 0.7 \/	6 \/ 11 2 \/	Room	68	-	105	-	105	
On-Resistance Match ΔRON S = 1 mA, VD = 40.7 V Full - - 10 - 8 Δ	On-nesistance	LON	$I_S = I IIIA, V_D = 0.7 V,$	6 V, 11.5 V	Full	-	-	143	-	137	
Part	On Posistance Match	۸D	I 1 mΛ \/ ι	0.7.1/	Room	4	-	7	-	7	0
Series Section	On-nesistance Match	ΔHON	is = 1 IIIA, VD = +	0.7 V	Full	-	-	10	-	8	52
Switch Off	On-Resistance Flatness	Bei ATMESS	lo = 1 mA Vo = 0.7 V	′ ±11 3 \/	Room	32	-	45	-	45	
Switch Off Leakage Current Injustify V	On-nesistance riatness	TIFLATNESS	15 - 1 111A, VD - 0.7 V	, +11.5 V	Full	-	-	49	-	47	
Switch Off Leakage Current V _D = 1 V/11 V, V _S = 11 V/1 V Room ± 0.02 -1 1 -1 1 1 1 1 1 1		lo/-49			Room	± 0.02					
Channel On Channel On Capacitance Cholon) Channel On Capacitance Cholon) Channel On Capacitance Cholon) Channel On Capacitance Channel On Capacitance Channel On Capacitance Channel On Capacitance Channel Characterist Channel On Capacitance Channel On Capacitance Channel On Capacitance Channel Characterist Channel On Capacitance Channel Chann	Switch Off	¹ S(off)			Full	-		50	-5	5	
Channel On Ib(on) V+ = +12 V, V- = 0 V Room ± .002	Leakage Current	ln/ m	$V_D = 1 \text{ V/11 V}, V_S =$	11 V/1 V	Room	± 0.02	-1	1	-1		nΔ
Leakage Current Topion VD = VS = 1 V/11 V Full - -50 50 -5 5 5		'D(off)			Full	-	-50	50	-5	5	11/4
Position		lp()			Room	± 0.02	-1	1		1]
Vinion Bilant Vinion Bila		'D(ON)	$V_{\rm D} = V_{\rm S} = 1 \text{ V/1}$	1 V	Full	-	-50	50	-5	5	
Vinal, B, C, and ENABLE) High Vih Vinal, B, C, and ENABLE) under test = 0.5 V Full 0.01											
\[\frac{\text{V_{NA,B, C, and ENABLE, High}}{\text{Input Current, V_{IN} Low}} \] \[\text{Input Current, V_{IN} Low} \] \[\text{Input Current, V_{IN} High} \] \[_	-		0.5		0.5	V
Input Current, V _{IN} High IH V _{INIA, B, Cand ENABLE)} under test = 1.6 V Full 0.01 -1 1 -1 1 1		V _{IH}						-	1.6	•	•
Transition Time H		_				-					υΑ
Transition Time trans t		$V_{IN(A, B, C \text{ and } ENABLE)}$ under test = 1.6 V		Full	0.01	-1	1	-1	1	μ, τ	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Dynamic Characteristics					_	1	T	1		
Enable Turn-On Time t _{ON} R _L = 300 Ω, C _L = 35 pF see figure 1, 2, 3 Room 106 - 185 - 155 Room 106 - 185 - 130 - 205 Room 106 - 185 - 130 - 205 Room 106 - 185 - 130 - 130 Room 130 Full - 1 - 144 - 137 Room 30 - 1 - 144 - 137 Room 30 - 1 - 12 - 12 Room 106 - 185 - 130 - 130 Room 106 - 185 - 130 Room 107 - 120 - 120 Room 107 Room 107 - 120 - 120 Room Room	Transition Time	TTDANG					-		-		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		TINANS					-		-		-
Facility	Enable Turn-On Time					106	-		-		
Enable Turn-Off Time topf topf topf top t							-		-		
Full - - 144 - 137	Enable Turn-Off Time						-				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$							-	144	-	137	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		tn				30	-		-	-	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	·				-	-		-	12		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Q	$V_g = 0 \text{ V}, R_g = 0 \Omega, C$	$C_L = 1 \text{ nF}$	Room	0.79	-	-	-	-	рC
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$							1	ı	1		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		OIRR	$R_1 = 50 \Omega$, $C_1 = 1$	15 pF	Room	< -90	-	-	-	-	
Source Off Capacitance C _{S(off)} f = 1 MHz DG9453 Room 1		X _{TALK}			Room	< -90	-	-	-	ı	ав
District Capacitance District Capacitanc	Source Off Capacitance e	Covers	f – 1 MHz	DG9451	Room	1	-	-	-	-	
Display Dis	Source On Capacitance	OS(off)	1 – 1 1011 12	DG9453	Room	1	-	-	-	-	
Channel On Capacitance e Channel On Capacitance	Drain Off Canacitance e	Co. "	f – 1 MHz	DG9451	Room	9	-	-	-	-	пF
Channel On Capacitance CD(on) f = 1 MHz DG9453 Room 8 - - - -	Diairi Oil Gapacitance	OD(off)	1 – 1 1011 12	DG9453	Room		-	-	-	-	PF
Power Supplies Power Supply Current I+ V _{IN(A, B, C and ENABLE)} = 0 V or 12 V Room 0.05 - 1 1 - 10 - 10 - 10 - 10	Channel On Capacitance e	C _{D(on)}	f = 1 MHz				-	-	-	-	
Power Supply Current I+ V _{IN(A, B, C and ENABLE)} = 0 V or 12 V Room 0.05 - 1 - 1	Power Supplies			2 00 100							
Full - - 10 - 10					Room	0.05	-	1	-	1	
Negative Supply Current I- V _{IN(A, B, C and ENABLE)} = 0 V or 12 V Room -0.05 -1 - -1 - -1 - -10 - -10 - -10 -	Power Supply Current	I+									
Negative Supply Current I- V _{IN(A, B, C and ENABLE)} = 0 V or 12 V Full - -10 - -10 -			. .			-0.05	-1	-	-1	-	
Ground Current love Room -0.05 -1 - -1 -	Negative Supply Current	l-	V _{IN(A, B, C and ENABLE)} = 0 V or 12 V			1		-		-	μA
Ground Current	0 10							-		-	
	Ground Current	I _{GND}			Full	-	-10	-	-10	-	

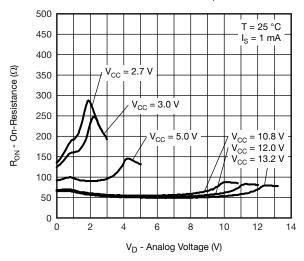
Notes

- a. V_{IN} = input voltage to perform proper function.
- b. Room -25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.

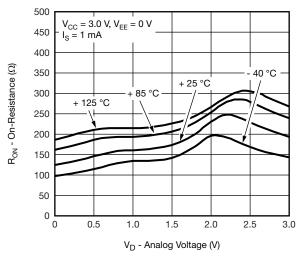
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



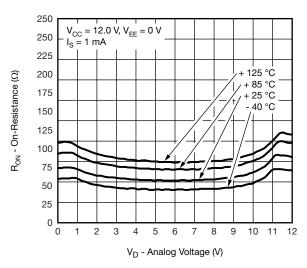
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



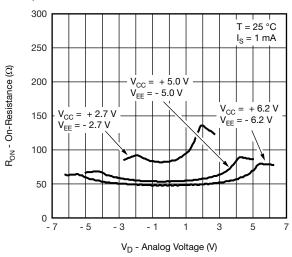
On-Resistance vs. V_D and Signal Supply Voltage



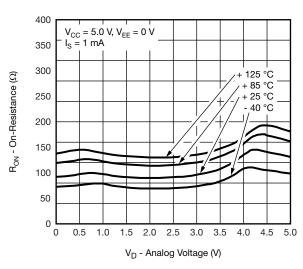
On-Resistance vs. Analog Voltage and Temperature



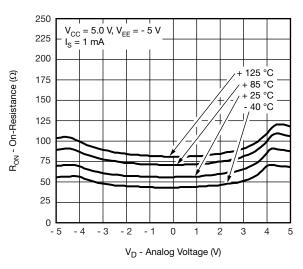
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature



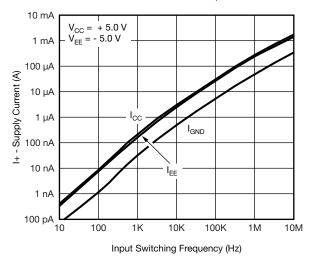
On-Resistance vs. Analog Voltage and Temperature



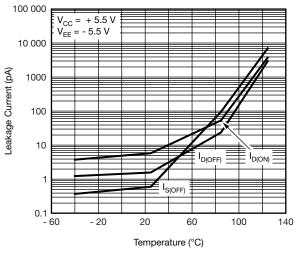
On-Resistance vs. Analog Voltage and Temperature



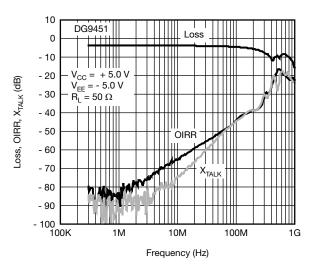
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



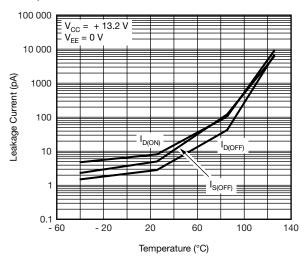
Supply Current vs. Input Switching Frequency



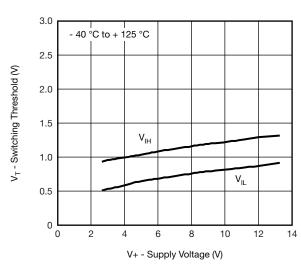
Leakage Current vs. Temperature



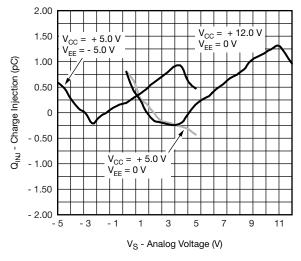
DG9451 Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



Leakage Current vs. Temperature



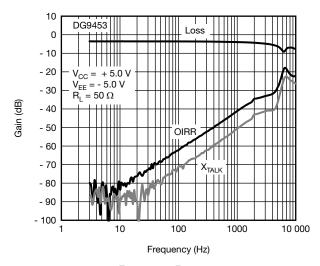
Switching Threshold vs. Supply Voltage



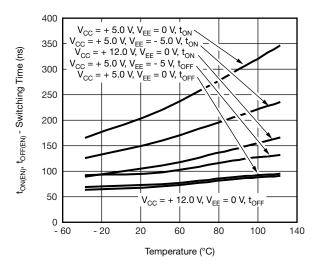
DG9451 Charge Injection vs. Analog Voltage



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

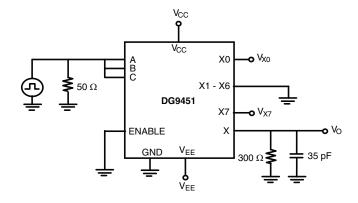


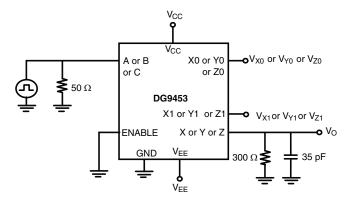
Frequency Response



Switching Time vs. Temperature

TEST CIRCUITS





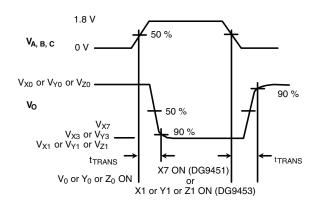


Fig. 1 - Transition Time



TEST CIRCUITS

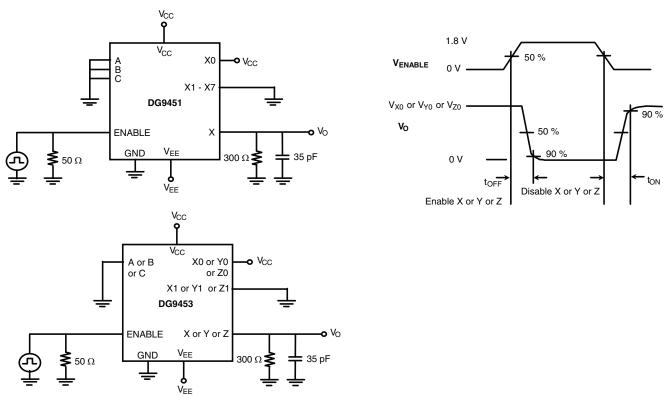


Fig. 2 - Enable Switching Time

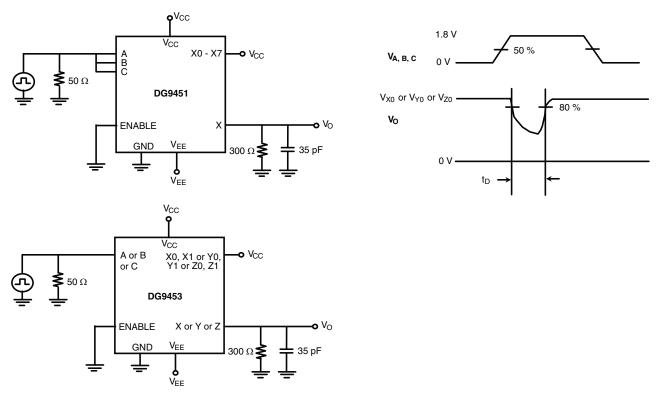


Fig. 3 - Break-Before-Make

TEST CIRCUITS

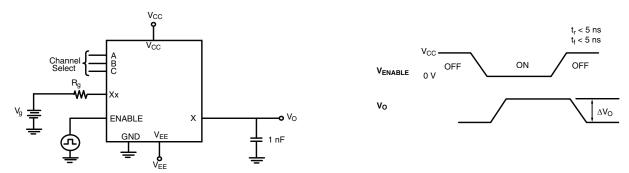
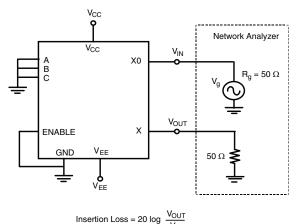
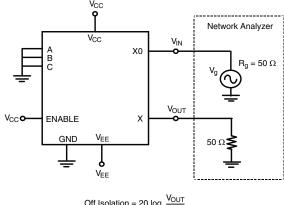


Fig. 4 - Charge Injection





Off Isolation = 20 log $\frac{V_{OUT}}{V_{IN}}$

Fig. 5 - Insertion Loss

Fig. 7 - Off Isolation

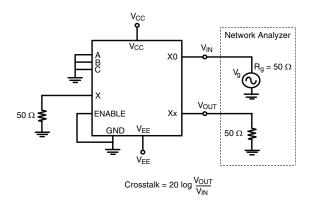


Fig. 6 - Crosstalk

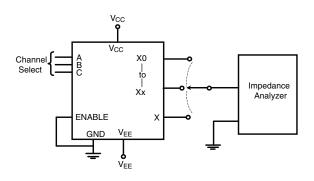
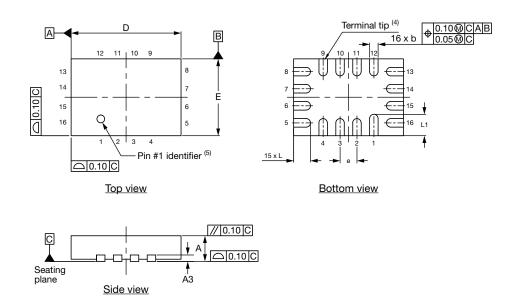


Fig. 8 - Source, Drain Capacitance

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Thin miniQFN16 Case Outline



DIMENSIONS		MILLIMETERS (1)		INCHES					
DIMENSIONS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
А	0.50	0.55	0.60	0.020	0.022	0.024			
A1	0	-	0.05	0	-	0.002			
A3		0.15 ref.			0.006 ref.				
b	0.15	0.20	0.25	0.006	0.008	0.010			
D	2.50	2.60	2.70	0.098	0.102	0.106			
е	0.40 BSC				0.016 BSC				
Е	1.70	1.80	1.90	0.067	0.071	0.075			
L	0.35	0.40	0.45	0.014	0.016	0.018			
L1	0.45	0.50	0.55	0.018	0.020	0.022			
N (3)	16			16					
Nd ⁽³⁾		4		4					
Ne ⁽³⁾		4		4					

Notes

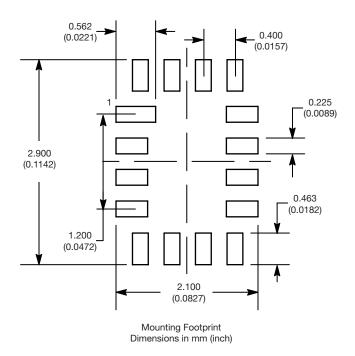
- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16

DWG: 6023



RECOMMENDED MINIMUM PADS FOR MINI QFN 16L





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