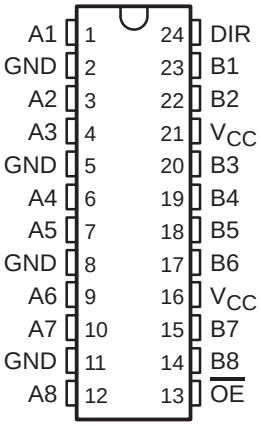
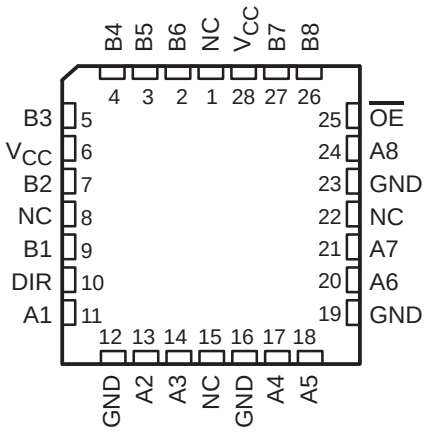
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed $V_{CC}$ and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Small-Outline (DW) Package, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) DIPs**

**SN54ABT25245 . . . JT PACKAGE**
**SN74ABT25245 . . . DW OR NT PACKAGE**
**(TOP VIEW)**




**SN54ABT25245 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The ’ABT25245 are 25-Ω octal bus transceivers designed for asynchronous communication between data buses. They improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

These devices allow noninverted data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can disable the device so that both buses are effectively isolated. When $\overline{OE}$ is low, the device is active.

These transceivers are capable of sinking 188 mA of $I_{OL}$ current, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed $V_{CC}$ and GND pins minimize switching noise for more-reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

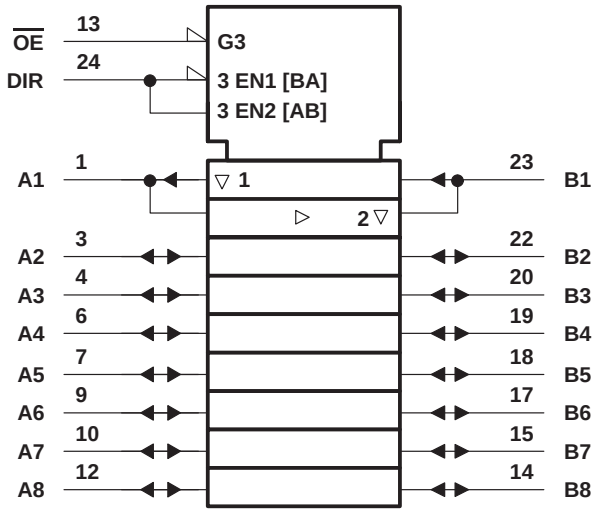
When $V_{CC}$ is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT25245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT25245 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

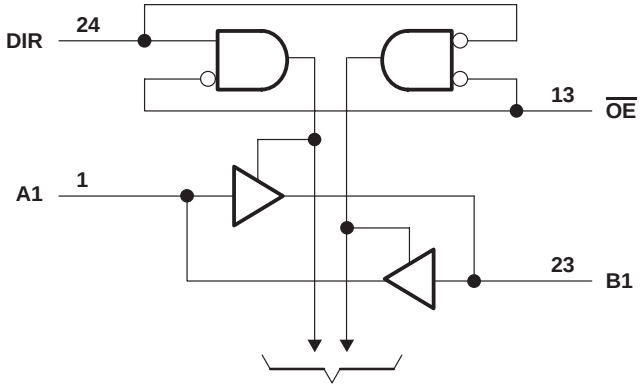
| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)




Pin numbers shown are for the DW, JT, and NT packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ . . . . . –0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Current into any output in the low state, $I_O$: SN74ABT25245 (A port) . . . . . 376 mA
SN74ABT25245 (B port) . . . . . 128 mA
Operating free-air temperature range: SN54ABT25245 . . . . . –55°C to 125°C
SN74ABT25245 . . . . . –40°C to 85°C
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package . . . . . 81°C/W
NT package . . . . . 67°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | | SN54ABT25245 | | SN74ABT25245 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{IK}$ | Input clamp current | | | | –18 | | –18 | mA |
| $I_{OH}$ | High-level output current | | A port | | –80 | | –80 | mA |
| | | | B port | | –32 | | –32 | |
| $I_{OL}$ | Low-level output current | | A port | | 188 | | 188 | mA |
| | | | B port | | 64 | | 64 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | Control inputs | | 4 | | 4 | ns/V |
| | | | A or B ports | | 10 | | 10 | |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | | 200 | | 200 | | µs/V |
| $T_A$ | Operating free-air temperature | | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ABT25245 | | | SN74ABT25245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | A port | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –3 mA | 2.7 | | | 2.7 | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –80 mA | 2.4 | | | 2.4 | | | |
| | B port | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | | |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –32 mA | 2* | | | 2 | | | |
| $V_{OL}$ | A port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 94 mA | | | 0.55 | | | 0.55 | V |
| | | | $I_{OL}$ = 188 mA | | | 0.7 | | | 0.7 | |
| | B port | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 64 mA | | | 0.55* | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | 100 | | mV |
| $I_I$ | Control inputs | $V_{CC}$ = 0 to 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 2.1 V to 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±20 | | | ±20 | |
| $I_{I(hold)}$ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 100 | | | 100 | | | µA |
| | | | $V_I$ = 2 V | –100 | | | –100 | | | |
| $I_{OZPU}$‡ | | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 0.5 V to 2.7 V, $\overline{OE}$ = X | | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$‡ | | $V_{CC}$ = 2.1 V to 0, $V_O$ = 0.5 V to 2.7 V, $\overline{OE}$ = X | | | | ±50 | | | ±50 | µA |
| $I_{OZH}$§ | | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, $\overline{OE}$ ≥ 2 V | | | | 10 | | | 10 | µA |
| $I_{OZL}$§ | | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, $\overline{OE}$ ≥ 2 V | | | | –10 | | | –10 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | ±100 | µA |
| $I_{CEX}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | | 50 | µA |
| $I_O$¶ | B port | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | | –210 | –50 | | –210 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, Outputs open, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 500 | | | 500 | µA |
| | | | Outputs low | | | 20 | | | 20 | mA |
| | | | Outputs disabled | | | 500 | | | 500 | µA |
| $\Delta I_{CC}$# | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1 | | | 1 | mA |
| $C_i$ | Control inputs | $V_{CC}$ = 5 V, | $V_I$ = $V_{CC}$ or GND | | 4 | | | 4 | | pF |
| $C_{io}$ | A or B ports | $V_{CC}$ = 5 V, | $V_O$ = $V_{CC}$ or GND | | 11.5 | | | 11.5 | | pF |

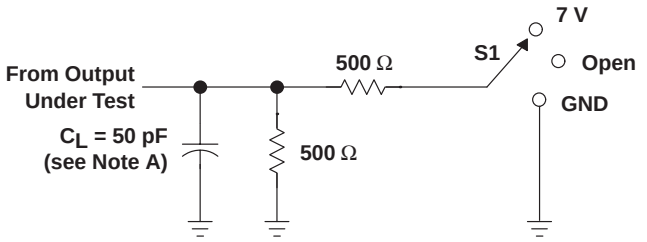


* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This parameter is characterized, but not production tested.
§ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

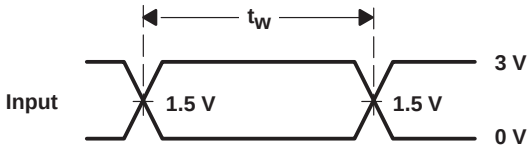
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT25245 | | SN74ABT25245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1 | 2.3 | 3.5 | 1 | | 1 | 3.9 | ns |
| $t_{PHL}$ | | | 1 | 2.4 | 3.5 | 1 | | 1 | 4.3 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1.5 | 3.7 | 5.4 | 1.5 | | 1.5 | 6.5 | ns |
| $t_{PZL}$ | | | 1.4 | 4 | 5.8 | 1.4 | | 1.4 | 6.8 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 2 | 4.3 | 6.1 | 2 | | 2 | 7.2 | ns |
| $t_{PLZ}$ | | | 2 | 3.9 | 5.8 | 2 | | 2 | 6.4 | |

## PARAMETER MEASUREMENT INFORMATION

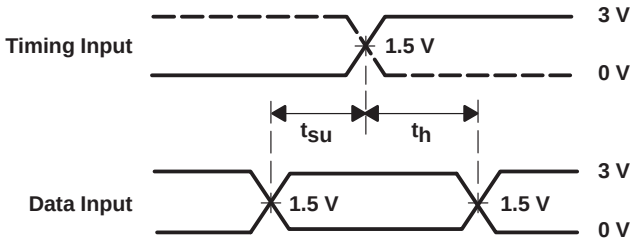



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

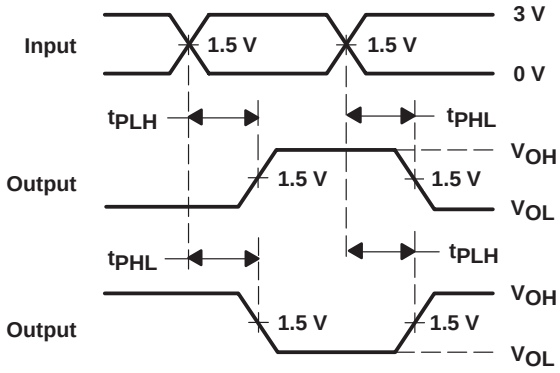
LOAD CIRCUIT



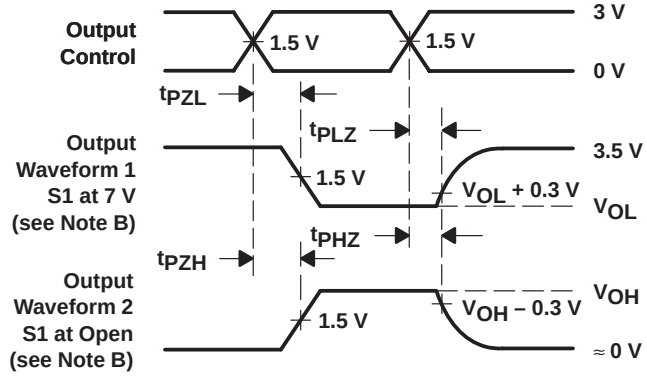

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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