

SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS401C – APRIL 1998 – REVISED MAY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $>2.3\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

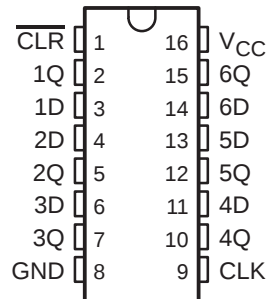
description

The 'LV174A devices are hex D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

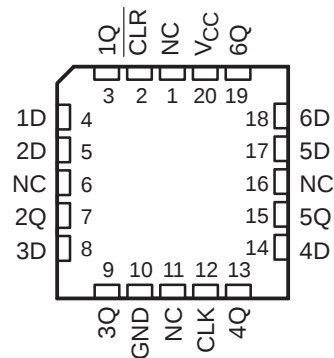
These devices are monolithic positive-edge-triggered flip-flops with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN54LV174A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV174A is characterized for operation from -40°C to 85°C .

SN54LV174A . . . J OR W PACKAGE
SN74LV174A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV174A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	L	X	Q_0



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

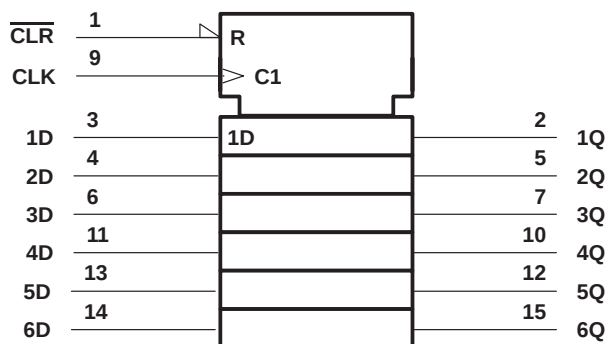
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

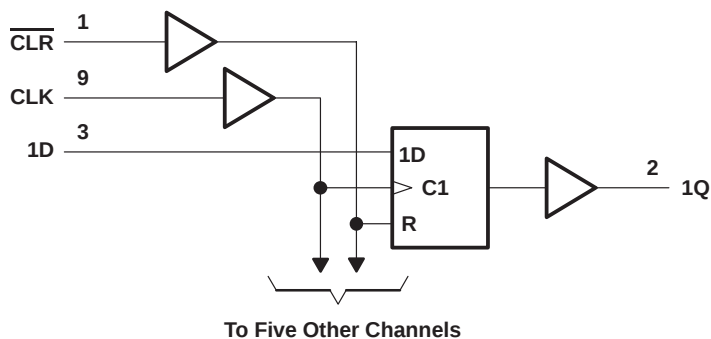
SCLS401C – APRIL 1998 – REVISED MAY 2000

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV174A, SN74LV174A

HEX D-TYPE FLIP-FLOPS

WITH CLEAR

SCLS401C – APRIL 1998 – REVISED MAY 2000

recommended operating conditions (see Note 4)

			SN54LV174A		SN74LV174A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV174A			SN74LV174A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −6 mA	3 V	2.48			2.48			
	I _{OH} = −12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	0 V to 5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.7			1.7			pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS401C – APRIL 1998 – REVISED MAY 2000

timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{CLR}}$ low	6			6.5		6.5		ns
		CLK high or low	7			7		7		
t_{su}	Setup time before CLK $\uparrow$	Data	8.5			9.5		9.5		ns
		$\overline{\text{CLR}}$ inactive	4			4		4		
t_h	Hold time, data after CLK $\uparrow$		-0.5			0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{CLR}}$ low	5			5		5		ns
		CLK high or low	5			5		5		
t_{su}	Setup time before CLK $\uparrow$	Data	5			6		6		ns
		$\overline{\text{CLR}}$ inactive	3			3		3		
t_h	Hold time, data after CLK $\uparrow$		0			0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{CLR}}$ low	5			5		5		ns
		CLK high or low	5			5		5		
t_{su}	Setup time before CLK $\uparrow$	Data	4.5			4.5		4.5		ns
		$\overline{\text{CLR}}$ inactive	2.5			2.5		2.5		
t_h	Hold time, data after CLK $\uparrow$		0.5			0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	55*	115*		50*		50		MHz
			$C_L = 50\text{ pF}$	45	90		40		40		
t_{pd}	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		6.3*	17.3*	1*	19.5*	1	19.5	ns
	CLK				8.4*	17.1*	1*	19*	1	19	
t_{pd}	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		8.2	21.9	1	23.5	1	23.5	ns
	CLK				10.8	20.6	1	23	1	23	
$t_{sk(o)}$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV174A, SN74LV174A

HEX D-TYPE FLIP-FLOPS

WITH CLEAR

SCLS401C – APRIL 1998 – REVISED MAY 2000

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}$	95*	170*		80*		80		MHz
			$C_L = 50\text{ pF}$	55	130		50		50		
t_{pd}	CLR	Q	$C_L = 15\text{ pF}$	4.5*	11.4*		1*	13.5*	1	13.5	ns
	CLK			5.8*	11*		1*	13*	1	13	
t_{pd}	CLR	Q	$C_L = 50\text{ pF}$	6	14.9		1	17	1	17	ns
	CLK			7.5	14.5		1	16.5	1	16.5	
$t_{sk(o)}$					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}$	130*	240*		110*		110		MHz
			$C_L = 50\text{ pF}$	90	180		80		80		
t_{pd}	CLR	Q	$C_L = 15\text{ pF}$	3*	7.6*		1*	9*	1	9	ns
	CLK			4.1*	7.2*		1*	8.5*	1	8.5	
t_{pd}	CLR	Q	$C_L = 50\text{ pF}$	4.2	9.6		1	11	1	11	ns
	CLK			5.5	9.2		1	10.5	1	10.5	
$t_{sk(o)}$					1					1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV174A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.34	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.3	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.02		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

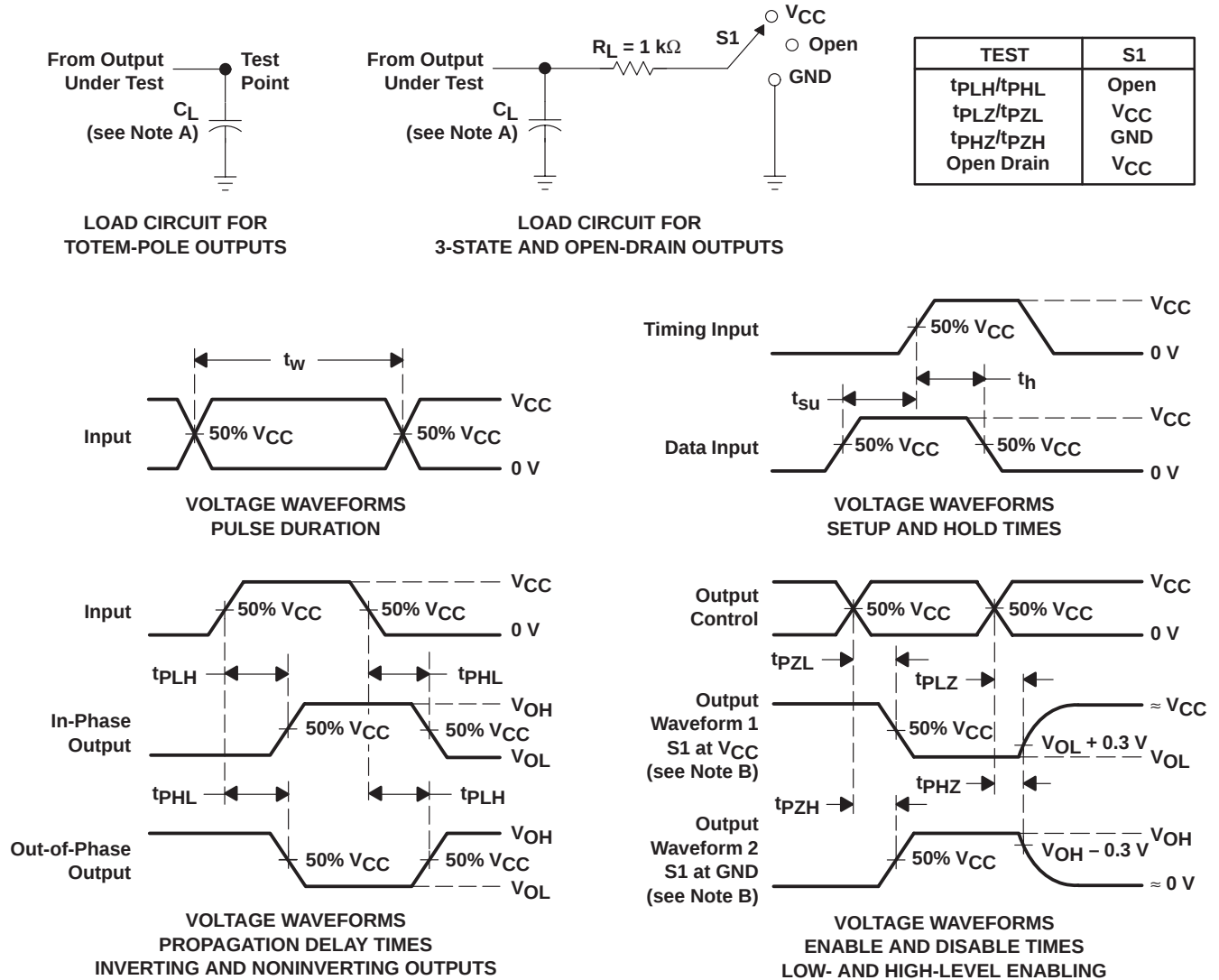
PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$	$f = 10\text{ MHz}$	3.3 V	14	pF
				5 V	15.1	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

 **TEXAS INSTRUMENTS**

THE WORLD LEADER IN DSP AND ANALOG

Products

Development Tools

Applications

GO

GO

GO

Search

GO

Advanced Search

Tech Support

TI Home

Comments

TI&ME

Site Map

Employment

TI Global

PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY](#) | [SAMPLES](#) | [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#) | [MODELS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74LV174A, Hex D-Type Flip-Flops With Clear

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74LV174A
Voltage Nodes (V)	5, 3.3, 2.5

FEATURES

▲Back to Top

- *EPIC*[™] (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- 2-V to 5.5-V V_{CC} Operation
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

EPIC is a trademark of Texas Instruments.

DESCRIPTION

▲Back to Top

The 'LV174A devices are hex D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices are monolithic positive-edge-triggered flip-flops with a direct clear (CLR\) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the

clock pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN54LV174A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LV174A is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

[▲ Back to Top](#)

To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

[▲ Back to Top](#)

Full datasheet in Acrobat PDF: [scls401c.pdf](#) (146 KB) (Updated: 05/22/2000)

Full datasheet in Zipped PostScript: [scls401c.psz](#) (148 KB)

APPLICATION NOTES

[▲ Back to Top](#)

View Application Reports for [Digital Logic](#)

- [CMOS Power Consumption and CPD Calculation](#) (SCAA035B - Updated: 06/01/1997)
- [Implications of Slow or Floating CMOS Inputs](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)

RELATED DOCUMENTS

[▲ Back to Top](#)

- [Documentation Rules \(SAP\) And Ordering Information](#) (SZZU001B, 4 KB - Updated: 05/06/1999)
- [Logic Selection Guide Second Half 2000](#) (SDYU001N, 5035 KB - Updated: 04/17/2000)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [More Power In Less Space - Technical Article](#) (SCAU001A, 850 KB - Updated: 03/01/1996)

SAMPLES

[▲ Back to Top](#)

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	SAMPLES
SN74LV174APWR	PW	16	-40 TO 85	ACTIVE	Request Samples

PRICING/AVAILABILITY

[▲ Back to Top](#)

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	BUDGETARY PRICE US\$/UNIT QTY=1000+	PACK QTY	PRICING/AVAILABILITY
SN74LV174AD	D	16	-40 TO 85	ACTIVE	0.37	40	Check stock or order
SN74LV174ADBR	DB	16	-40 TO 85	ACTIVE	0.37	2000	Check stock or order
SN74LV174ADGVR	DGV	16	-40 TO 85	ACTIVE	0.45	2000	Check stock or order
SN74LV174ADR	D	16	-40 TO	ACTIVE	0.40	2500	Check stock or order

			85				
SN74LV174APWR	<u>PW</u>	16	-40 TO 85	ACTIVE	0.37	2000	<u>Check stock or order</u>

MODELS

[▲ Back to Top](#)

- [Hex D-Type Flop-Flop With Clear](#) (SCEM133, 114 KB - Updated: 07/17/2000)
[Hex D-Type Flop-Flop With Clear](#) (SCEM133, 16 KB, ZIP - Updated: 07/17/2000)

Table Data Updated on: 11 / 17 / 2000