

BQ79656-Q1, BQ79654-Q1, BQ79652-Q1 Functional Safety-Compliant Automotive 16S/14S/12S Battery Monitor, Balancer and Integrated Hardware Protector with Integrated Current Sense

1 Features

- Qualified for automotive applications
- AEC-Q100 Qualified with the following results:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$ ambient operating temperature range
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- **Functional Safety-Compliant**
 - Developed for functional safety applications
 - Documentation to aid ISO 26262 system design
 - Systematic capability up to ASIL D
 - Hardware capability up to ASIL D
- $\pm 1.5\text{mV}$ ADC accuracy
- Pin-package and software compatible device family:
 - Stackable monitor 16S (BQ79616-Q1, BQ79656-Q1), 14S (BQ79614-Q1, BQ79654-Q1), and 12S (BQ79612-Q1, BQ79652-Q1)
 - Standalone monitor 48 V system (BQ79614-Q1)
- Supports current-sense measurement
- Built-in redundancy path for voltage and temperature and current diagnostics
- Highly accurate cell voltage measurements within $128\text{ }\mu\text{s}$ for all cell channels
- Integrated post-ADC configurable digital low-pass filters
- Supports bus bar connection and measurement
- Built-in host-controlled hardware reset to emulate POR-like device reset
- Supports internal cell balancing
 - Balancing current at 240 mA
 - Built-in balancing thermal management with automatic pause and resume control
- Isolated differential daisy chain communication with optional ring architecture
- Embedded fault signal and heartbeat through communication line
- 5 V LDO output to power external digital isolator
- UART/SPI host interface/communication bridge device BQ79600-Q1
- Built-in SPI master

2 Applications

- [Battery Management System \(BMS\) in hybrid and electric powertrain systems](#)
- [Energy storage battery packs with Battery Management Systems](#)
- E-bikes, E-Scooters

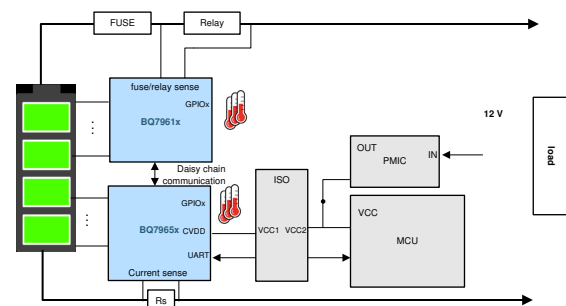
3 Description

The BQ7965x-Q1 family of devices provides high-accuracy cell voltage measurements for a minimum of 6S to a maximum of 12S (BQ79652-Q1), 14S (BQ79654-Q1), or 16S (BQ79656-Q1) battery modules in less than $200\text{ }\mu\text{s}$ while these devices also support shunt-resistor current sense measurement. The integrated front-end filters enable the system to implement with simple, low voltage raring, differential RC filters on the cell input channels. The integrated, post-ADC, low-pass filters enable filtered, DC-like, voltage measurements. This family of devices also supports integrated current sensing capabilities with option to synchronize with cell voltage measurements for better state of charge (SOC) calculation. The device supports autonomous internal cell balancing with temperature monitoring to auto-pause and resume balancing to avoid an overtemperature condition.

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
BQ79652-Q1	HTQFP (64-pin)	10.00 mm $\times$ 10.00 mm
BQ79654-Q1		
BQ79656-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified System Diagram



4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2021) to Revision A (June 2022)	Page
• Changed BQ79654-Q1 and BQ79652-Q1 from Product Preview to Production Data.....	1

5 Description (continued)

The inclusion of the isolated, bidirectional, daisy chain ports supports both capacitor- and transformer-based isolation, allowing the use of the most effective components for centralized or distribution architectures commonly found in the xEV powertrain system. This device also includes eight GPIOs or auxiliary inputs that can be used for external thermistor measurements.

Host communication to the BQ7965x-Q1 family of devices can be connected via the device's dedicated UART interface or through a communication bridge device, BQ79600. Additionally, an isolated, differential daisy-chain communication interface allows the host to communicate with the entire battery stack over a single interface. In the event of a communication line break, the daisy-chain communication interface is configurable to a ring architecture that allows the host to talk to devices at either end of the stack.

6 Device and Documentation Support

6.1 Device Support

6.1.1 Third-Party Products Disclaimer

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6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Trademarks

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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ79652PAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	BQ79652	Samples
BQ79654PAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	BQ79654	Samples
BQ79656PAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	BQ79656	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

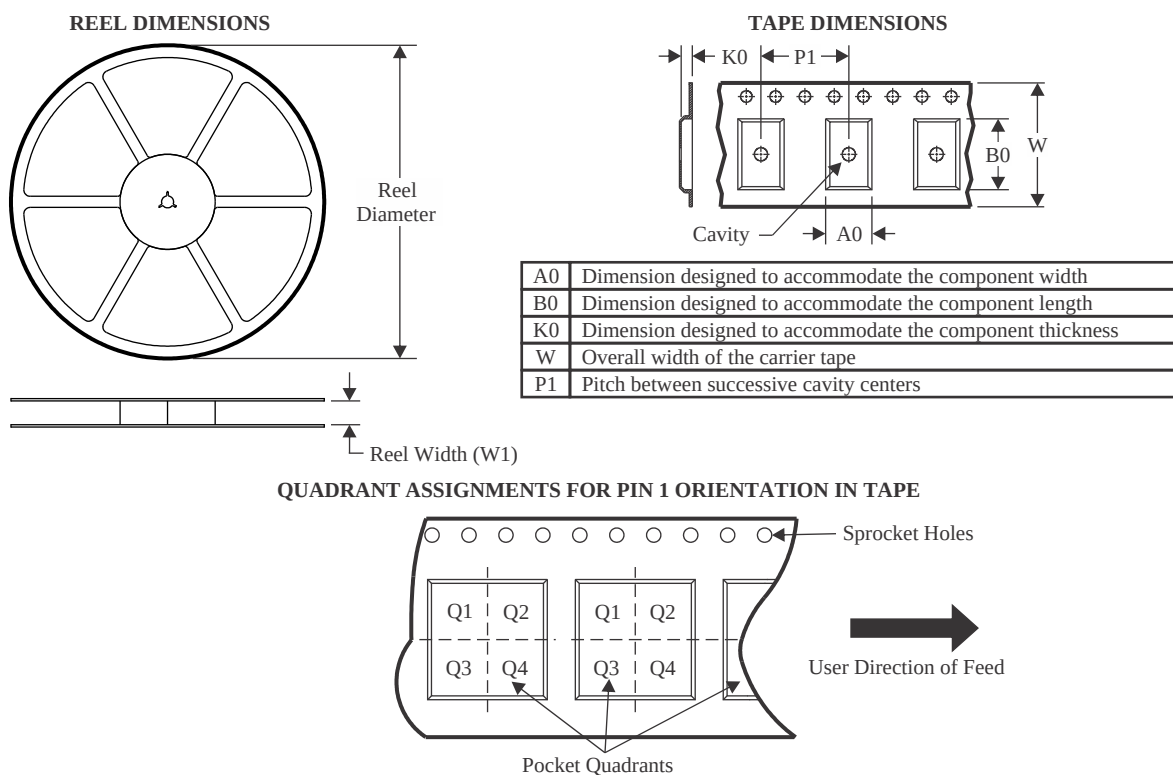
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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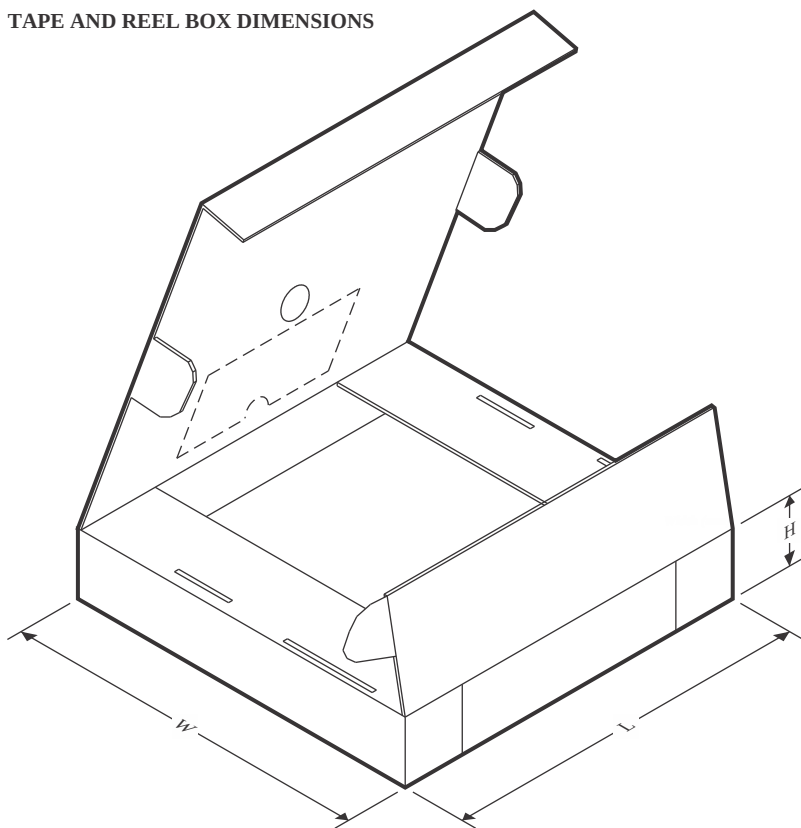
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ79652PAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
BQ79654PAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
BQ79656PAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ79652PAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0
BQ79654PAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0
BQ79656PAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0

GENERIC PACKAGE VIEW

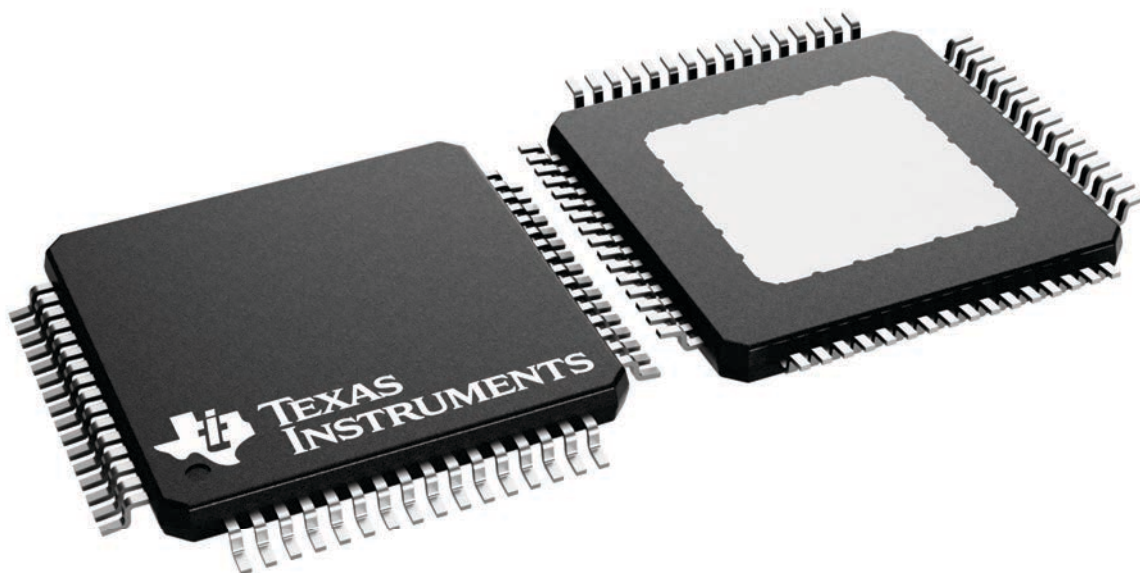
PAP 64

HTQFP - 1.2 mm max height

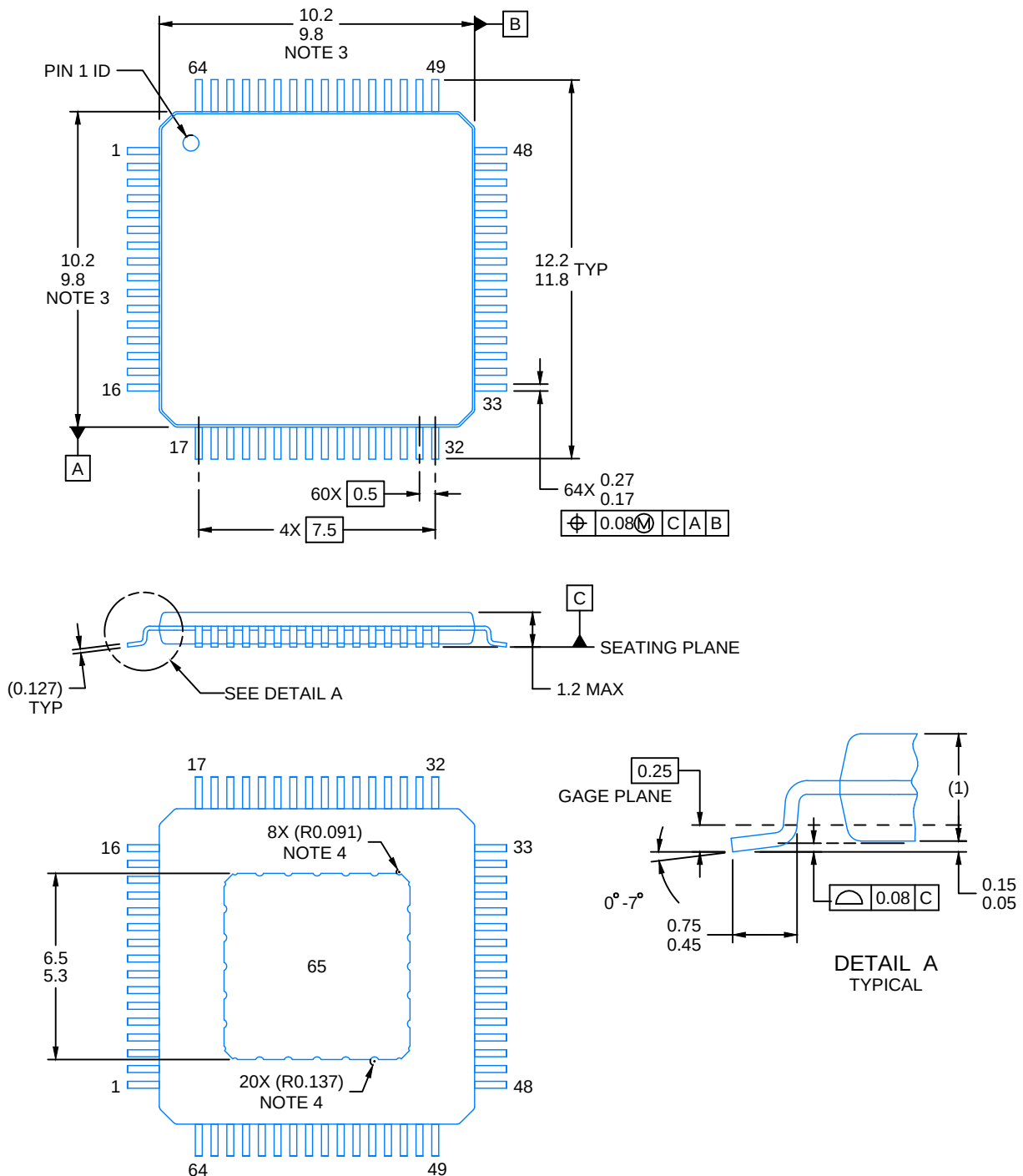
10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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NOTES:

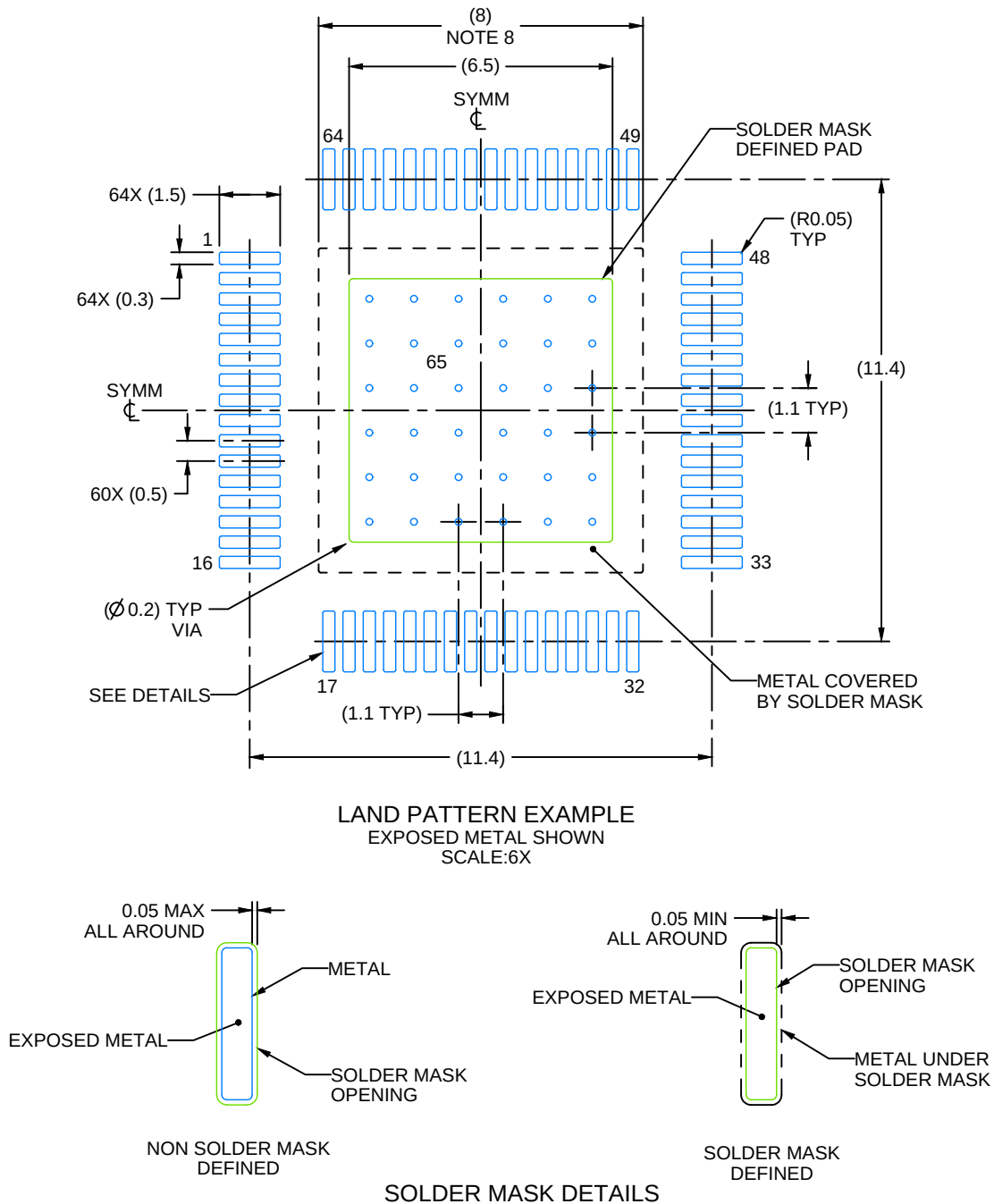
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

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PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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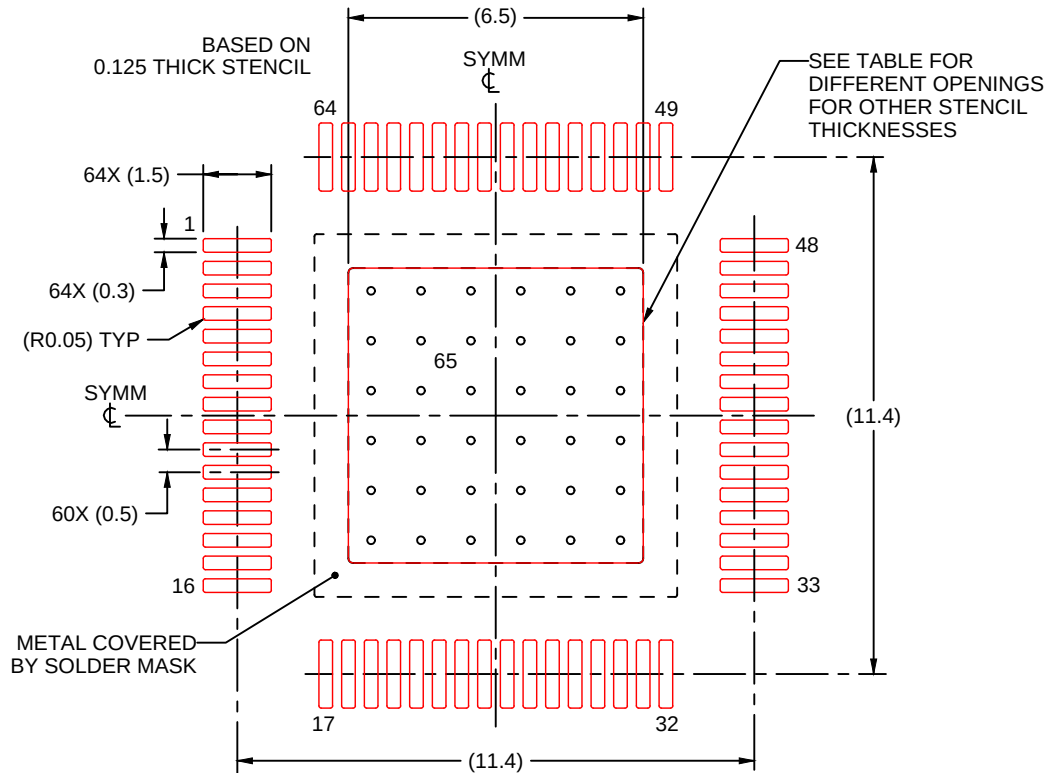
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.27 X 7.27
0.125	6.5 X 6.5 (SHOWN)
0.15	5.93 X 5.93
0.175	5.49 X 5.49

4226412/A 11/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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