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Kind regards,

Team Nexperia

DATA SHEET

74ABT16841A

20-bit bus interface latch (3-State)

Product data

2004 Feb 02

Replaces data sheet 74ABT16841A/74ABTH16841A of 2002 Dec 17

20-bit bus interface latch (3-State)

74ABT16841A

FEATURES

- High speed parallel latches
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64 mA / –32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16841A Bus interface latch is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16841A consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE HIGH-to-LOW transition, the data that meets the set-up and hold time is latched.

Data appears on the bus when the Output Enable (nOE) is LOW. When nOE is HIGH the output is in the high-impedance state.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$	3.1 2.2	ns
C_{IN}	Input capacitance	$V_I = 0\text{ V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_O = 0\text{ V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	500	μA
I_{CCL}		Outputs LOW; $V_{CC} = 5.5\text{ V}$	10	mA

ORDERING INFORMATION

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Type number	Package		
	Name	Description	Version
74ABT16841ADL	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ABT16841ADGG	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

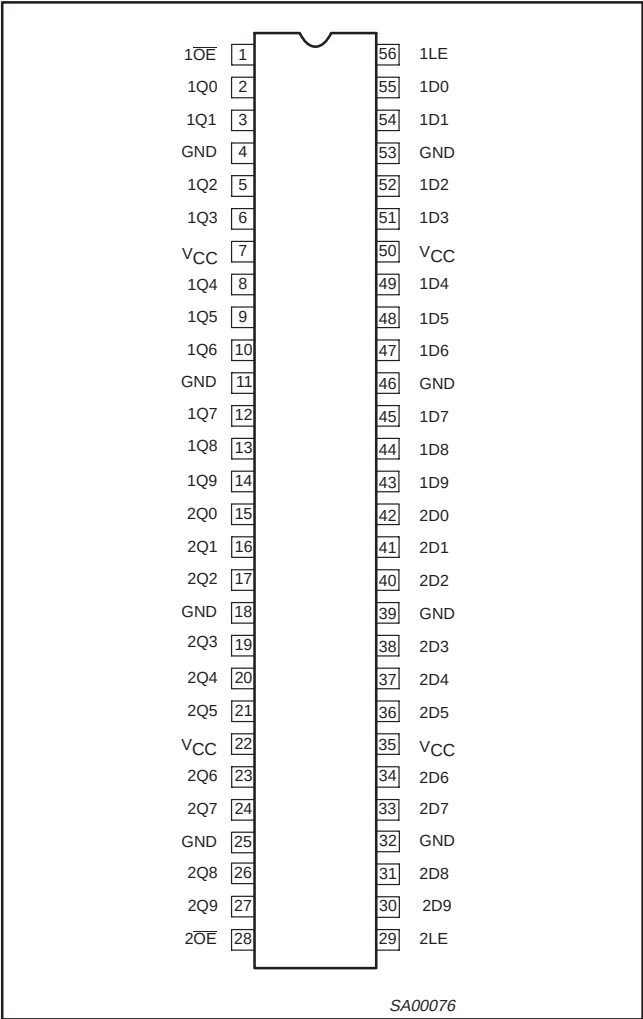
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 – 1D9 2D0 – 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
1, 28	1OE, 2OE	Output enable inputs (active-LOW)
56, 29	1LE, 2LE	Latch enable inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

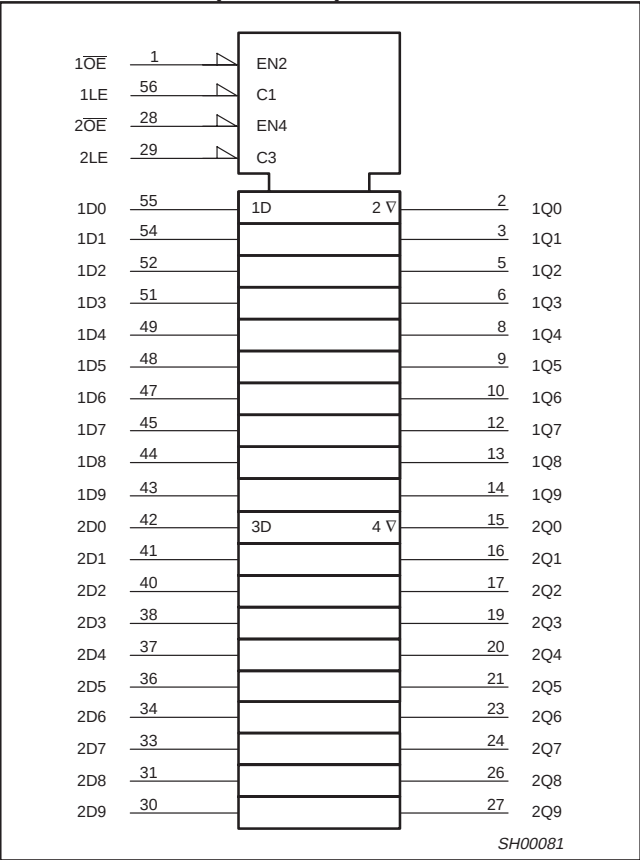
20-bit bus interface latch (3-State)

74ABT16841A

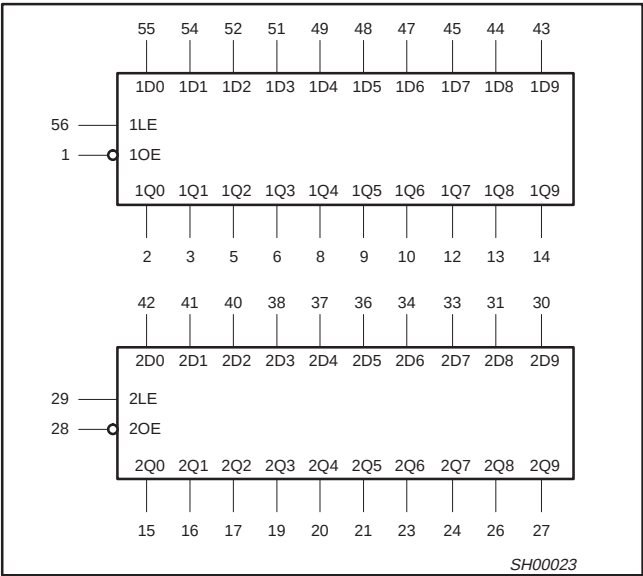
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

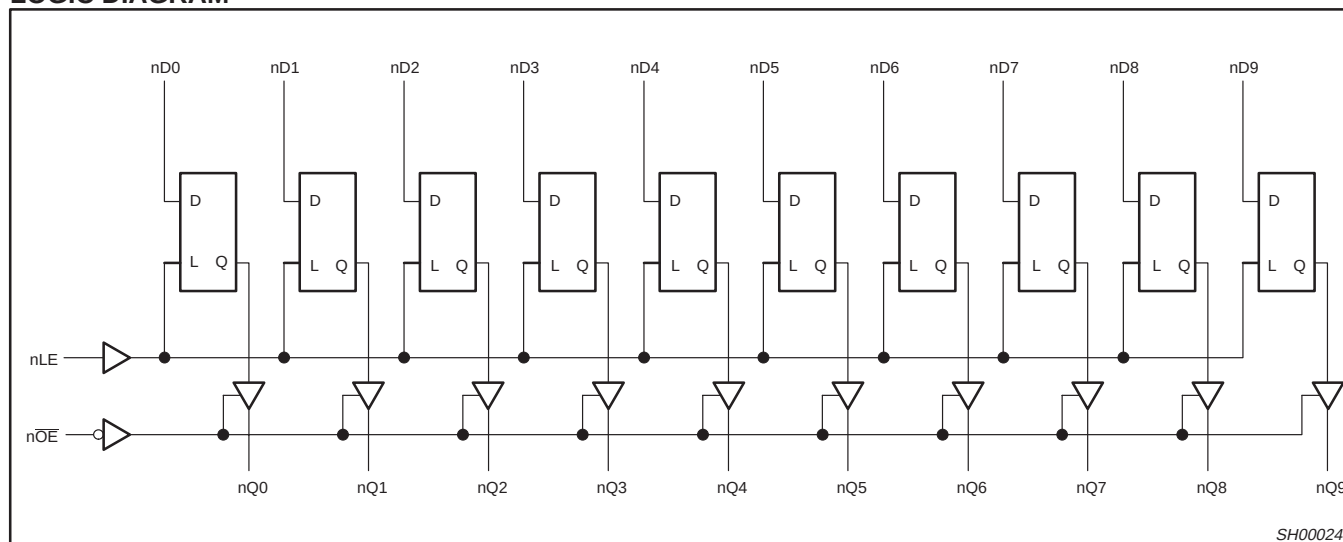
INPUTS			OUTPUTS	OPERATING MODE
nOE	nLE	nDx	nQ0 – nQ9	
L	H	L	L	Transparent
L	H	H	H	
L	↓	L	L	Latched
L	↓	H	H	
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
↓ = HIGH-to-LOW LE transition
NC= No change
X = Don't care
Z = High impedance "off" state

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LOGIC DIAGRAM

**ABSOLUTE MAXIMUM RATINGS^{1, 2}**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0 V	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0 V	−50	mA
V _{OUT}	DC output voltage ³	Output in Off or HIGH state	−0.5 to +5.5	V
I _{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	−64	
T _{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	HIGH-level input voltage	2.0	–	V
V _{IL}	LOW-level Input voltage	–	0.8	V
I _{OH}	HIGH-level output current	–	–32	mA
I _{OL}	LOW-level output current	–	64	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T _{amb}	Operating free-air temperature range	–40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25 °C			T _{amb} = −40 °C to +85 °C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = −18 mA	−	−0.9	−1.2	−	−1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; I _{OH} = −3 mA; V _I = V _{IL} or V _{IH}	2.5	2.9	−	2.5	−	V
		V _{CC} = 5.0 V; I _{OH} = −3 mA; V _I = V _{IL} or V _{IH}	3.0	3.4	−	3.0	−	V
		V _{CC} = 4.5 V; I _{OH} = −32 mA; V _I = V _{IL} or V _{IH}	2.0	2.4	−	2.0	−	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}	−	0.42	0.55	−	0.55	V
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5 V; I _O = 1 mA; V _I = GND or V _{CC}	−	0.13	0.55	−	0.55	V
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	−	±0.01	±1	−	±1.0	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V	−	±5.0	±100	−	±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1 V; V _O = 0.5 V; V _I = GND or V _{CC} ; V _{OE} = Don't care	−	±5.0	±50	−	±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5 V; V _O = 2.7 V; V _I = V _{IL} or V _{IH}	−	5.0	10	−	10	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5 V; V _O = 0.5 V; V _I = V _{IL} or V _{IH}	−	−5.0	−10	−	−10	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}	−	5.0	50	−	50	μA
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V	−50	−70	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs High, V _I = GND or V _{CC}	−	0.5	1	−	1	mA
I _{CCL}		V _{CC} = 5.5 V; Outputs Low, V _I = GND or V _{CC}	−	10	19	−	19	mA
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}	−	0.5	1	−	1	mA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND	−	0.2	1	−	1	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. From $V_{CC} = 2.1\text{ V}$ to $V_{CC} = 5\text{ V} \pm 10\%$ a transition time of up to 100 μsec is permitted.
- Unused pins at V_{CC} or GND .

AC CHARACTERISTICS

GND = 0 V, $t_R = t_F = 2.5\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V			T _{amb} = −40 °C to +85 °C V _{CC} = +5.0 V ±0.5 V		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay nDx to nQx	2	1.1 1.5	3.1 2.2	4.1 3.1	1.1 1.5	4.9 3.6	ns
t _{PLH} t _{PHL}	Propagation delay nLE to nQx	1	1.5 1.0	2.5 2.1	3.3 2.8	1.5 1.0	3.7 3.1	ns
t _{PZH} t _{PZL}	Output enable time to HIGH and LOW level	4 5	1.2 1.2	2.4 2.2	3.2 2.9	1.2 1.2	4.0 3.6	ns
t _{PHZ} t _{PLZ}	Output disable time from HIGH and LOW level	4 5	1.8 1.5	3.0 2.5	4.0 3.2	1.8 1.5	4.9 3.7	ns

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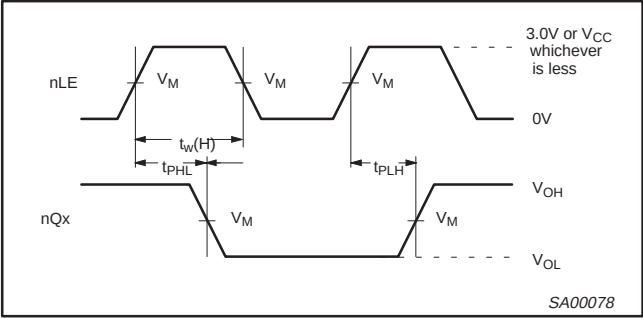
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F = 2.5\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$

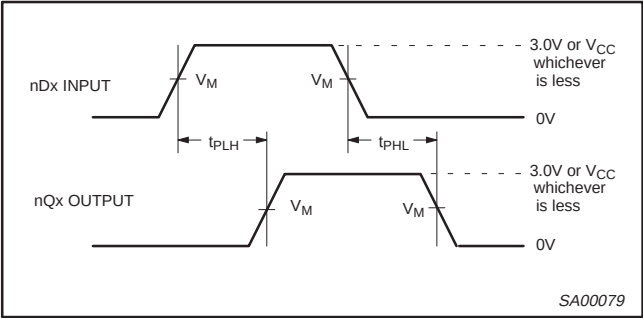
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$T_{\text{amb}} = +25\text{ }^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{ V}$		$T_{\text{amb}} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{ V } \pm 0.5\text{ V}$		
			Min	Typ	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Set-up time, HIGH or LOW nDx to nLE	3	2.0 1.0	1.0 0.4	2.0 1.0	— —	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, HIGH or LOW nDx to nLE	3	2.0 2.0	−0.3 −0.7	2.0 2.0	— —	ns
$t_w(\text{H})$	nLE pulse width HIGH	1	2.9	1.9	2.9	—	ns

AC WAVEFORMS

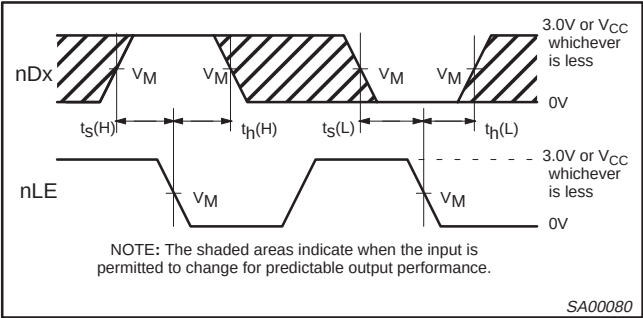
$V_M = 1.5\text{ V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{ V}$



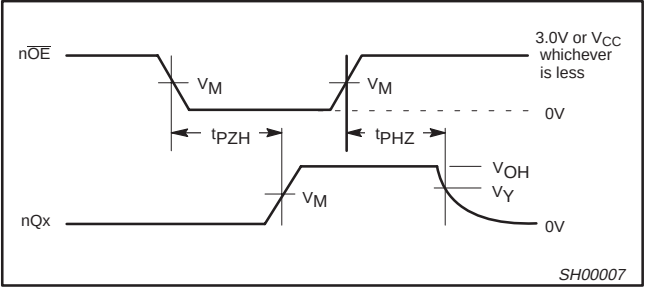
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



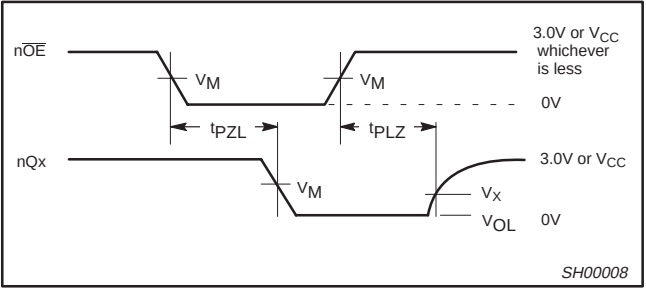
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Set-up and Hold Times



Waveform 4. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

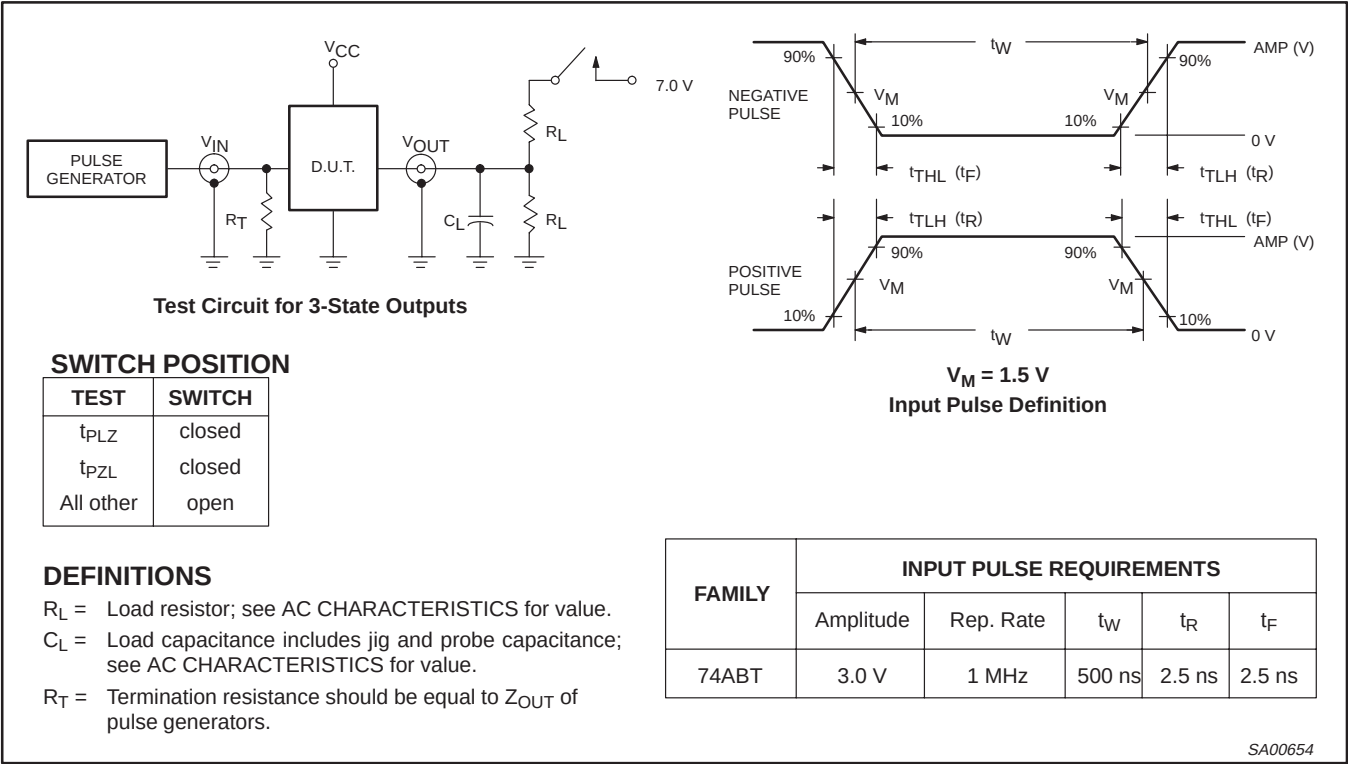


Waveform 5. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

20-bit bus interface latch (3-State)

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TEST CIRCUIT AND WAVEFORM

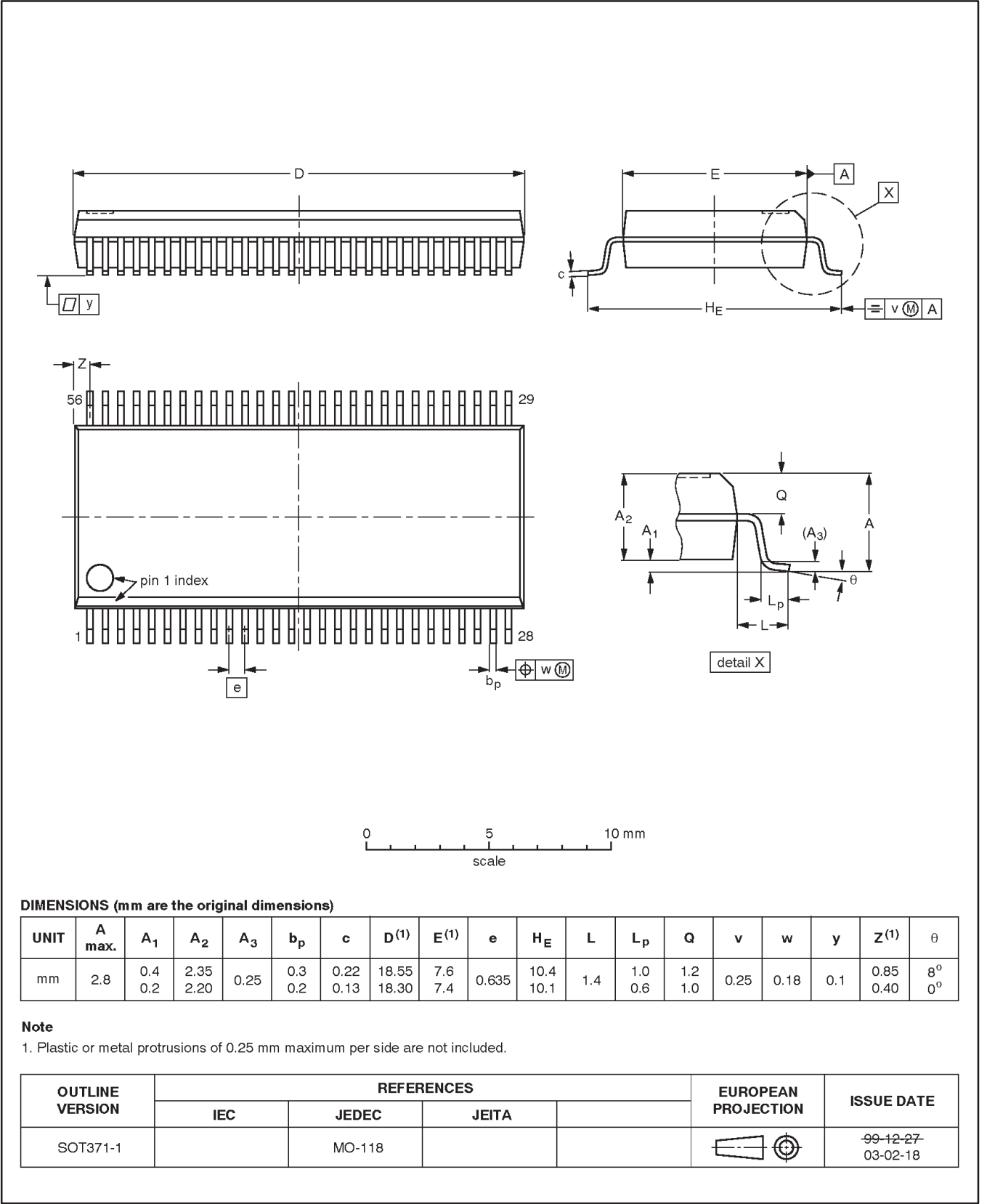


20-bit bus interface latch (3-State)

74ABT16841A

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

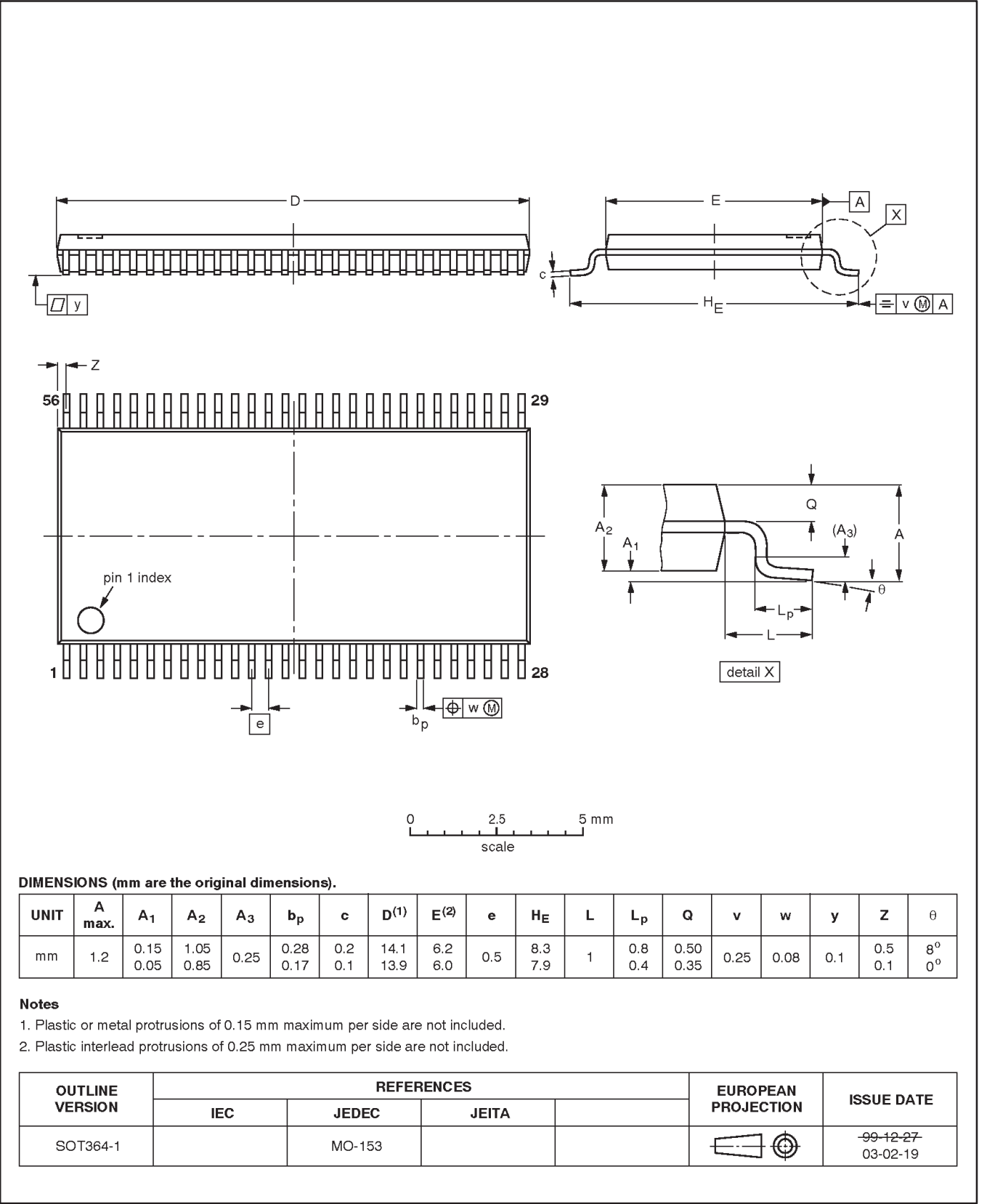


20-bit bus interface latch (3-State)

74ABT16841A

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



20-bit bus interface latch (3-State)

74ABT16841A

REVISION HISTORY

Rev	Date	Description
_3	20040202	Product data (9397 750 12821); 853-1797 ECN 01-A15433 of 27 January 2004. Replaces data sheet 74ABT_H16841A_2 of 2002 Dec 17 (9397 750 10845). Modifications: • Delete all references to 74ABTH16841A (product discontinued).
_2	20021217	Product data (9397 750 10845); ECN 853-1797 29296 of 12 December 2002. Supersedes data of 27 February 1998 (9397 750 03506).
_1	19980227	Product specification (9397 750 03506). ECN 853-1797 19025 of 27 February 1998.

20-bit bus interface latch (3-State)

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