

# High Speed, Low Voltage, 3 $\Omega$ , Differential 4:1 CMOS Analog Multiplexer/Switch

## DESCRIPTION

The DG2707 is a high speed, low voltage, 3  $\Omega$ , differential 4:1 multiplexer. It operates from a 1.65 V to 4.3 V single power supply. All channels guaranteed break before make switching. When powered with single 3.15 V supply, channel to channel ON Resistance matching is within 0.3  $\Omega$ .

All control logic input has 0.5 V to 1.65 V threshold. The EN pin enables cascading of the multiplexers. It features a 120 MHz - 3 dB bandwidth, - 90 dB crosstalk and - 70 dB off-isolation at 1 MHz.

The DG2707 comes in a small miniQFN-16 lead package (1.8 mm x 2.6 mm x 0.75 mm). As a committed partner to community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations and is 100 % RoHS compliant.

## FEATURES

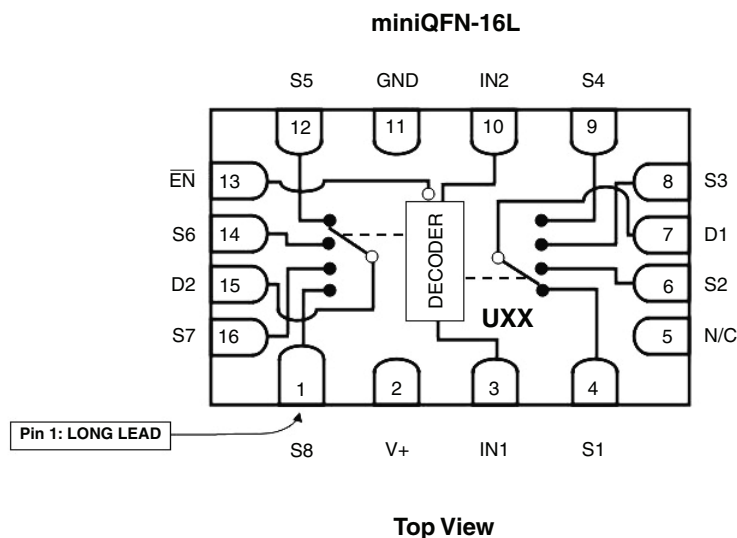
- Low voltage operation (1.65 V to 4.3 V)
- Low on-resistance -  $R_{ON}$ : 2.8  $\Omega$  typ. at 3.15 V
- Low voltage logic threshold
- Low crosstalk: - 70 dB
- High off-isolation: - 90 dB
- Ultra small package: miniQFN16 of 1.8 mm x 2.6 mm


**RoHS**  
COMPLIANT

## APPLICATIONS

- A/V and analog signal routing
- Battery operated devices
- Data acquisition systems
- Communications systems
- Medical and ATE equipments

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: **UXX**  
Traceability Code:  
U is DG2707DN  
XX = Date/Lot

## ORDERING INFORMATION

Temp. Range	Package	Part Number
- 40 $^{\circ}$ C to 85 $^{\circ}$ C	miniQFN-16	DG2707DN-T1-E4

**TRUTH TABLE DG2707 MULTIPLEXER, MINIQFN-16L**

Enable Input	Select Input		On Switches (Pin)	
EN (Pin 13)	IN2 (Pin 10)	IN1 (Pin 3)	Description (Pin)	Common (Pin)
0	0	0	S5 (Pin 12)	D2 (Pin 15)
0	0	1	S6 (Pin 14)	
0	1	0	S7 (Pin 16)	
0	1	1	S8 (Pin 1)	
0	0	0	S1 (Pin 4)	D1 (Pin 7)
0	0	1	S2 (Pin 6)	
0	1	0	S3 (Pin 8)	
0	1	1	S4 (Pin 9)	
1	X	X	All Switches are off	
Pin 5 N/C				

**ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

Parameter		Limit	Unit
Reference to GND	V+	- 0.3 to 5.0	V
	EN, IN, D <sub>X</sub> , S <sub>X</sub> <sup>a</sup>	- 0.3 to (V+ + 0.3)	
Current (Any terminal except S <sub>X</sub> or D <sub>X</sub> )		30	mA
Continuous Current (S <sub>X</sub> or D <sub>X</sub> )		± 300	
Peak Current (Pulsed at 1 ms, 10 % Duty Cycle)		± 500	
Storage Temperature (D Suffix)		- 65 to 150	°C
Thermal Resistance (Package) <sup>b</sup>	miniQFN-16	152	°C/W
Power Dissipation (Packages) <sup>b</sup>	miniQFN-16 <sup>c, d</sup>	525	mW

**Notes:**

- a. Signals on S<sub>X</sub> or D<sub>X</sub>, or IN<sub>X</sub> or EN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6.6 mW/°C above 70 °C
- d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.



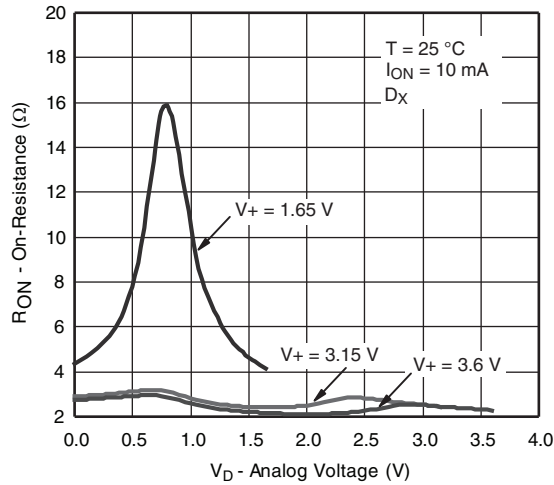
SPECIFICATIONS (V+ = 3.15 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified	Temp. <sup>b</sup>	Limits - 40 °C to 85 °C			Unit
				Min. <sup>d</sup>	Typ. <sup>c</sup>	Max. <sup>d</sup>	
Analog Switch							
Analog Signal Range <sup>e</sup>	V <sub>analog</sub>	R <sub>DS(on)</sub>	Full	0		V+	V
On Resistance	R <sub>DS(on)</sub>	V+ = 3.15 V, I <sub>SX</sub> = 10 mA, V <sub>D<sub>X</sub></sub> = 1.0 V	Room		2.8	5.5	Ω
			Full			6	
R <sub>ON</sub> Match	ΔR <sub>(on)</sub>	V+ = 3.15 V, I <sub>SX</sub> = 10 mA, V <sub>D<sub>X</sub></sub> = 1.0 V	Room		0.3		
R <sub>ON</sub> Resistance Flatness	R <sub>(on)</sub> Flatness	V+ = 3.15 V, I <sub>SX</sub> = 10 mA, V <sub>D<sub>X</sub></sub> = 0.0 V, 1.0 V	Room		0.6		
Channel-Off Leakage Current	I <sub>SX(off)</sub>	V+ = 3.6 V, V <sub>SX</sub> = 0.5 V/3 V, V <sub>D<sub>X</sub></sub> = 3 V/0.5 V	Room	- 5		5	nA
	I <sub>DX(off)</sub>		Full	- 10		10	
Channel-On Leakage Current	I <sub>DX(on)</sub>	V+ = 3.6 V, V <sub>SX</sub> , V <sub>D<sub>X</sub></sub> = 3 V/0.5 V	Room	- 10		10	
			Full	- 20		20	
Digital Control							
Input High Voltage	V <sub>INH</sub>		Full	1.65			V
Input Low Voltage	V <sub>INL</sub>					0.4	
Input Current	I <sub>INL</sub> or I <sub>INH</sub>	V <sub>IN</sub> = 0 or V+			- 1		1
Input Capacitance	C <sub>IN</sub>	V+ = 3.15, f = 1 MHz			5.1		pF
Dynamic Characteristics							
Break-Before-Make Time	t <sub>BBM</sub>	V <sub>SX</sub> = 1.5 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF	Room		1		ns
			Full	5			
Enable Turn-On Time	t <sub>ON(EN)</sub>		Room		20	45	
			Full			55	
Enable Turn-Off Time	t <sub>OFF(EN)</sub>		Room		15	35	
			Full			45	
Transition Time	t <sub>TRANS</sub>		Room		35	55	
			Full			65	
Charge Injection <sup>d</sup>	Q <sub>INJ</sub>	C <sub>L</sub> = 1 nF, R <sub>GEN</sub> = 0 Ω, V <sub>SX</sub> = 2 V	Room		- 14		pC
Off-Isolation <sup>d</sup>	OIRR	V+ = 3.15 V, f = 1 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF	Room		- 70		dB
Crosstalk <sup>d, f</sup>	X <sub>TALK</sub>				- 90		
Bandwidth <sup>d</sup>	BW	V+ = 3.15 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, - 3 dB	Room		120		MHz
Total Harmonic Distortion <sup>d</sup>	THD	V+ = 3.15 V, R <sub>load</sub> = 600 Ω	Room		0.02		%
S <sub>X</sub> , D <sub>X</sub> Off Capacitance <sup>d</sup>	C <sub>S(off)</sub>	V+ = 3.15 V, f = 1 MHz	Room		16		pF
	CD <sub>X(off)</sub>				42		
Channel-On Capacitance <sup>d</sup>	CD <sub>X(on)</sub>					49	
Power Supply							
Power Supply Range	V+			1.65		4.3	V
Power Supply Current	I+	V <sub>IN</sub> = 0 V or V+	Full			1	μA

## Notes:

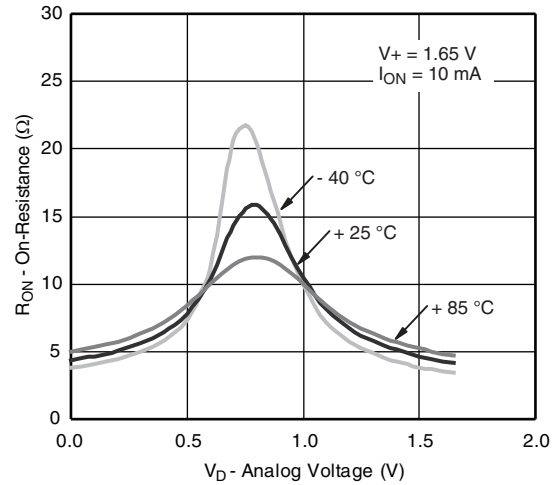
- a. Room = 25 °C, Full = as determined by the operating suffix.  
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.  
c. Typical values are for design aid only, not guaranteed nor subject to production testing.  
d. Guarantee by design, not subjected to production test.  
e. V<sub>IN</sub> = input voltage to perform proper function.  
f. Crosstalk measured between channels.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

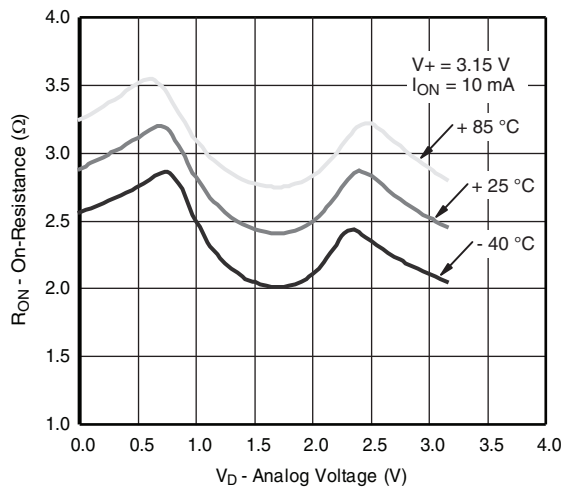
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



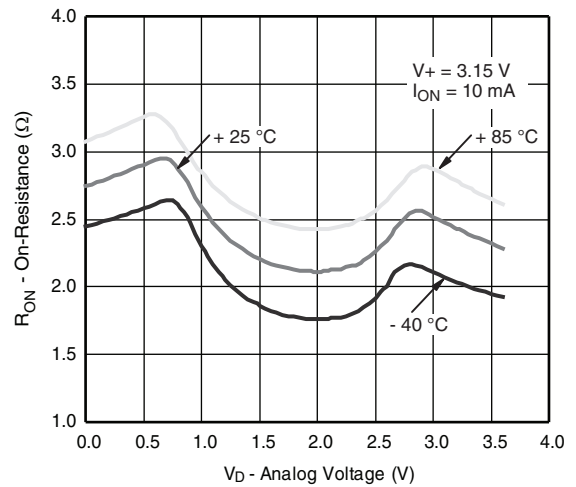
**$R_{ON}$  vs.  $V_D$  and Single Supply Voltage**



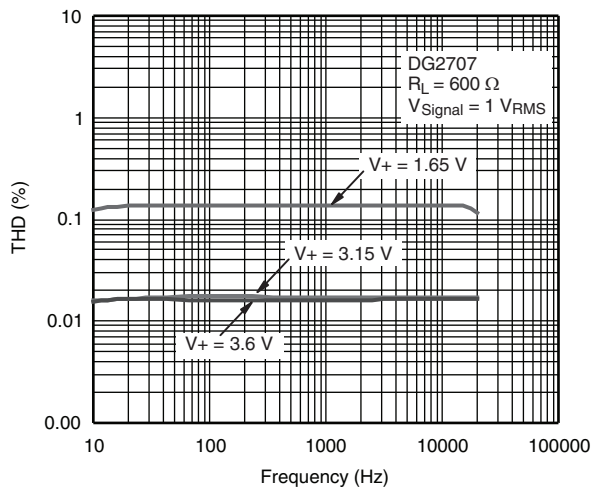
**$R_{ON}$  vs. Analog Voltage and Temperature**



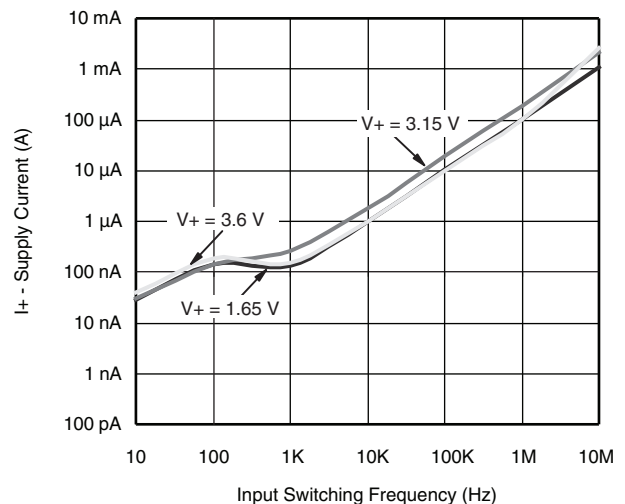
**$R_{ON}$  vs. Analog Voltage and Temperature**



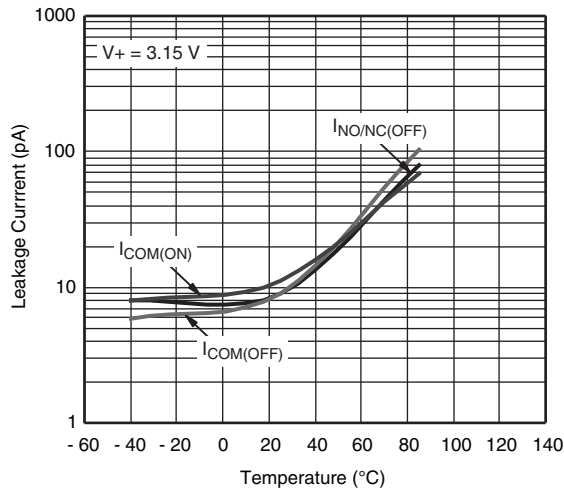
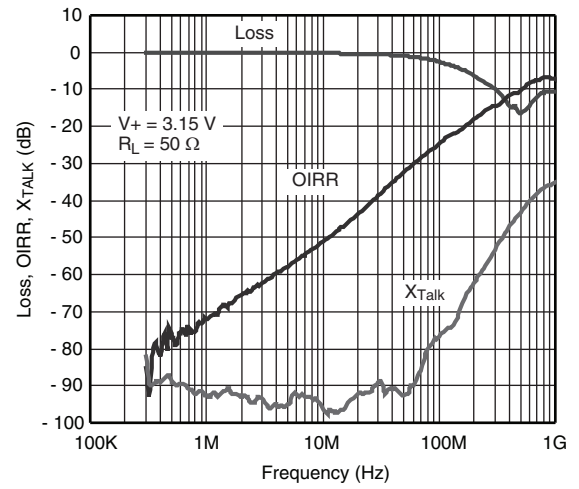
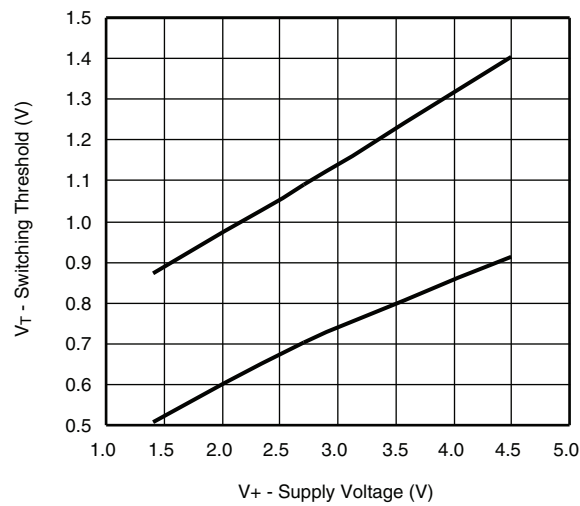
**$R_{ON}$  vs. Analog Voltage and Temperature**



**Switching Threshold vs. Supply Voltage**



**Supply Current vs. Input Switching Frequency**

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Leakage Current vs. Temperature**

**Insertion Loss, Off-Isolation Crosstalk vs. Frequency**

**Switching Threshold vs. Supply Voltage**

## TEST CIRCUITS

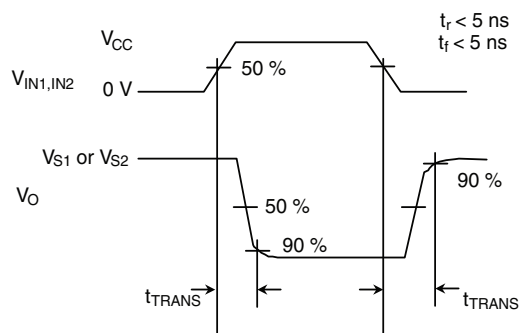
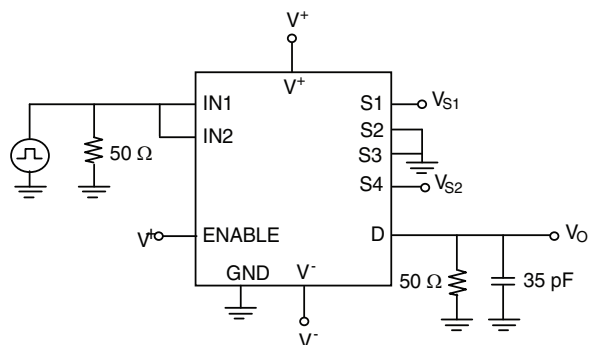


Figure 1. Transition Time

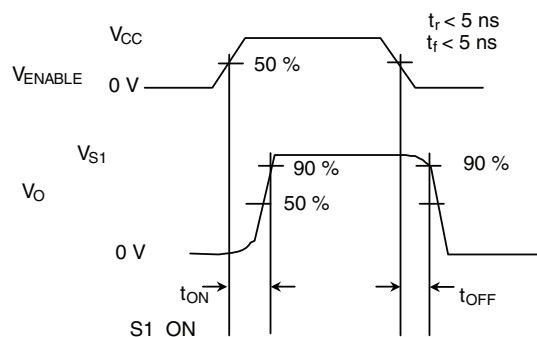
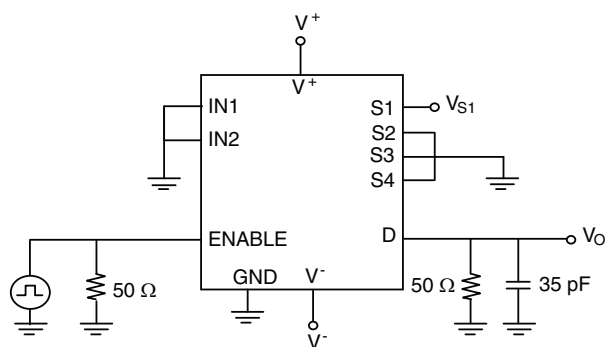


Figure 2. Enable Switching Time

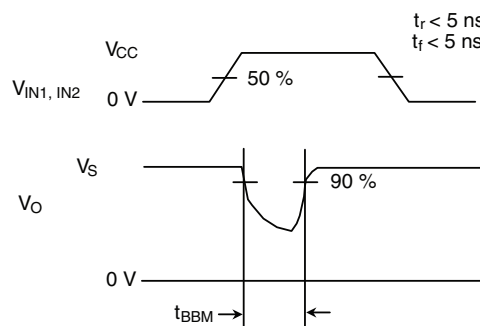
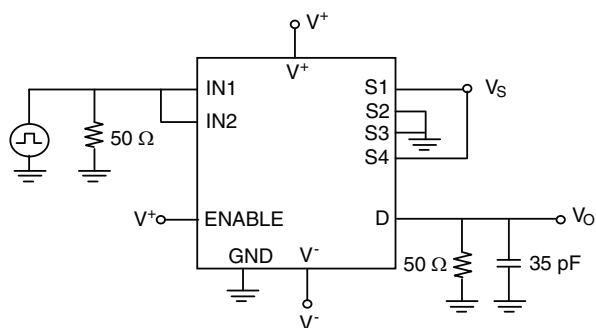
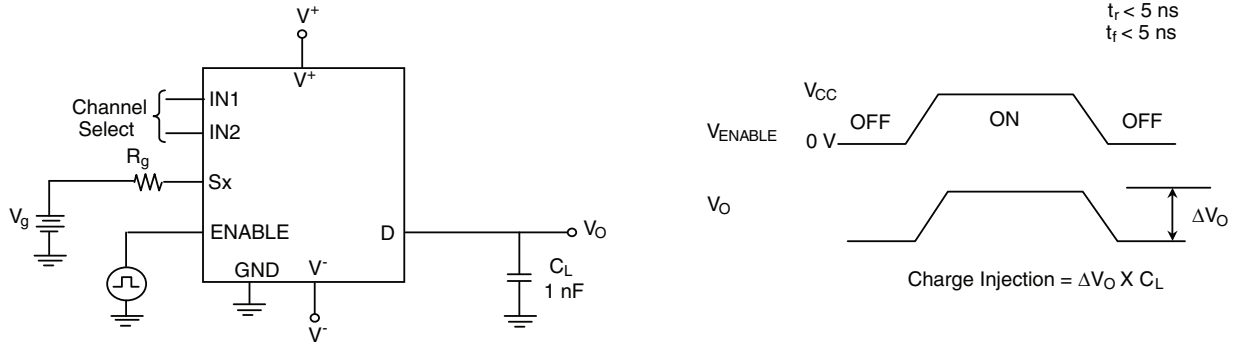
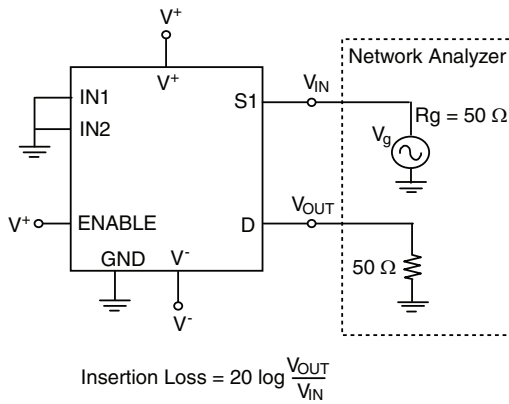
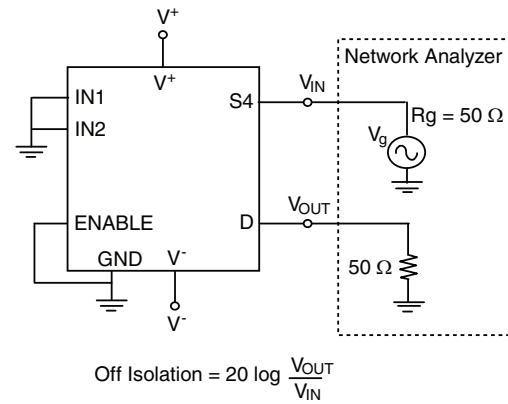
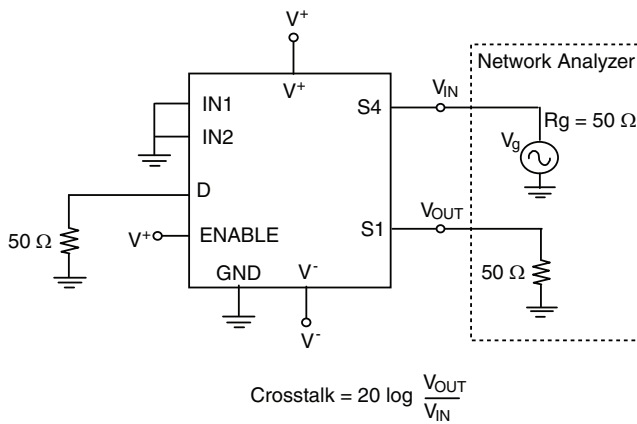
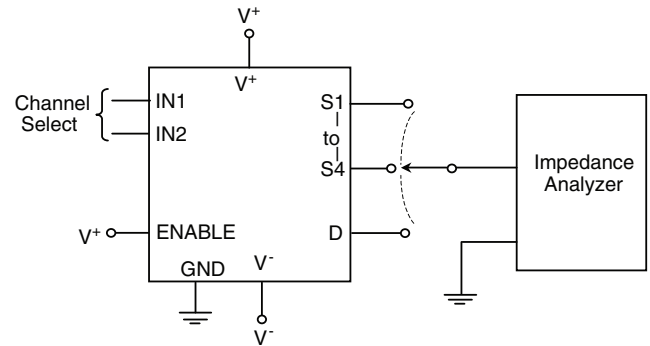
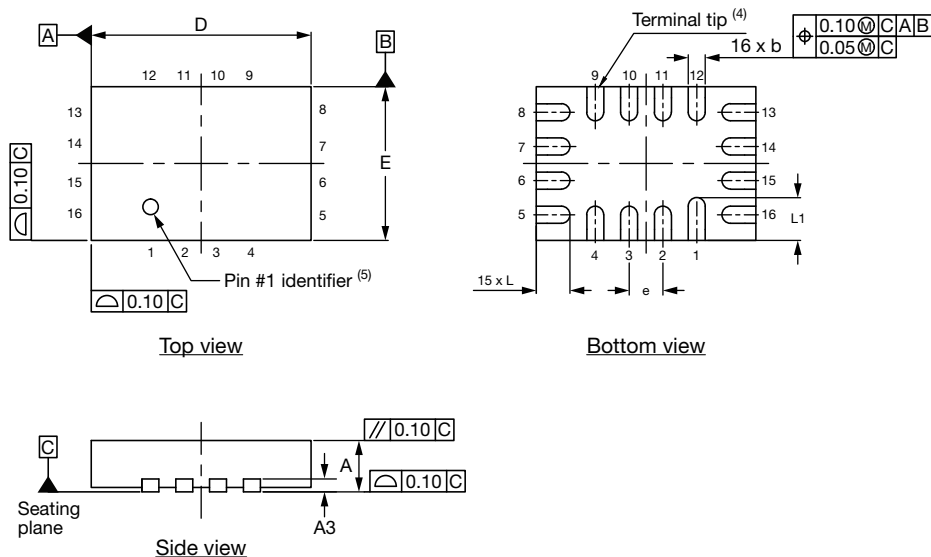


Figure 3. Break-Before Make

**TEST CIRCUITS**

**Figure 4. Charge Injection**

**Figure 5. Insertion Loss**

**Figure 6. Off-Isolation**

**Figure 7. Crosstalk**

**Figure 8. Source, Drain Capacitance**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?68397](http://www.vishay.com/ppg?68397).

## Thin miniQFN16 Case Outline



DIMENSIONS	MILLIMETERS <sup>(1)</sup>			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N <sup>(3)</sup>	16			16		
Nd <sup>(3)</sup>	4			4		
Ne <sup>(3)</sup>	4			4		

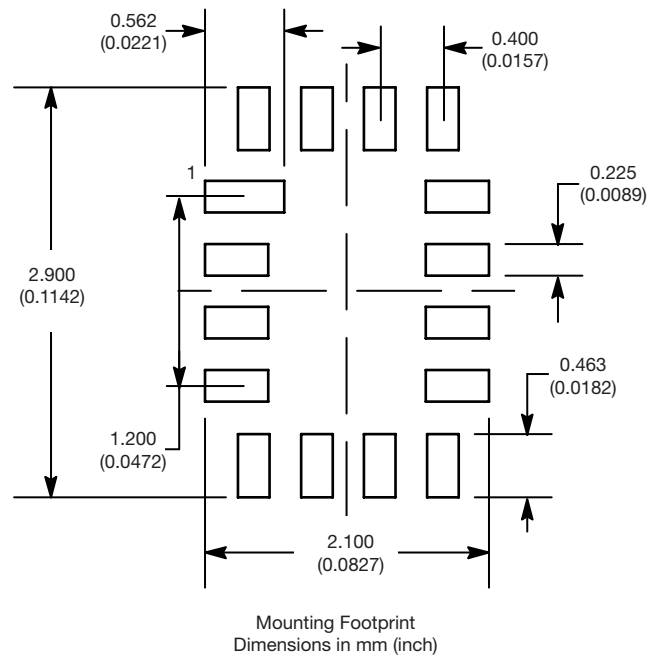
### Notes

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16  
DWG: 6023



## RECOMMENDED MINIMUM PADS FOR MINI QFN 16L





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