

Quad SPST CMOS Analog Switches

December 1993

Features

- $\pm 15\text{V}$ Input Signal Range
- Low $R_{DS(ON)}$ ($\leq 175\Omega$)
- TTL, CMOS Compatible
- Latch Proof
- True Second Source
- 44V Maximum Supply Ratings
- Logic Inputs Accept Negative Voltages

Description

The DG201A (normally open) and DG202 (normally closed) quad SPST analog switches are designed using Harris' 44V CMOS process. These bidirectional switches are latch-proof and feature break-before-make switching. Designed to block signals up to 30V peak-to-peak in the OFF state, the DG201A and DG202 offer the advantages of low on resistance ($\leq 175\Omega$), wide input signal range ($\pm 15\text{V}$) and provide both TTL and CMOS compatibility.

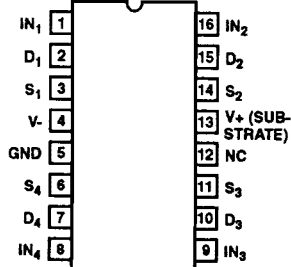
The DG201A and DG202 are specification and pinout compatible with the industry standard devices.

Ordering Information

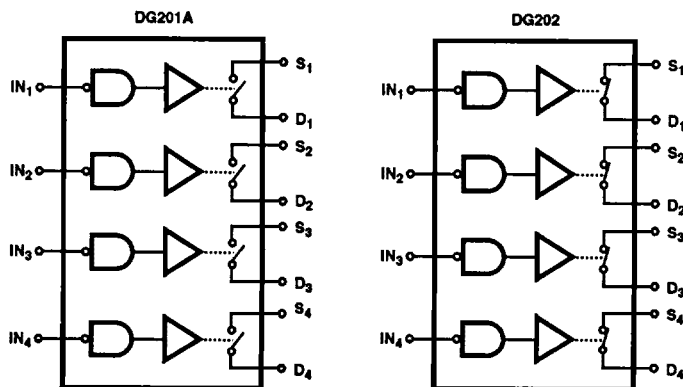
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG201AAK	-55°C to +125°C	16 Lead Ceramic DIP
DG201ABK	-25°C to +85°C	16 Lead Ceramic DIP
DG201AAK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG201ABY	-25°C to +85°C	16 Lead SOIC (W)
DG201ACK	0°C to +70°C	16 Lead Ceramic DIP
DG201ACJ	0°C to +70°C	16 Lead Plastic DIP
DG201ACY	0°C to +70°C	16 Lead SOIC (W)
DG202AK	-55°C to +125°C	16 Lead Ceramic DIP
DG202AK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG202BK	-25°C to +85°C	16 Lead Ceramic DIP
DG202CK	0°C to +70°C	16 Lead Ceramic DIP
DG202CJ	0°C to +70°C	16 Lead Plastic DIP

Pinout

DG201A, DG202
(CDIP, PDIP, SOIC)
TOP VIEW



Functional Diagrams



NOTES:

1. Four SPST switches per package.
2. Switches shown for logic "1" input

TRUTH TABLE

LOGIC	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" $\leq 0.8\text{V}$, Logic "1" $\geq 2.4\text{V}$

Specifications DG201A, DG202

Absolute Maximum Ratings

V ₊ to V ₋	44V
V ₋ to Ground	-25V
V _{IN} to Ground (Note 1)	(V ₋ -2V), (V ₊ +2V)
V _S or V _D to V ₊ (Note 1)	+2, (V ₋ -2V)
V _S or V _D to V ₋ (Note 1)	-2, (V ₊ +2V)
Current, any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max)	70mA
Lead Temperature (Soldering 10s)	+300°C
Storage Temperature Range	
C Suffix	-65°C to +125°C
A & B Suffix	-65°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
Plastic DIP Package	100°C/W	-
SOIC Package	100°C/W	-
Junction Temperature		
Ceramic DIP Package	+175°C	
Plastic DIP Package	+150°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V₊ = 15V, V₋ = -15V, GND = 0V, T_A = Over Operating Temperature Range

PARAMETERS	TEST CONDITIONS	DG201AA/DG202A			DG201AB, C/DG202B, C			UNITS	
		MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX		
DYNAMIC CHARACTERISTICS									
Turn-On Time, t_{ON}	See Figure 1	-	480	600	-	480	600	ns	
Turn-Off Time, t_{OFF}	See Figure 1	-	370	450	-	370	450	ns	
Charge Injection, Q	$C_L = 1000\text{pF}$, $R_S = 0$, $V_S = 0\text{V}$	-	20	-	-	20	-	pC	
Source OFF Capacitance, $C_{S(OFF)}$	$f = 140\text{kHz}$, $V_{IN} = 5\text{V}$, $V_S = 0\text{V}$	-	5.0	-	-	5.0	-	pF	
Drain OFF Capacitance, $C_{D(OFF)}$	$f = 140\text{kHz}$, $V_{IN} = 5\text{V}$, $V_D = 0\text{V}$	-	5.0	-	-	5.0	-	pF	
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$	$f = 140\text{kHz}$, $V_{IN} = 5\text{V}$, $V_S = V_D = 0\text{V}$	-	16	-	-	16	-	pF	
OFF Isolation, OIRR	$V_{IN} = 5\text{V}$, $Z_L = 75\Omega$, $V_S = 2.0\text{V}$, $f = 100\text{kHz}$	-	70	-	-	70	-	dB	
Crosstalk (Channel to Channel), CCRR		-	90	-	-	90	-	dB	
INPUT									
Input Current with Voltage High, I_{INH}	$V_{IN} = 2.4\text{V}$	-1.0	-0.0004	-	-1.0	-0.0004	-	μA	
	$V_{IN} = 15\text{V}$	-	0.003	1.0	-	0.003	1.0	μA	
Input Current with Voltage Low, I_{INL}	$V_{IN} = 0\text{V}$	-1.0	-0.0004	-	-1.0	-0.0004	-	μA	
SWITCH									
Analog Signal Range, V_{ANALOG}		-15	-	15	-15	-	15	V	
Drain Source On Resistance, $R_{DS(ON)}$	$V_D = \pm 10\text{V}$, $V_{IN} = 0.8\text{V}$ (DG201A) $I_S = 1\text{mA}$, $V_{IN} = 2.4\text{V}$ (DG202)	-	115	175	-	115	200	Ω	
Source OFF Leakage Current, $I_{S(OFF)}$	$V_{IN} = 2.4\text{V}$ (DG201A) $V_{IN} = 0.8\text{V}$ (DG202)	$V_S = 14\text{V}$, $V_D = -14\text{V}$	-	0.01	1.0	-	0.01	5.0	nA
		$V_S = -14\text{V}$, $V_D = 14\text{V}$	-1.0	-0.02	-	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	$V_{IN} = 2.4\text{V}$ (DG201A) $V_{IN} = 0.8\text{V}$ (DG202)	$V_S = -14\text{V}$, $V_D = 14\text{V}$	-	0.01	1.0	-	0.01	5.0	nA
		$V_S = 14\text{V}$, $V_D = -14\text{V}$	-1.0	-0.02	-	-5.0	-0.02	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 4)	$V_{IN} = 0.8\text{V}$ (DG201A) $V_{IN} = 2.4\text{V}$ (DG202)	$V_D = V_S = 14\text{V}$	-	0.1	1.0	-	0.1	5.0	μA
		$V_D = V_S = -14\text{V}$	-1.0	-0.15	-	-5.0	-0.15	-	μA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I_+	All Channels ON or OFF	-	0.9	2	-	0.9	2	mA	
Negative Supply Current, I_-		-1	-0.3	-	-1	-0.3	-	mA	

Specifications DG201A, DG202

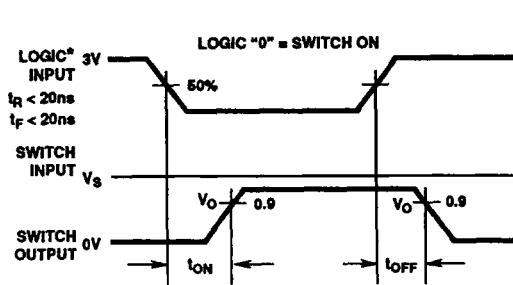
Electrical Specifications $V_+ = 15V$, $V_- = -15V$, $GND = 0V$, $T_A =$ Over Operating Temperature Range (Continued)

PARAMETERS		TEST CONDITIONS	DG201AA/DG202A			DG201AB, C/DG202B, C			UNITS
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
INPUT									
Input Current with Voltage High, I _{INH}	V _{IN} = 2.4V	-10	-	-	-10	-	-	μA	
	V _{IN} = 15V	-	-	10	-	-	10	μA	
Input Current with Voltage Low, I _{INL}	V _{IN} = 0V	-10	-	-	-10	-	-	μA	
SWITCH									
Analog Signal Range, V _{ANALOG}			-15	-	15	-15	-	15	V
Drain Source On Resistance, R _{DS(ON)}	V _D = ±10V, V _{IN} = 0.8V (DG201A) I _S = 1mA, V _{IN} = 2.4V (DG202)		-	-	250	-	-	250	Ω
Source OFF Leakage Current, I _{S(OFF)}	V _{IN} = 2.4V (DG201A) V _{IN} = 0.8V (DG202)	V _S = 14V, V _D = -14V	-	-	100	-	-	100	nA
		V _S = -14V, V _D = 14V	-100	-	-	-100	-	-	nA
Drain OFF Leakage Current, I _{D(OFF)}		V _S = -14V, V _D = 14V	-	-	100	-	-	100	nA
		V _S = 14V, V _D = -14V	-100	-	-	-100	-	-	nA
Drain ON Leakage Current, I _{D(ON)} (Note 4)	V _{IN} = 0.8V (DG201A) V _{IN} = 2.4V (DG202)	V _D = V _S = 14V	-	-	200	-	-	200	μA
		V _D = V _S = -14V	-200	-	-	-200	-	-	μA

NOTES:

1. Signals on V_S , V_D , or V_{IN} exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. $I_{D(ON)}$ is leakage from driver into ON switch.

Test Circuits



*Logic shown for DG201A, invert for DG202

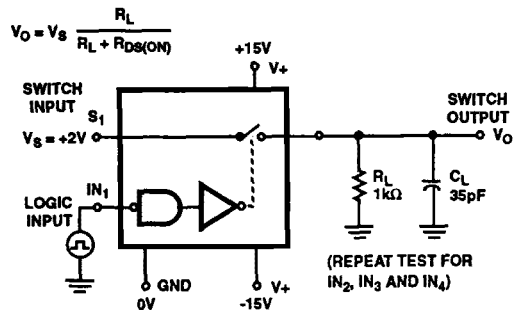
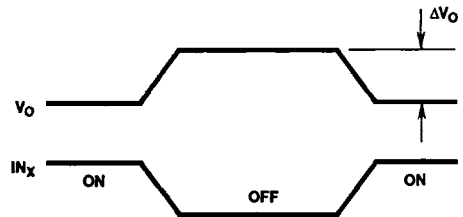
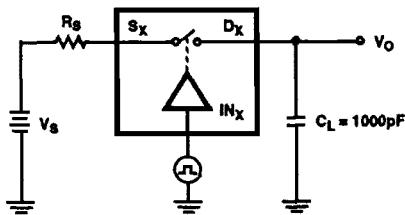


FIGURE 1. T_{ON} AND T_{OFF} SWITCHING TEST



NOTES:

1. ΔV_O = Measured voltage error due to charge injection.
2. The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.

FIGURE 2. CHARGE INJECTION TEST CIRCUIT

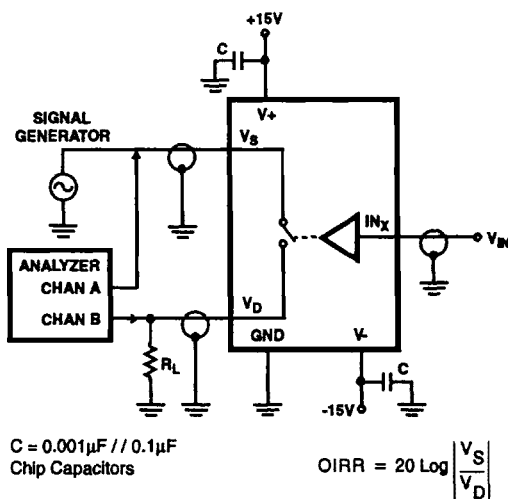


FIGURE 3. OFF ISOLATION TEST CIRCUIT

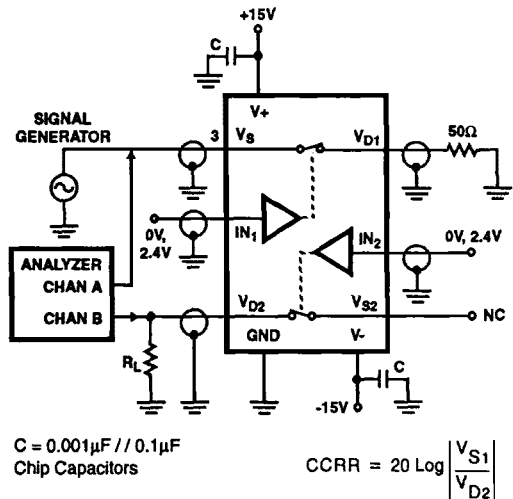


FIGURE 4. CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT