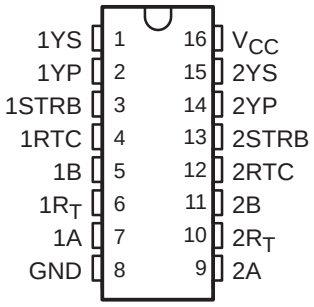
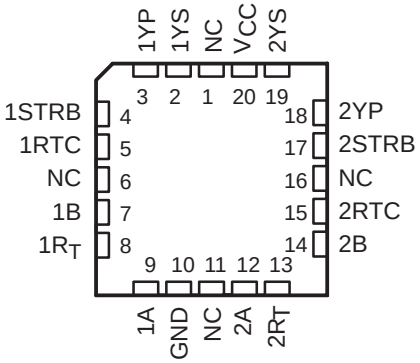
SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

- **Choice of Open-Collector or Active Pullup (Totem-Pole) Outputs**
- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual-Channel Operation**
- **TTL Compatible**
- **±15-V Common-Mode Input Voltage Range**
- **Optional-Use Built-In 130-Ω Line-Terminating Resistor**
- **Individual Frequency-Response Controls**
- **Individual Channel Strobes**
- **Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers**
- **Designed to Be Interchangeable With National DS9615 Line Receivers**

SN55115 . . . J OR W PACKAGE
SN75115 . . . N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay.

The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pullup terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

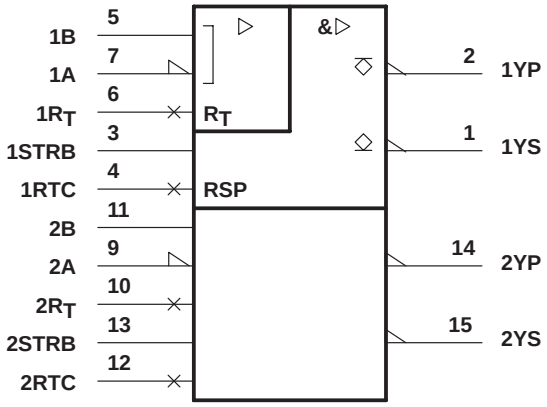
The SN55115 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75115 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

STRB	DIFF INPUT (A AND B)	OUTPUT (YP AND YS TIED TOGETHER)
L	X	H
H	L	H
H	H	L

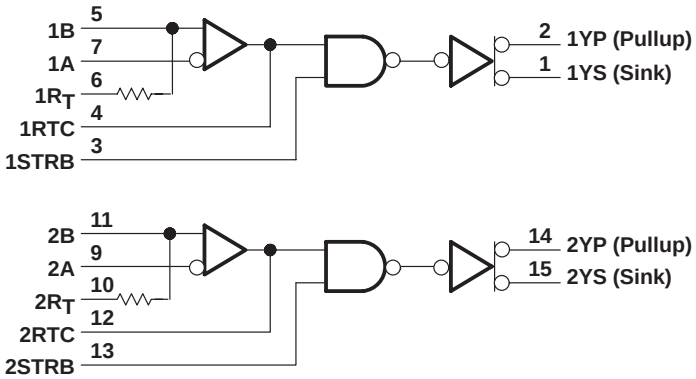
$H = V_I \geq V_{IH}$ min or V_{ID} more positive than V_{T+} max
$L = V_I \leq V_{IL}$ max or V_{ID} more negative than V_{T-} max
X = irrelevant

logic symbol†

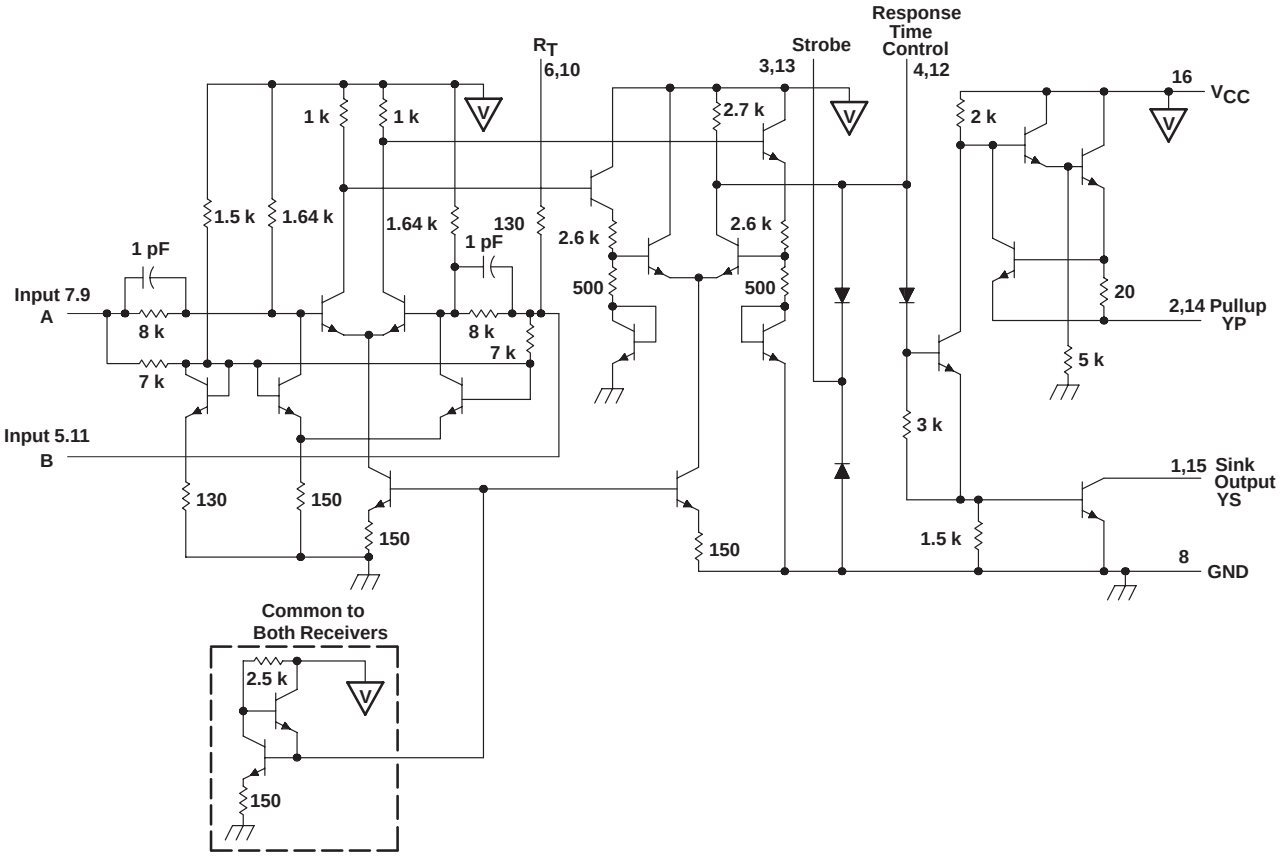


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values are nominal and in ohms.
Pin numbers shown are for the J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage V_I (A, B, and R_T)	±25 V
Input voltage V_I (STRB)	5.5 V
Off-state voltage applied to open-collector outputs	14 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W†	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK, J, and W packages, SN55115 chips are either silver glass or alloy mounted. SN75115 chips are glass mounted.

recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage at STRB, V_{IH}	2.4			2.4			V
Low-level input voltage at STRB, V_{IL}			0.4			0.4	V
High-level output current, I_{OH}			–5			–5	mA
Low-level output current, I_{OL}			15			15	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55115			SN75115			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IT+}§	Positive-going threshold voltage	V_O = 0 .4 V, I_{OL} = 15 mA, V_{IC} = 0				500			500	mV
V_{IT-}§	Negative-going threshold voltage	V_O = 2 .4 V, I_{OH} = −5 mA, V_{IC} = 0		−500¶			−500¶			mV
V_{ICR}	Common-mode input voltage range	V_{ID} = ±1 V		+15 to −15	+24 to −19		+15 to −15	+24 to −19		V
V_{OH}	High-level ouput voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OH} = −5 mA	T_A = MIN	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = MAX	2.4			2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V, Other input at 5.5 V	T_A = MIN			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = MAX			−0.7			−0.7	
I_{SH}	High-level strobe current	V_{CC} = MIN, V_{ID} = −0.5 V, V_{strobe} = 4.5 V	T_A = 25°C			2			5	µA
			T_A = MAX			5			10	
I_{SL}	Low-level strobe current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{strobe} = 0.4 V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
$I_{(RTC)}$	Response-time-control current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MIN, V_{OH} = 12 V, V_{ID} = −4.5 V	T_A = 25°C			100				µA
			T_A = MAX			200				
		V_{CC} = MIN, V_{OH} = 5.25 V, V_{ID} = −4.75 V	T_A = 25°C						100	
			T_A = MAX						200	
R_T	Line-terminating resistance	V_{CC} = 5 V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Supply-circuit output current#	V_{CC} = MAX, V_{ID} = −0.5 V, V_O = 0	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply current (both receivers)	V_{CC} = MAX, V_{ID} = 0.5 V, V_{IC} = 0	T_A = 25°C		32	50		32	50	mA

† Unless otherwise noted, V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§ Differential voltages are at the B input terminal with respect to the A input terminal.

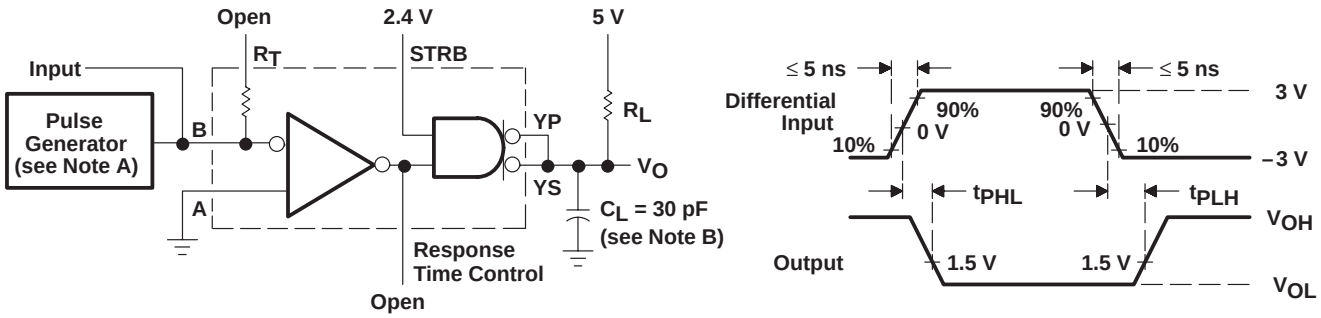
¶ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55115			SN75115			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 3.9 kΩ, See Figure 1		18	50		18	75	ns
t_{PHL}	Propagation delay time, high-to-low level output	R_L = 390 Ω, See Figure 1		20	50		20	75	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORM

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W ≤ 100 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

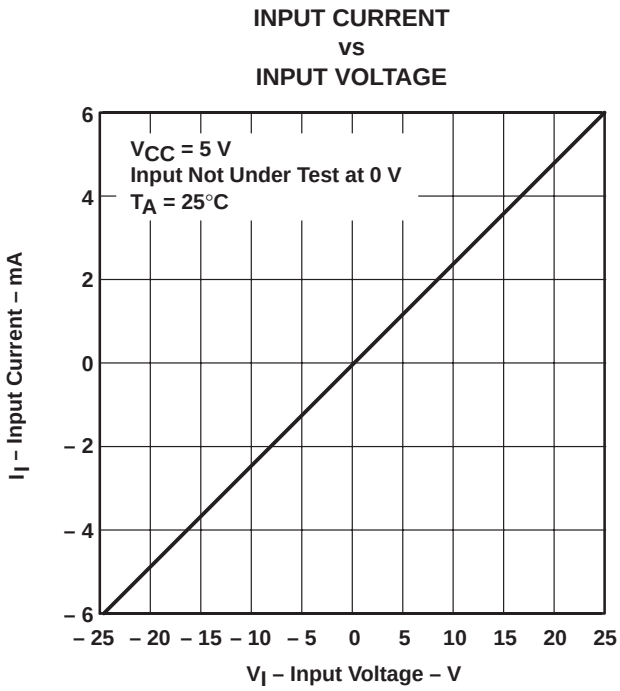


Figure 2

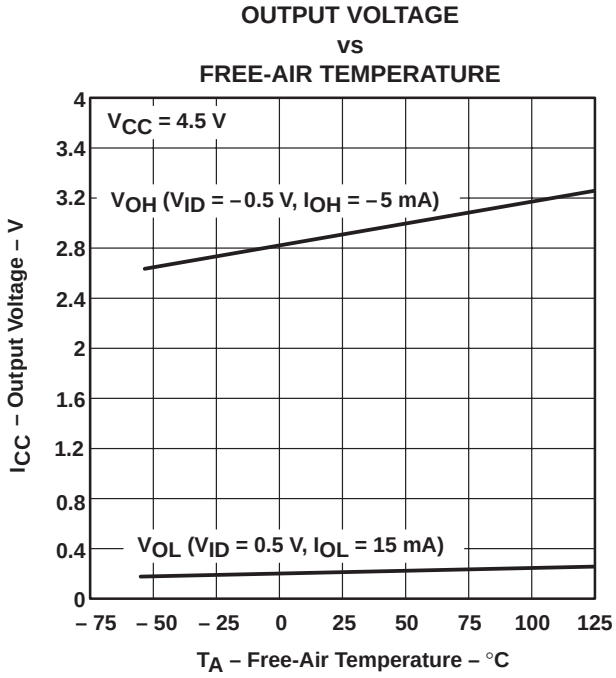


Figure 3

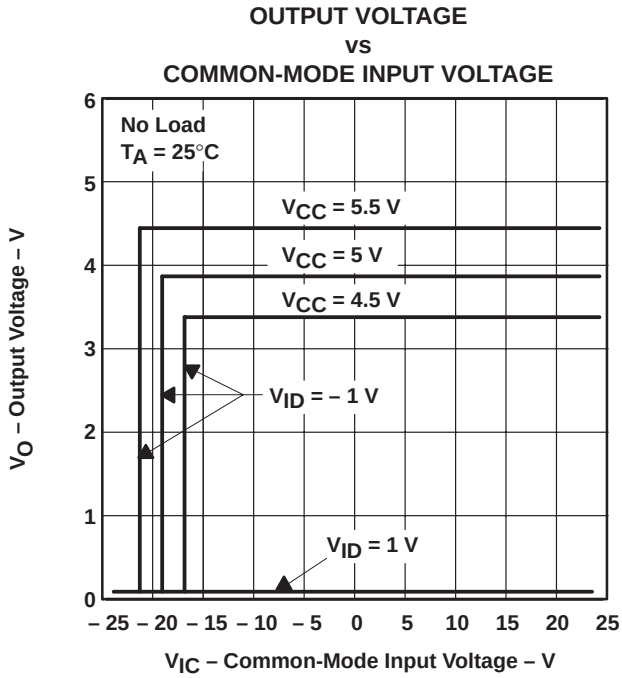


Figure 4

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

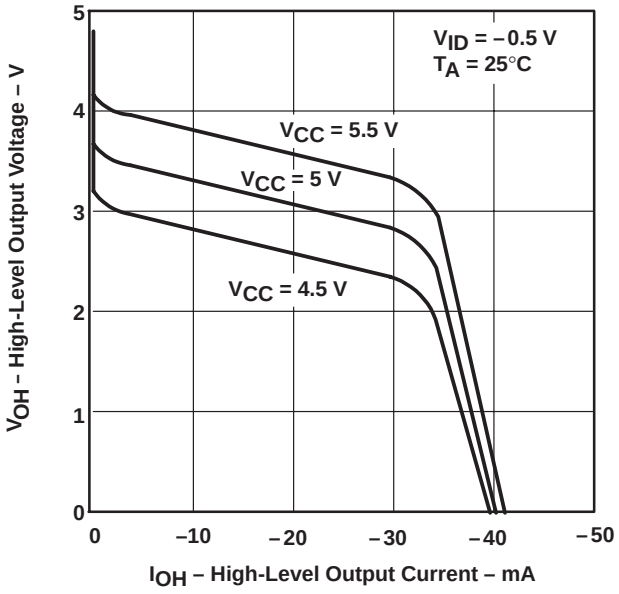


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

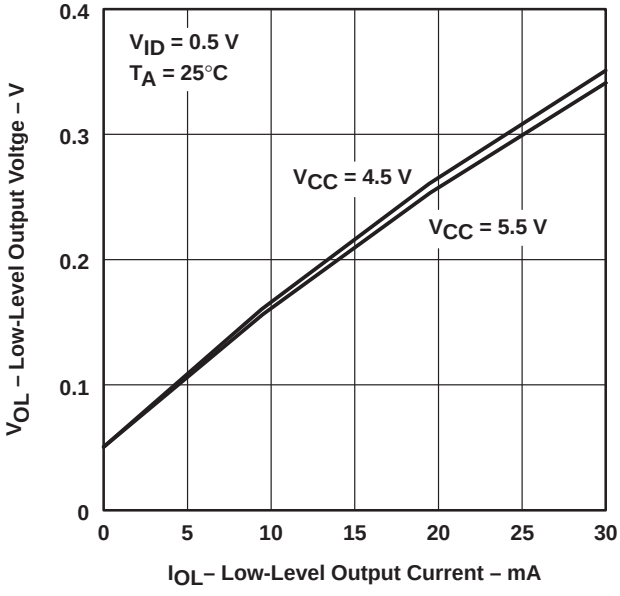


Figure 6

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

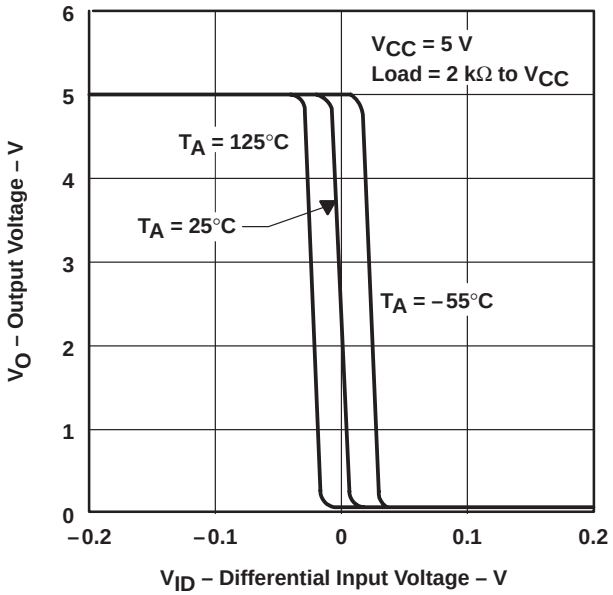


Figure 7

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

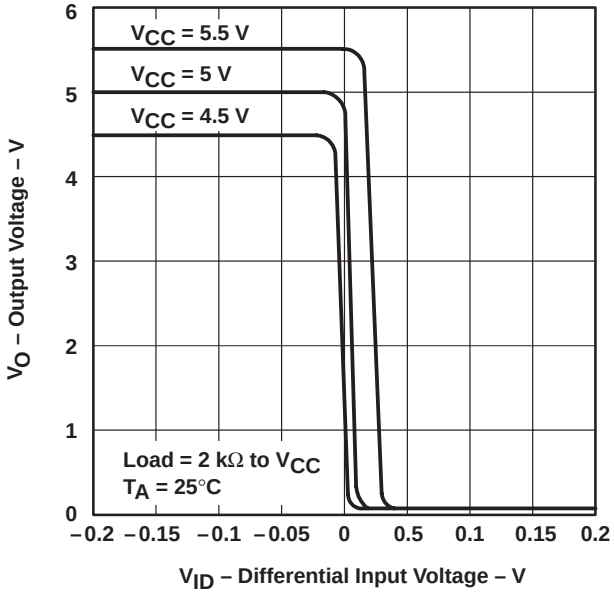


Figure 8

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs STROBE INPUT VOLTAGE

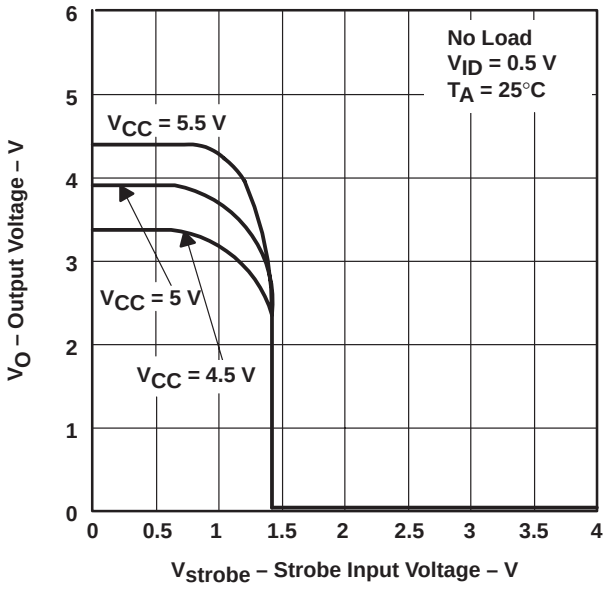


Figure 9

OUTPUT VOLTAGE vs STROBE INPUT VOLTAGE

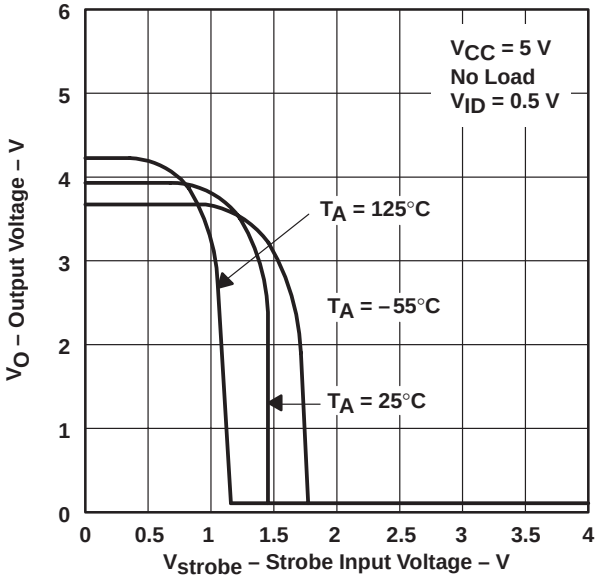


Figure 10

SUPPLY CURRENT (BOTH RECEIVERS) vs SUPPLY VOLTAGE

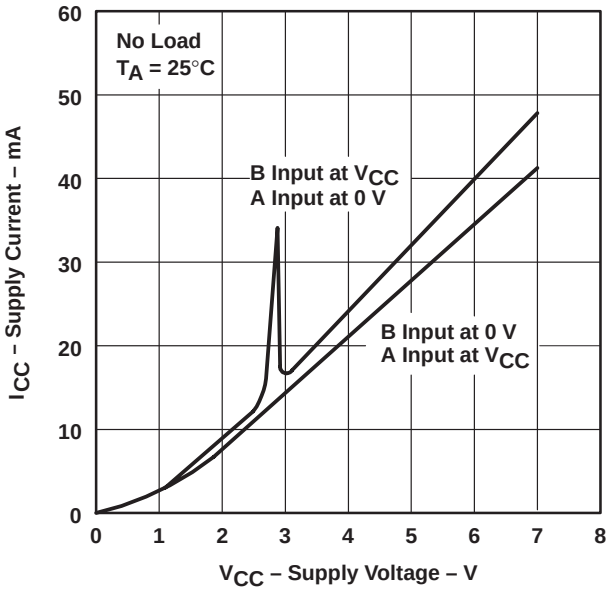


Figure 11

SUPPLY CURRENT (BOTH RECEIVERS) vs FREE-AIR TEMPERATURE

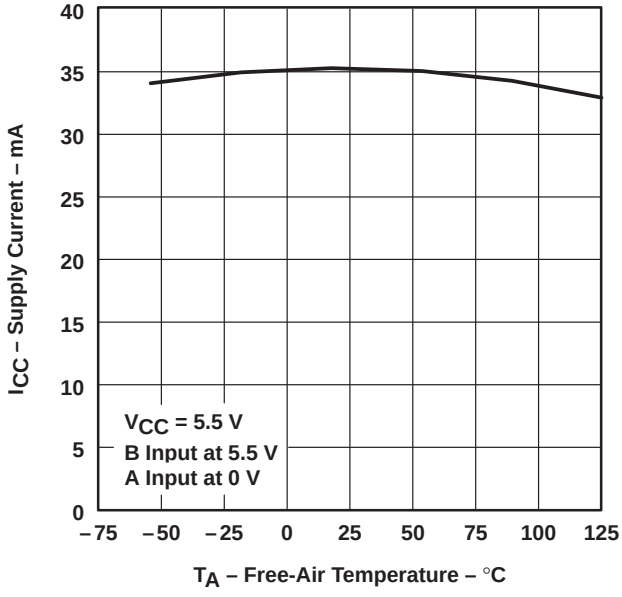


Figure 12

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

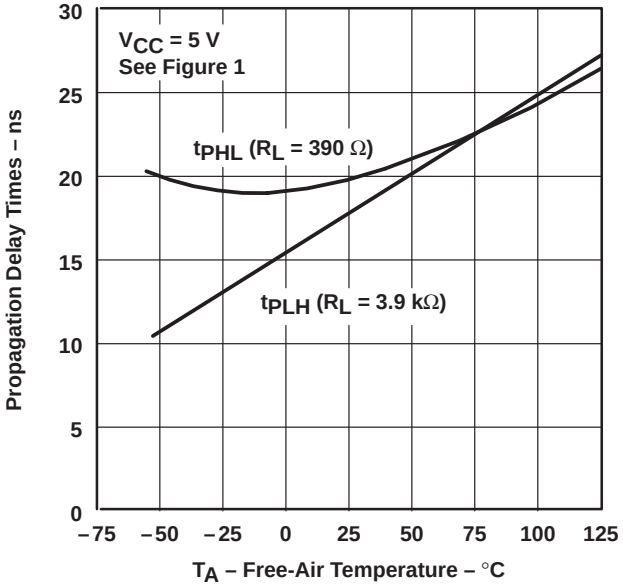


Figure 13

MAXIMUM OPERATING FREQUENCY vs RESPONSE-TIME-CONTROL CAPACITANCE

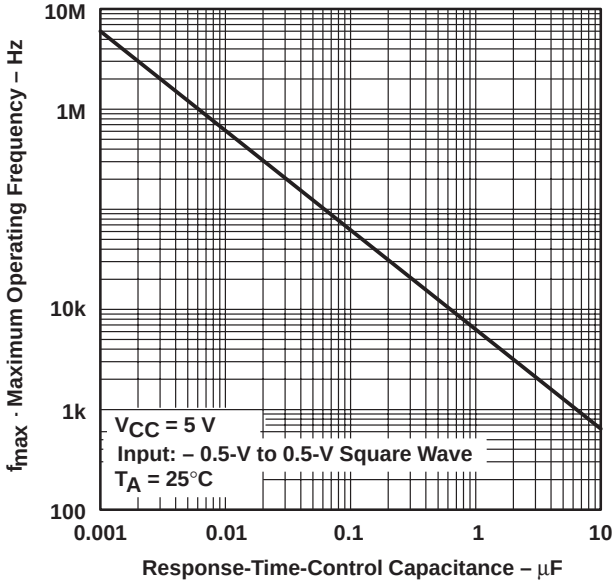
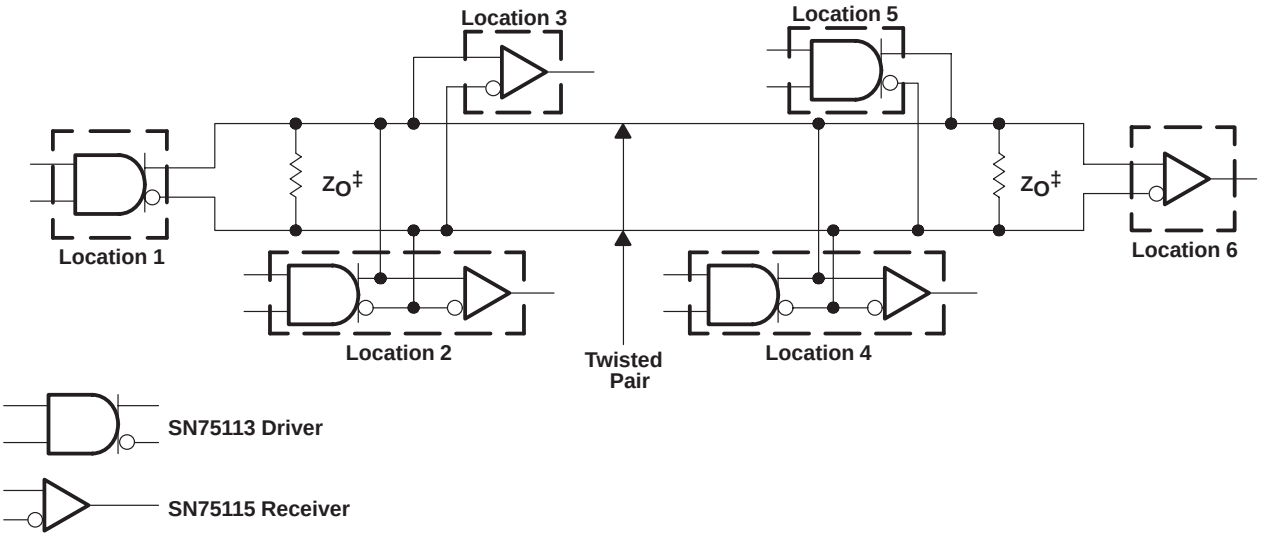


Figure 14

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



‡ $Z_O = R_T$. A capacitor may be connected in series with Z_O to reduce power dissipation.

Figure 15. Basic Party-Line or Data-Bus Differential Data Transmission

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

SN75115, DUAL DIFFERENTIAL LINE RECEIVER

Device Status: Active

Parameter Name	SN75115
Receivers Per Package	2
Receiver tpd (ns)	75
Receiver (Vth) (mV)	1000
Supply Voltage(s) (V)	5
ICC (max) (mA)	50
Footprint	SN75115

Description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay.

The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pullup terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

The SN55115 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN75115 is characterized for operation from 0°C to 70°C.

H = V_I >= V_{IH} min or V_{ID} more positive than V_{T+} max L = V_I <= V_{IL} max or V_{ID} more negative thanV_{T-} max
X = irrelevant

Features

- Choice of Open-Collector or Active Pullup (Totem-Pole) Outputs
- Single 5-V Supply
- Differential Line Operation
- Dual-Channel Operation
- TTL Compatible
- ±15-V Common-Mode Input Voltage Range
- Optional-Use Built-In 130-Ω Line-Terminating Resistor
- Individual Frequency-Response Controls
- Individual Channel Strobes
- Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers
- Designed to Be Interchangeable With National DS9615 Line Receivers

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: slls072d.pdf (183 KB)
Full datasheet in Zipped PostScript: slls072d.psz (157 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
SN75115D	D	16	0 TO 70	ACTIVE	2.00	40	Check stock or order
SN75115DR	D	16	0 TO 70	ACTIVE	1.70	2500	Check stock or order
SN75115N	N	16	0 TO 70	ACTIVE	2.00	25	Check stock or order
SN75115NS	NS	16	0 TO 70	ACTIVE			Check stock or order

Application Reports

- 422 AND 485 OVERVIEW AND SYSTEM CONFIGURATIONS (SLLA070 - Updated: 02/15/2000)
- ANALOG APPLICATIONS JOURNAL, FEBRUARY 2000 (SLYT012A - Updated: 03/23/2000)
- ANALOG APPLICATIONS JOURNAL, NOVEMBER 1999 (SLYT010A - Updated: 03/23/2000)
- COMPARING BUS SOLUTIONS (SLLA067 - Updated: 03/06/2000)
- ELECTROSTATIC DISCHARGE APPLICATION NOTE (SSYA008 - Updated: 05/05/1999)
- JITTER ANALYSIS (SLLA075 - Updated: 03/31/2000)
- SKEW DEFINITIONS (SLLA060 - Updated: 08/13/1999)
- THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS (SZZA017A - Updated: 09/15/1999)

Related Documents

- A STATISTICAL SURVEY OF COMMON-MODE NOISE (SLLA057, 131 KB - Updated: 12/23/1999)

Table Data Updated on: 6/2/2000