ADC083000 8-Bit, 3 GSPS, High Performance, Low Power A/D Converter

Check for Samples: ADC083000

FEATURES

- **Single +1.9V ±0.1V Operation**
- **Choice of SDR or DDR Output Clocking**
- **Serial Interface for Extended Control**
- **Adjustment of Input Full-Scale Range and Offset**
- **Duty Cycle Corrected Sample Clock**
- **Test Pattern**

APPLICATIONS

- **Direct RF Down Conversion**
- **Digital Oscilloscopes**
- **Satellite Set-Top Boxes**
- **Communications Systems**
- **Test Instrumentation**

KEY SPECIFICATIONS

- **Resolution 8 Bits**
- **Max Conversion Rate 3 GSPS (min)**
- **Error Rate 10^{-18} (typ)**
- **ENOB @ 748 MHz Input 7.0 Bits (typ)**
- **SNR @ 748 MHz 44.5 dB (typ)**
- **Full Power Bandwidth 3 GHz (typ)**
- **Power Consumption**
  - **Operating 1.9 W (typ)**
  - **Power Down Mode 25 mW (typ)**

DESCRIPTION

The ADC083000 is a single, low power, high performance CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 3.4 GSPS. Consuming a typical 1.9 Watts at 3 GSPS from a single 1.9 Volt supply, this device is specified to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable an excellent response of all dynamic parameters up to Nyquist, producing a high 7.0 Effective Number Of Bits, (ENOB) with a 748 MHz input signal and a 3 GHz sample rate while providing a 10^{-18} Word Error Rate. The ADC083000 achieves a 3 GSPS sampling rate by utilizing both the rising and falling edge of a 1.5 GHz input clock. Output formatting is offset binary and the LVDS digital outputs are compatible with IEEE 1596.3-1996, with the exception of an adjustable common mode voltage between 0.8V and 1.15V.

The ADC has a 1:4 demultiplexer that feeds four LVDS buses and reduces the output data rate on each bus to a quarter of the sampling rate.

The converter typically consumes less than 25 mW in the Power Down Mode and is available in a 128-lead, thermally enhanced exposed pad HLQFP and operates over the Industrial ($-40°C \le T_A \le +85°C$) temperature range.

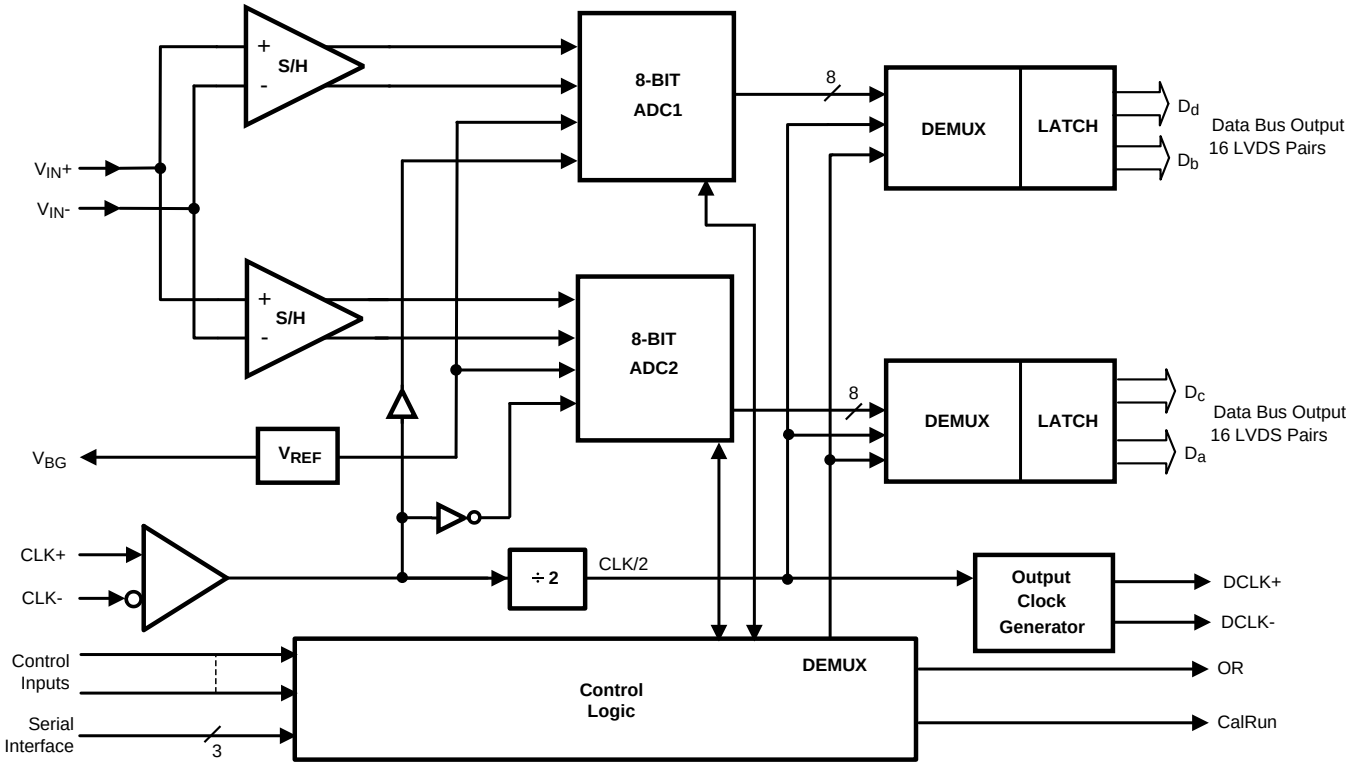
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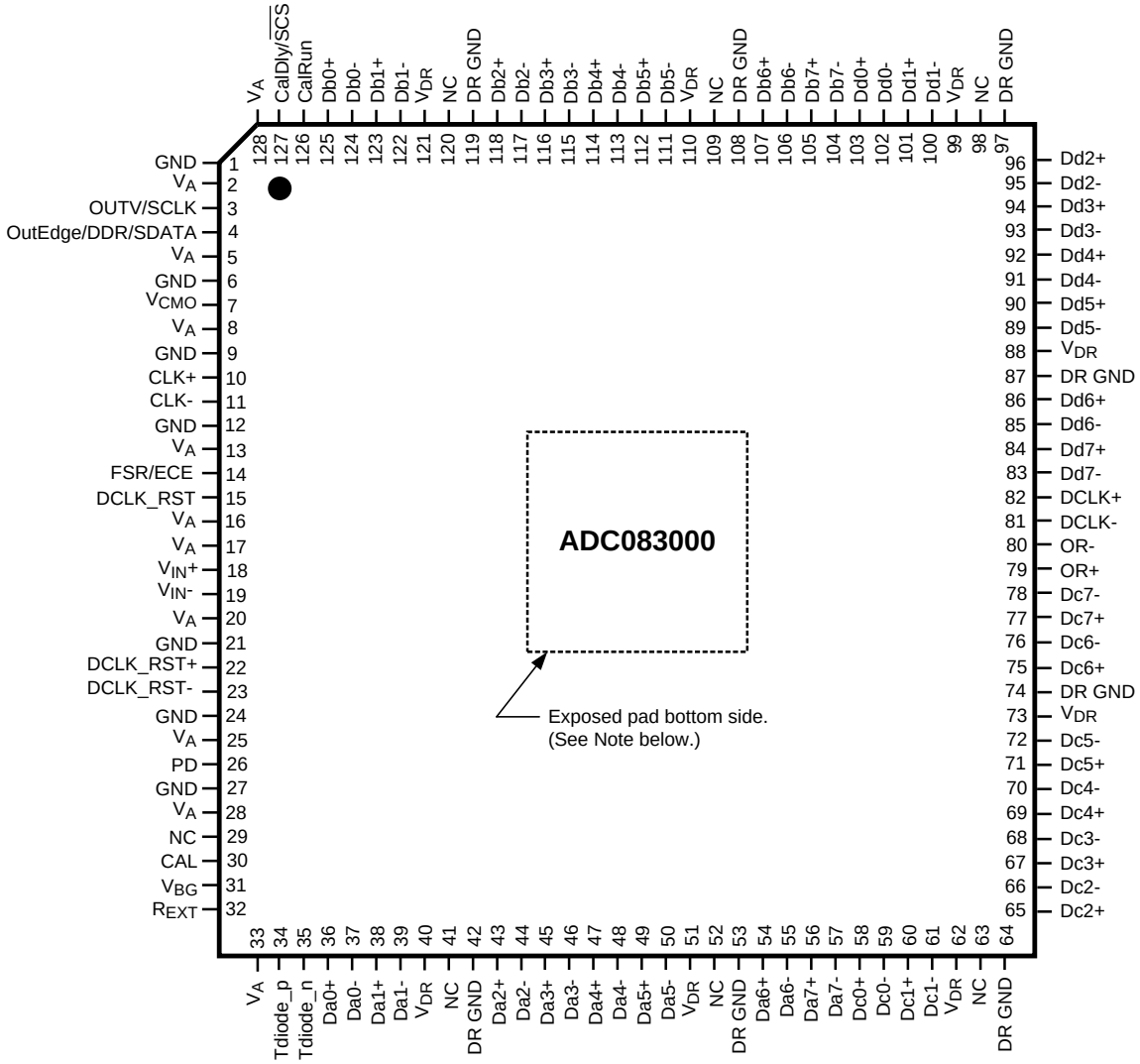
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Block Diagram



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Pin Configuration

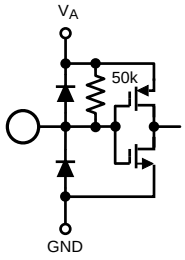
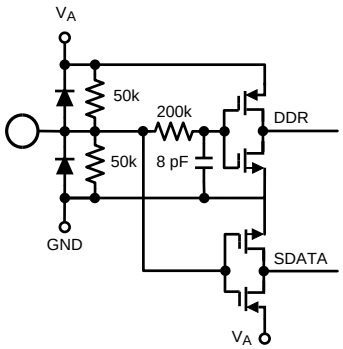
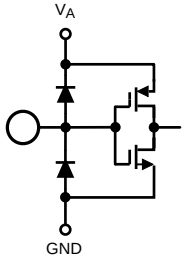
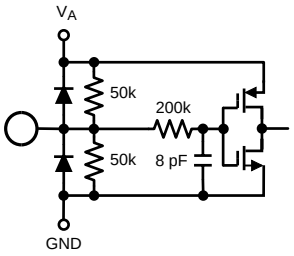
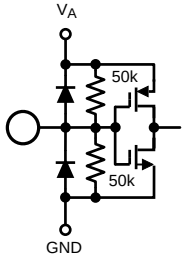


NOTE

The exposed pad on the bottom of the package must be soldered to a ground plane to ensure rated performance.

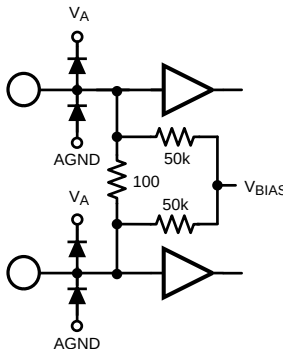
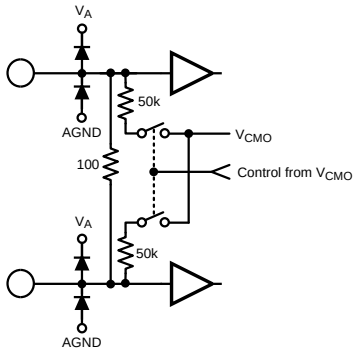
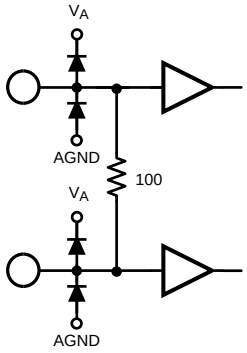
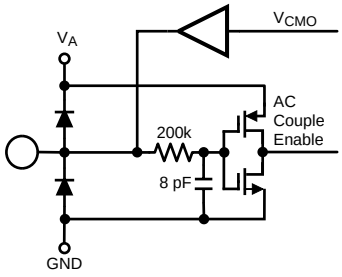
Pin Descriptions and Equivalent Circuits

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
3	OutV / SCLK		**Output Voltage Amplitude / Serial Interface Clock** **(Input):LVCMOS** Tie this pin high for normal differential DCLK and data amplitude. Ground this pin for a reduced differential output amplitude and reduced power consumption. See The LVDS Outputs. When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data. See NORMAL/EXTENDED CONTROL for details on the extended control mode. See THE SERIAL INTERFACE for description of the serial interface.
4	OutEdge / DDR / SDATA		**Edge Select / Double Data Rate / Serial Data** **(Input):LVCMOS** This input sets the output edge of DCLK+ at which the output data transitions. (See OutEdge Setting). When this pin is floating or connected to 1/2 the supply voltage, DDR clocking is enabled. When the extended control mode is enabled, this pin functions as the SDATA input. See NORMAL/EXTENDED CONTROL for details on the extended control mode. See THE SERIAL INTERFACE for description of the serial interface.
15	DCLK_RST		**DCLK Reset** **(Input):LVCMOS** A positive pulse on this pin is used to reset and synchronize the DCLK outs of multiple converters. See MULTIPLE ADC SYNCHRONIZATION for detailed description. When bit 14 in the Configuration Register (address 1h) is set to 0b, this single-ended DCLK_RST pin is selected. See also pins 22,23 description.
26	PD		**Power Down** **(Input):LVCMOS** A logic high on the PD pin puts the entire device into the Power Down Mode.
30	CAL		**Calibration Cycle Initiate** **(Input):LVCMOS** A minimum 80 input clock cycles logic low followed by a minimum of 80 input clock cycles high on this pin initiates the calibration sequence. See Calibration for an overview of self-calibration and On-Command Calibration for a description of on-command calibration.
14	FSR/ECE		**Full Scale Range Select / Extended Control Enable** **(Input):LVCMOS** In non-extended control mode, a logic low on this pin sets the full-scale differential input range to 600 mV_{P-P}. A logic high on this pin sets the full-scale differential input range to 820 mV_{P-P}. See The Analog Inputs. To enable the extended control mode, whereby the serial interface and control registers are employed, allow this pin to float or connect it to a voltage equal to $V_A/2$. See NORMAL/EXTENDED CONTROL for information on the extended control mode.
127	CalDly / $\overline{SCS}$		**Calibration Delay / Serial Interface Chip Select** **(Input):LVCMOS** With a logic high or low on pin 14, this pin functions as Calibration Delay and sets the number of input clock cycles after power up before calibration begins (See Calibration). With pin 14 floating, this pin acts as the enable pin for the serial interface input and the CalDly value becomes "0" (short delay with no provision for a long power-up calibration delay).

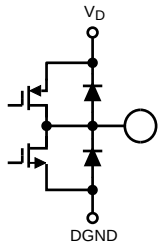
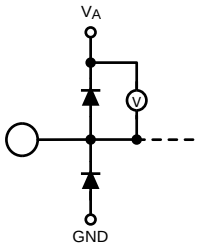
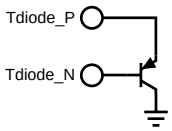
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Pin Descriptions and Equivalent Circuits (continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
10 11	CLK+ CLK-		**Sampling Clock Input** **(Input):LVDS** The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on both the rising and falling edge of CLK. See Acquiring the Input for a description of acquiring the input and THE SAMPLE CLOCK INPUT for an overview of the clock inputs.
18 19	V_{IN}+ V_{IN}−		**Signal Input** **(Input):Analog** The differential full-scale input range is 600 mV_{P-P} when the FSR pin is low, or 820 mV_{P-P} when the FSR pin is high. In the Extended Control Mode, FSR is determined by the Full-Scale Voltage Adjust register (address 3h, bits 15:7).
22 23	DCLK_RST+ DCLK_RST-		**Sample Clock Reset** **(Input):LVDS** A positive differerntial pulse on these pins is used to reset and synchronize the DCLK outs of multiple converters. See MULTIPLE ADC SYNCHRONIZATION for detailed description. When bit 14 in the Configuration Register (address 1h) is set to 1b, these differential DCLK_RST pins are selected. See also pin 15 description.
7	V_{CMO}		**Common Mode Voltage** **(Output):Analog -** The voltage output at this pin is required to be the common mode input voltage at V_{IN}+ and V_{IN}− when d.c. coupling is used. This pin should be grounded when a.c. coupling is used at the analog input. This pin is capable of sourcing or sinking 100µA and can drive a load up to 80 pF. See THE ANALOG INPUT.
31	V_{BG}		**Bandgap Output Voltage** **(Output):Analog -** Capable of 100 µA source/sink and can drive a load up to 80 pF.

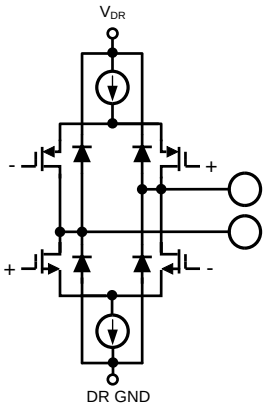
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Pin Descriptions and Equivalent Circuits (continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
126	CalRun		**Calibration Running (Output):LVCMOS -** This pin is at a logic high while a calibration is running.
32	R_{EXT}		**External Bias Resistor Connection Analog -** Nominal value is 3.3k-Ohms (±0.1%) to ground. See Calibration.
34 35	Tdiode_P Tdiode_N		**Temperature Diode Analog -** Positive (Anode) and Negative (Cathode). These pins may be used for die temperature measurements, however no specified accuracy is implied or ensured. Noise coupling from adjacent output data signals has been shown to affect temperature measurements using this feature. See Thermal Management.

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Pin Descriptions and Equivalent Circuits (continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
36 / 37 38 / 39 43 / 44 45 / 46 47 / 48 49 / 50 54 / 55 56 / 57 58 / 59 60 / 61 65 / 66 67 / 68 69 / 70 71 / 72 75 / 76 77 / 78	Da0+ / Da0- Da1+ / Da1- Da2+ / Da2− Da3+ / Da3- Da4+ / Da4− Da5+ / Da5- Da6+ / Da6− Da7+ / Da7- Dc0+ / Dc0- Dc1+ / Dc1- Dc2+ / Dc2− Dc3+ / Dc3- Dc4+ / Dc4− Dc5+ / Dc5- Dc6+ / Dc6− Dc7+ / Dc7-		**A and C Data** **(Output):LVDS** Data Outputs from the first internal converter. The data should be extracted in the order ABCD. These outputs should always be terminated with a 100Ω differential resistor at the receiver.
83 / 84 85 / 86 89 / 90 91 / 92 93 / 94 95 / 96 100 / 101 102 / 103 104 / 105 106 / 107 111 / 112 113 / 114 115 / 116 117 / 118 122 / 123 124 / 125	Dd7− / Dd7+ Dd6- / Dd6+ Dd5− / Dd5+ Dd4- / Dd4+ Dd3- / Dd3+ Dd2- / Dd2+ Dd1− / Dd1+ Dd0- / Dd0+ Db7- / Db7+ Db6- / Db6+ Db5− / Db5+ Db4- / Db4+ Db3− / Db3+ Db2- / Db2+ Db1− / Db1+ Db0- / Db0+		**B and D Data** **(Output):LVDS** Data Outputs from the second internal converter. The data should be extracted in the order ABCD. These outputs should always be terminated with a 100Ω differential resistor at the receiver.
79 80	OR+ OR-		**Out Of Range** **(Output):LVDS -** A differential high at these pins indicates that the differential input is out of range (outside the range ±325 mV or ±435 mV as defined by the FSR pin). These outputs should always be terminated with a 100Ω differential resistor at the receiver.
82 81	DCLK+ DCLK-		**Differential Clock** **(Output):LVDS -** The Differential Clock output used to latch the output data. Delayed and non-delayed data outputs are supplied synchronous to this signal. DCLK is 1/2 the sample clock rate in SDR mode and 1/4 the sample clock rate in the DDR mode. These outputs should always be terminated with a 100Ω differential resistor at the receiver. The DCLK outputs may not be active during the calibration cycle depending upon the setting of Configuration Register (address 1h), bit- 14 (RTD). See Calibration.
2, 5, 8, 13, 16, 17, 20, 25, 28, 33, 128	V_A		**Analog power supply pins** **(Power)** - Bypass these pins to ground.
40, 51 ,62, 73, 88, 99, 110, 121	V_{DR}		**Output Driver power supply pins** **(Power) -** Bypass these pins to DR GND.
1, 6, 9, 12, 21, 24, 27	GND		**(Gnd) -** Ground return for V_A.
42, 53, 64, 74, 87, 97, 108, 119	DR GND		**(Gnd) -** Ground return for V_{DR}.
29,41,52, 63, 98, 109, 120	NC		**No Connection** Make no connection to these pins

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

Supply Voltage (V_A, V_{DR})		2.2V
Supply Difference V_A - V_{DR}		0V to -100mV
Voltage on Any Input Pin (Except V_{IN}+, V_{IN}-)		−0.15V to (V_A + 0.15V)
Voltage on V_{IN}+, V_{IN}- (Maintaining Common Mode)		-0.15V to 2.5V
Ground Difference |GND - DR GND|		0V to 100 mV
Input Current at Any Pin (4)		±25 mA
Package Input Current (4)		±50 mA
Power Dissipation at $T_A \le 85°C$		2.3 W
ESD Susceptibility (5)	Human Body Model	2500V
	Machine Model	250V
Storage Temperature		−65°C to +150°C
Soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to www.ti.com/packaging. (6)		

(1) All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no specification of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power and ground pins.
(5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.
(6) Reflow temperature profiles are different for lead-free and non-lead-free packages.

OPERATING RATINGS (1)(2)

Ambient Temperature Range	$-40°C \le T_A \le +85°C$
Supply Voltage (V_A)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
Analog Input Common Mode Voltage	V_{CMO} ±50mV
V_{IN}+, V_{IN}- Voltage Range (Maintaining Common Mode)	0V to 2.15V (100% duty cycle) 0V to 2.5V (10% duty cycle)
Ground Difference (|GND - DR GND|)	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	$0.4V_{P-P}$ to $2.0V_{P-P}$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no specification of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

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PACKAGE THERMAL RESISTANCE

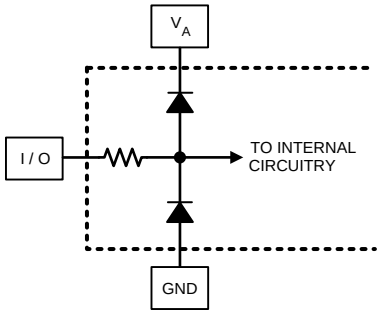
Package	θ_{JA}	$\theta_{JC\ (Top\ of\ Package)}$	$\theta_{J\text{-}PAD\ (Thermal\ Pad)}$
128-Lead Exposed Pad HLQFP	26°C / W	10°C / W	2.8°C / W

CONVERTER ELECTRICAL CHARACTERISTICS

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $820mV_{P\text{-}P}$, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5GHz at $0.5V_{P\text{-}P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
INL	Integral Non-Linearity (Best fit)	DC Coupled, 1MHz Sine Wave Over Ranged	±0.35	**±0.9**	LSB (max)
DNL	Differential Non-Linearity	DC Coupled, 1MHz Sine Wave Over Ranged	±0.20	**±0.6**	LSB (max)
	Resolution with No Missing Codes			**8**	Bits
V_{OFF}	Offset Error		-0.20		LSB
V_{OFF}_ADJ	Input Offset Adjustment Range	Extended Control Mode	±45		mV
PFSE	Positive Full-Scale Error (4)		−1.6	**±25**	mV (max)
NFSE	Negative Full-Scale Error (4)		−1.00	**±25**	mV (max)
FS_ADJ	Full-Scale Adjustment Range	Extended Control Mode	±20	**±15**	%FS
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth		3		GHz
	Word Error Rate		10^{-18}		Errors/Sample
	Gain Flatness	0.0 to -1.0 dBFS	50 to 950		MHz
ENOB	Effective Number of Bits	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	7.2	**6.8**	Bits (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	7.0	**6.6**	Bits (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	6.5		Bits

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



(2) To ensure accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.

(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).

(4) Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See Figure 2. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

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CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $820mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5GHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits T_A = 25°C, unless otherwise noted. (1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	45.1	**42.4**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	43.9	**41.2**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	41.1		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	45.4	**43.5**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	44.2	**42.2**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	41.8		dB
THD	Total Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	-57	**-49**	dB (max)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	-56	**-48**	dB (max)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	-49.5		dB
2nd Harm	Second Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	−68		dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	−66		dB
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	−56		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	−64		dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	−58		dB
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	−52		dB
SFDR	Spurious-Free dynamic Range	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	57	**49**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	54.5	**48**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	52.0		dB
IMD	Intermodulation Distortion	f_{IN1} = 749.084 MHz, V_{IN} = FSR − 7 dB f_{IN2} = 756.042 MHz, V_{IN} = FSR − 7 dB	-52		dBFS
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
V_{IN}	Full Scale Analog Differential Input Range	FSR pin 14 Low	600	**550**	mV_{P-P} (min)
				650	mV_{P-P} (max)
		FSR pin 14 High	820	**770**	mV_{P-P} (min)
				870	mV_{P-P} (max)

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CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $820mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5GHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
V_{CMI}	Analog Input Common Mode Voltage		V_{CMO}	**V_{CMO} − 50** **V_{CMO} + 50**	mV (min) mV (max)
C_{IN}	Analog Input Capacitance (5)(6)	Differential	0.08		pF
		Each input pin to ground	2.2		pF
R_{IN}	Differential Input Resistance		100	**95** **105**	Ω (min) Ω (max)
ANALOG OUTPUT CHARACTERISTICS					
V_{CMO}	Common Mode Output Voltage	I_{CMO} = ±100 µA	1.26	**0.95** **1.45**	V (min) V (max)
V_{CMO_LVL}	V_{CMO} input threshold to set DC Coupling mode	V_A = 1.8V	0.60		V
		V_A = 2.0V	0.66		V
TC V_{CMO}	Common Mode Output Voltage Temperature Coefficient	T_A = −40°C to +85°C	118		ppm/°C
C_{LOAD} V_{CMO}	Maximum V_{CMO} load Capacitance			**80**	pF
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.26	**1.20** **1.33**	V (min) V (max)
TC V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = −40°C to +85°C, I_{BG} = ±100 µA	28		ppm/°C
C_{LOAD} V_{BG}	Maximum Bandgap Reference load Capacitance			**80**	pF
TEMPERATURE DIODE CHARACTERISTICS					
ΔV_{BE}	Temperature Diode Voltage	192 µA vs. 12 µA, T_J = 25°C	71.23		mV
		192 µA vs. 12 µA, T_J = 85°C	85.54		mV
LVDS INPUT CHARACTERISTICS					
V_{ID}	Differential Clock Input Level	Sine Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
		Square Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
I_I	Input Current	V_{IN} = 0 or V_{IN} = V_A	±1		µA
C_{IN}	Input Capacitance (7)(8)	Differential	0.02		pF
		Each input to ground	1.5		pF

(5) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(6) This parameter is specified by design and is not tested in production.
(7) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(8) This parameter is specified by design and is not tested in production.

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CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $820mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5GHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
LVDS OUTPUT CHARACTERISTICS					
V_{OD}	LVDS Differential Output Voltage	Measured differentially, OutV = V_A, V_{BG} = Floating (9)	680	**470**	mV_{P-P} (min)
				920	mV_{P-P} (max)
		Measured differentially, OutV = GND, V_{BG} = Floating (9)	520	**380**	mV_{P-P} (min)
				720	mV_{P-P} (max)
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels		±1		mV
V_{OS}	Output Offset Voltage, see Figure 1	V_{BG} = Floating	800		mV
V_{OS}	Output Offset Voltage, see Figure 1	$V_{BG} = V_A$ (9)	1150		mV
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels		±1		mV
I_{OS}	Output Short Circuit Current	Output+ & Output- connected to 0.8V	±4		mA
Z_O	Differential Output Impedance		100		Ohms
LVCMOS INPUT CHARACTERISTICS					
V_{IH}	Logic High Input Voltage	See (10)		**0.85 x V_A**	V (min)
V_{IL}	Logic Low Input Voltage	See (10)		**0.15 x V_A**	V (max)
C_{IN}	Input Capacitance (11) (12)	Each input to ground	1.2		pF
LVCMOS OUTPUT CHARACTERISTICS					
V_{OH}	CMOS H level output	I_{OH} = -400uA (10)	1.65	**1.5**	V
V_{OL}	CMOS L level output	I_{OH} = 400uA (10)	0.15	**0.3**	V
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD = Low	734	**810**	mA (max)
I_{DR}	Output Driver Supply Current	PD = Low	300	**410**	mA (max)
P_D	Power Consumption	PD = Low	1.9	**2.3**	W (max)
		PD = High	25		mW
PSRR1	D.C. Power Supply Rejection Ratio	Change in offset with change in V_A from 1.8V to 2.0V	70		dB
PSRR2	A.C. Power Supply Rejection Ratio	248 MHz, $100mV_{P-P}$ riding on V_A	50		dB
AC ELECTRICAL CHARACTERISTICS - Sampling Clock					
f_{CLK1}	Maximum Input Clock Frequency	Sampling rate is 2x clock input		**1.5**	GHz (min)
f_{CLK2}	Minimum Input Clock Frequency	Sampling rate is 2x clock input	500		MHz

(9) Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 400mv (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 40mV (typical).
(10) This parameter is specified by design and/or characterization and is not tested in production.
(11) This parameter is specified by design and is not tested in production.
(12) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

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CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $820mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5GHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
t_{CYC}	Input Clock Duty Cycle	500MHz ≤ Input clock frequency ≤ 1.5 GHz (13)	50	**20** **80**	% (min) % (max)
t_{LC}	Input Clock Low Time	See (14)	333	**133**	ps (min)
t_{HC}	Input Clock High Time	See (14)	333	**133**	ps (min)
	DCLK Duty Cycle	See (14)	50	**45** **55**	% (min) % (max)
t_{AD}	Sampling (Aperture) Delay	Input CLK transition to Acquisition of Data	1.4		ns
t_{AJ}	Aperture Jitter		0.55		ps rms
t_{OD}	Input Clock to Data Output Delay (in addition to Pipeline Delay)	50% of Input Clock transition to 50% of Data transition	3.7		ns
	Pipeline Delay (Latency) (14) (15)	Dd Outputs		**13**	Input Clock Cycles
		Db Outputs		**14**	
		Dc Outputs		**13.5**	
		Da Outputs		**14.5**	
AC ELECTRICAL CHARACTERISTICS - Output Clock and Data (16)					
t_{LHT}	LH Transition Time - Differential	10% to 90%	150		ps
t_{HLT}	HL Transition Time - Differential	10% to 90%	150		ps
t_{SKEWO}	DCLK to Data Output Skew	50% of DCLK transition to 50% of Data transition, SDR Mode and DDR Mode, 0° DCLK (14)	±50		ps (max)
t_{OSU}	Data to DCLK Set-Up Time	DDR Mode, 90° DCLK (13)	570		ps
t_{OH}	DCLK to Data Hold Time	DDR Mode, 90° DCLK (13)	555		ps
AC ELECTRICAL CHARACTERISTICS - Serial Interface Clock					
f_{SCLK}	Serial Clock Frequency	See (14)	67		MHz
t_{SS}	Data to Serial Clock Setup Time	See (14)	2.5		ns (min)
t_{HS}	Data to Serial Clock Hold Time	See (14)	1		ns (min)
	Serial Clock Low Time			**6**	ns (min)
	Serial Clock High Time			**6**	ns (min)
AC ELECTRICAL CHARACTERISTICS - General Signals					
t_{SR}	Setup Time DCLK_RST±	See (13)	90		ps
t_{HR}	Hold Time DCLK_RST±		30		ps
t_{PWR}	Pulse Width DCLK_RST±	See (14)		**4**	CLK± Cyc. (min)
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)	See (14)	1		µs
t_{CAL}	Calibration Cycle Time		1.4×10^5		CLK± Cyc.
t_{CAL_L}	CAL Pin Low Time	See Figure 8 (14)		**80**	CLK± Cyc. (min)

(13) This parameter is specified by design and/or characterization and is not tested in production.
(14) This parameter is specified by design and is not tested in production.
(15) Each of the two converters of the ADC083000 has two LVDS output buses, which each clock data out at one quarter the sample rate. Bus Db has a pipeline latency that is one Input Clock cycle less than the latency of bus Dd. Likewise, bus Da has a pipeline latency that is one Input Clock cycle less than the latency of bus Dc.
(16) All parameters are measured through a transmission line and 100Ω termination using a 0.33pF load oscilloscope probe.

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CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $820mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5GHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
t_{CAL_H}	CAL Pin High Time	See Figure 8 (14)		**80**	CLK± Cyc. (min)
t_{CalDly}	Calibration delay CalDly = Low	See Calibration, Figure 8, (14)		**2^{25}**	CLK± Cyc. (min)
	Calibration delay CalDly = High	See Calibration, Figure 8, (14)		**2^{31}**	CLK± Cyc. (max)

SPECIFICATION DEFINITIONS

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sampling edge of the Clock input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the maximum deviation from the ideal step size of 1 LSB. Measured at 3 GSPS with a sine wave input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

Positive Gain Error = Offset Error − Positive Full-Scale Error

Negative Gain Error = −(Offset Error − Negative Full-Scale Error)

Gain Error = Negative Full-Scale Error − Positive Full-Scale Error = Positive Gain Error + Negative Gain Error

INTEGRAL NON-LINEARITY (INL) is the maximum departure of the transfer curve of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$V_{FS} / 2^n$

where V_{FS} is the differential full-scale amplitude of V_{IN} as set by the FSR input (pin-14) and "n" is the ADC resolution in bits, which is 8 for the ADC083000.

LVDS DIFFERENTIAL OUTPUT VOLTAGE (V_{OD}) is the absolute value of the difference between the V_D+ & V_D- outputs; each measured with respect to Ground.

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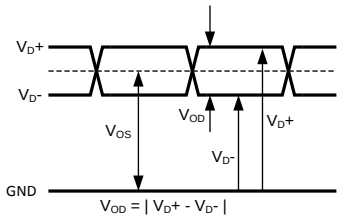


Figure 1.

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D- pins output voltage; i.e., [(V_D+) +(V_D-)]/2.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential -V_{IN} / 2. For the ADC083000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 128.

OUTPUT DELAY (t_{OD}) is the time delay from 50% point of the input clock transition, CLK, to the 50% point of the updated data transition at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential +V_{IN} / 2. For the ADC083000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected from the output and is measured with a 248 MHz, 100 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding d.c.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

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where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

WORD ERROR RATE is the probability of error and is defined as the probable number of errors per unit of time divided by the number of words seen in that amount of time. A Word Error Rate of 10^{-18} corresponds to a statistical error in one conversion about every four (4) years.

Transfer Characteristic

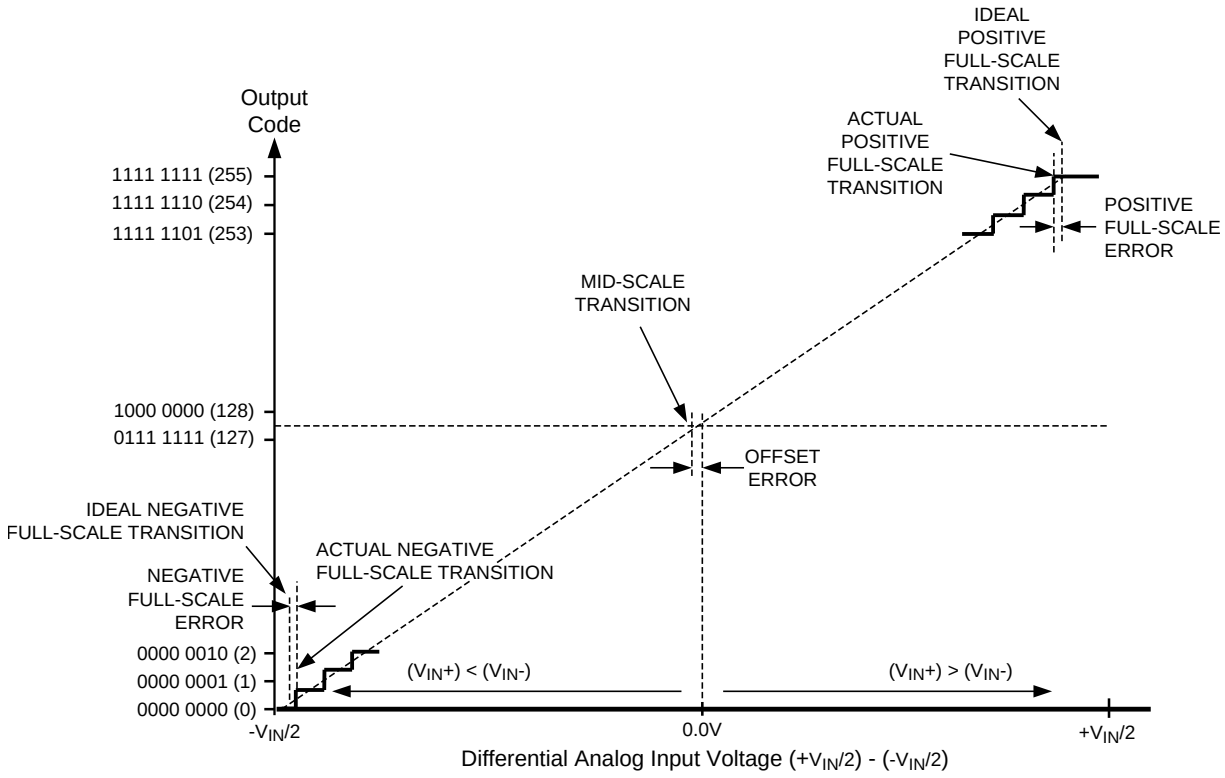


Figure 2. Input / Output Transfer Characteristic

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Timing Diagrams

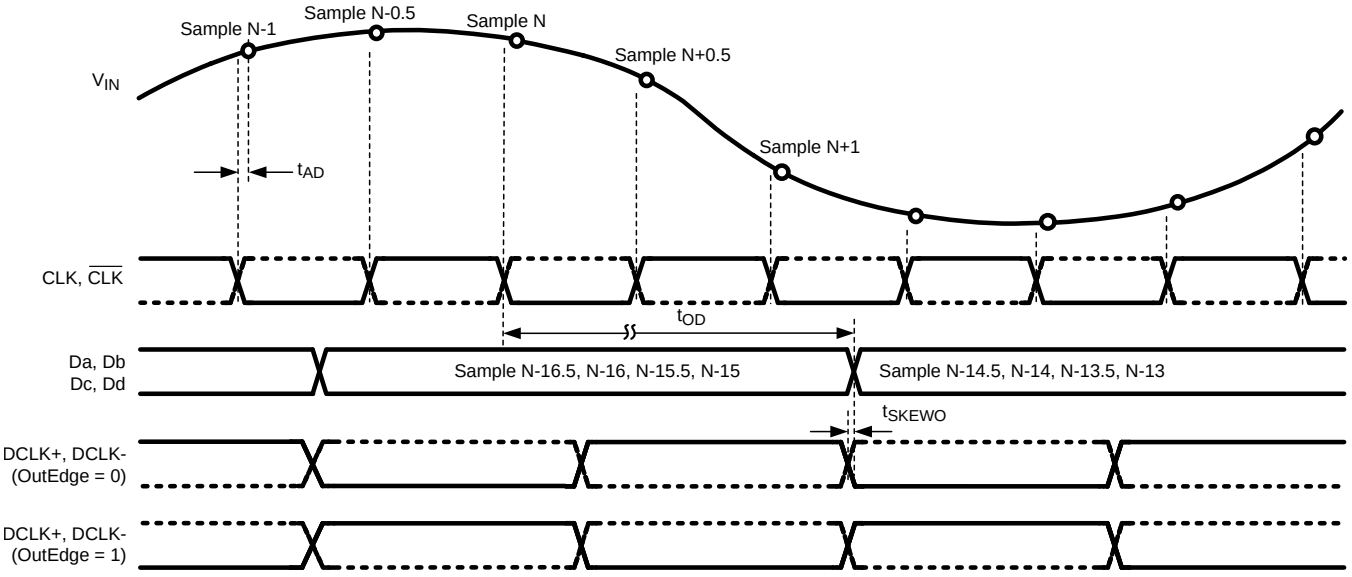


Figure 3. ADC083000 Timing — SDR Clocking

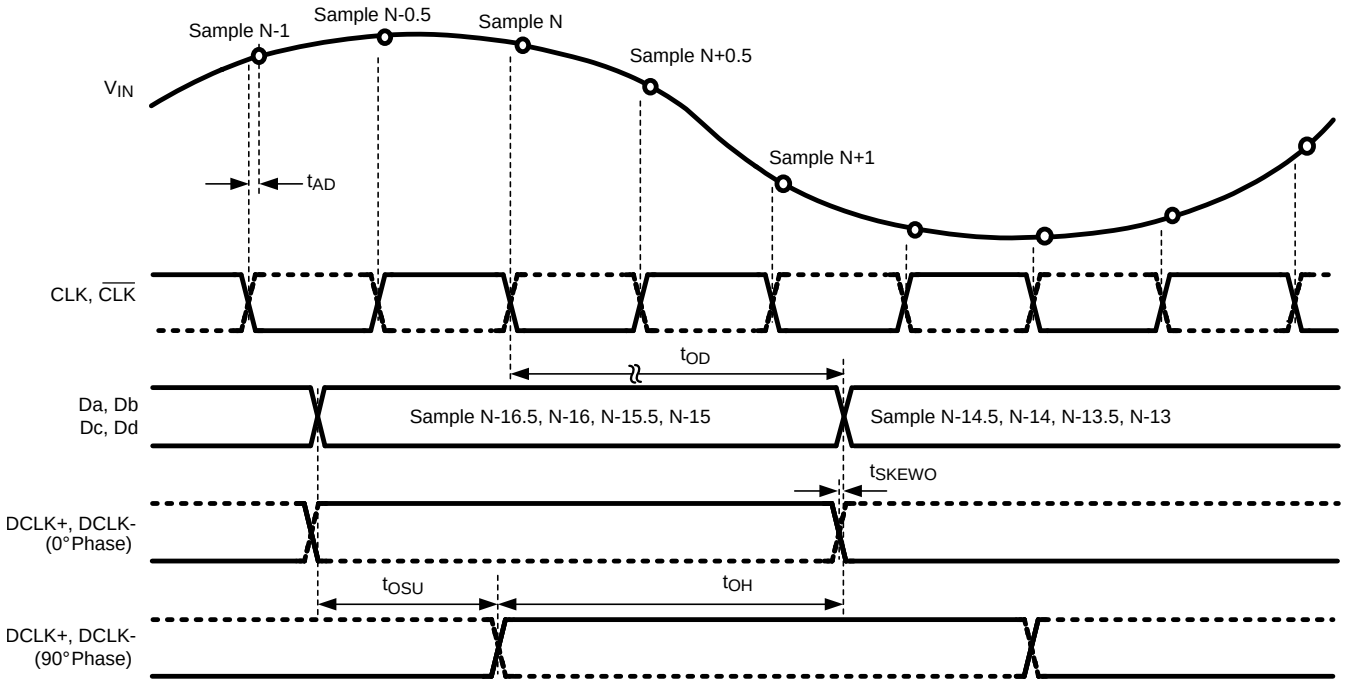


Figure 4. ADC083000 Timing — DDR Clocking

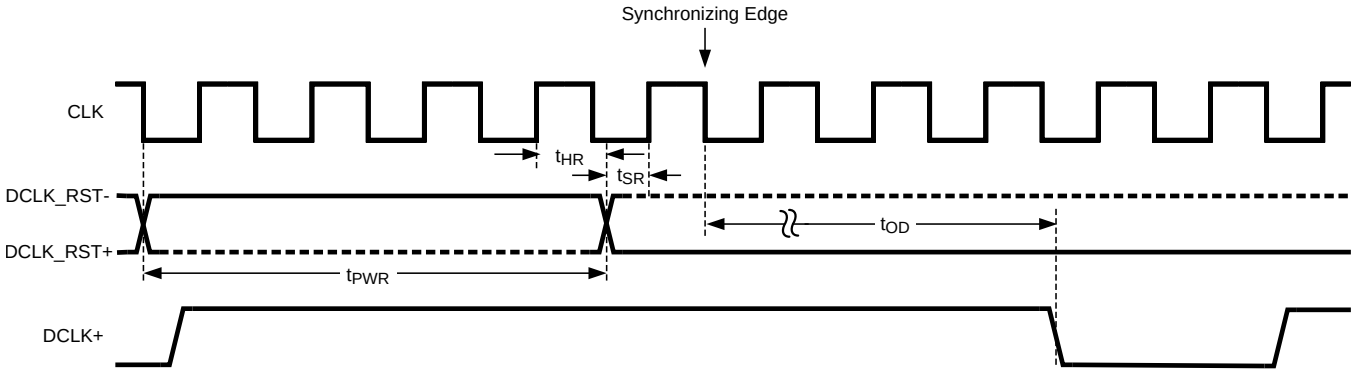


Figure 5. Clock Reset Timing in DDR Mode

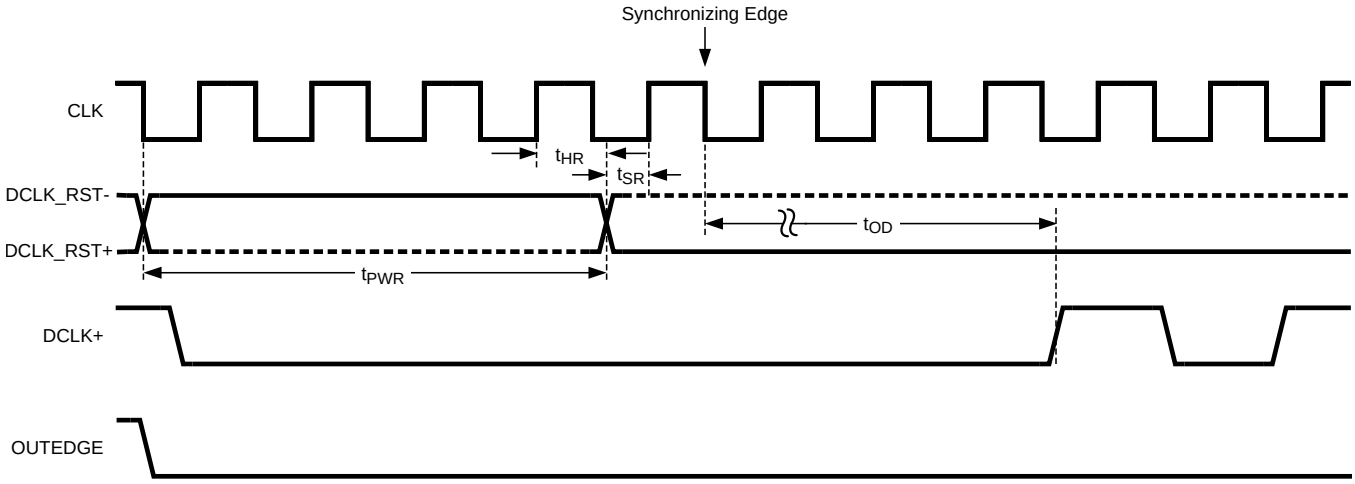


Figure 6. Clock Reset Timing in SDR Mode with OUTEDGE Low

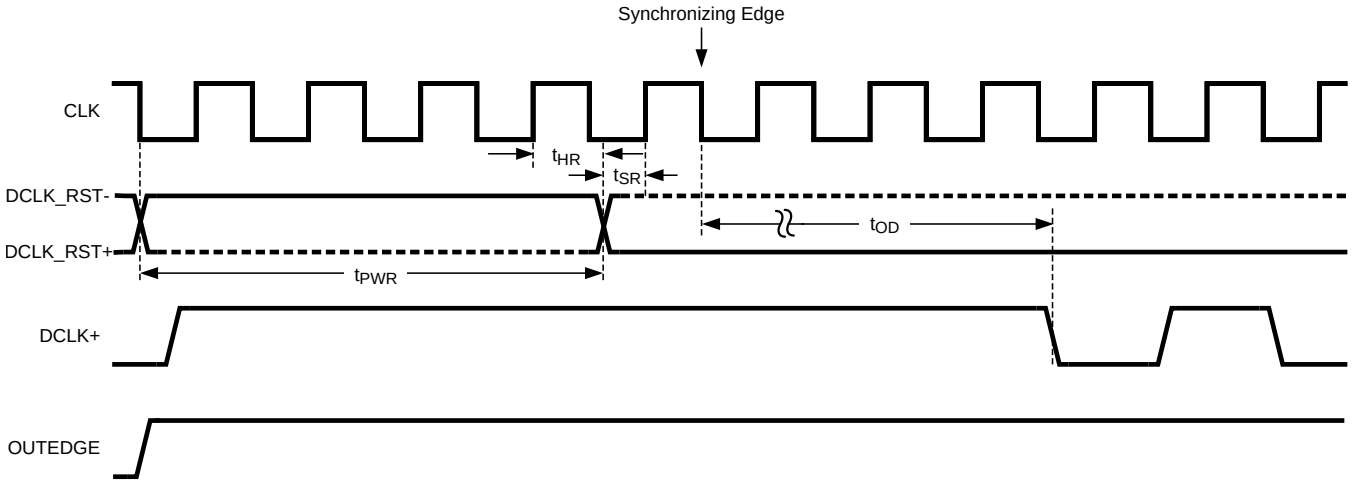


Figure 7. Clock Reset Timing in SDR Mode with OUTEDGE High

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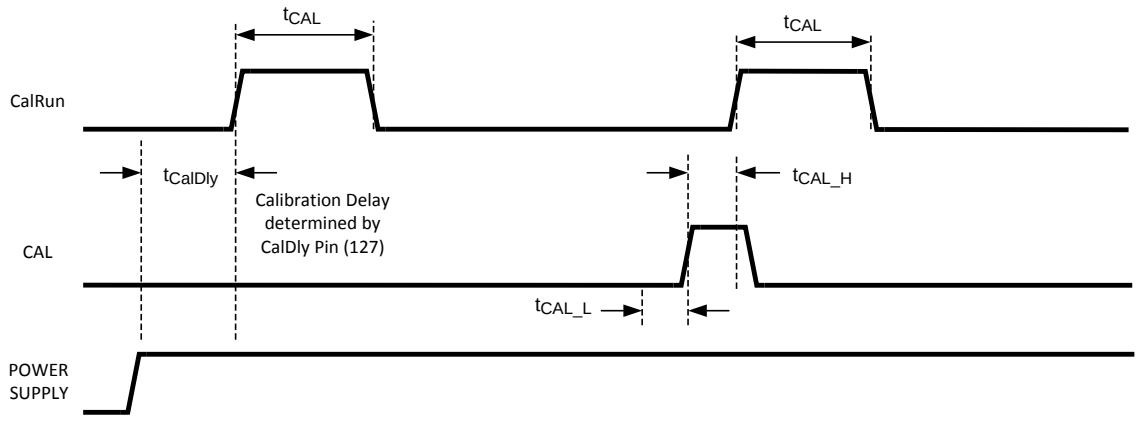


Figure 8. Calibration and On-Command Calibration Timing

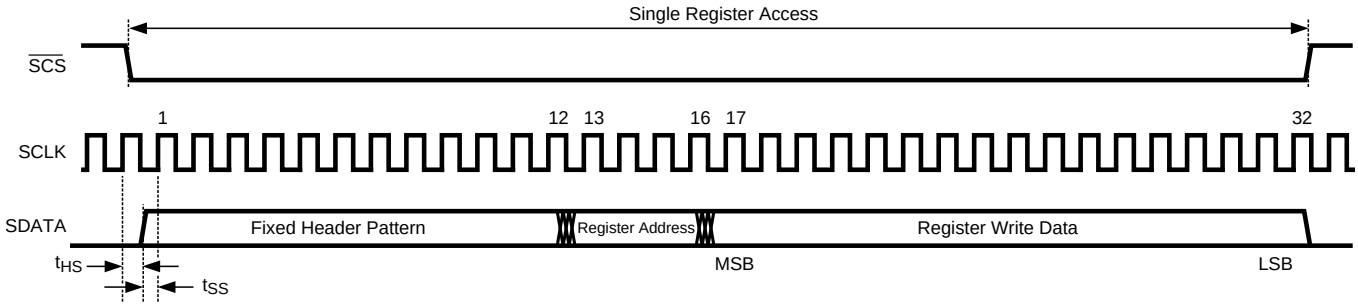


Figure 9. Serial Interface Timing

TYPICAL PERFORMANCE CHARACTERISTICS

V_A=V_{DR}=1.9V, F_{CLK}=1500MHz, T_A=25°C unless otherwise stated.

DNL vs. TEMPERATURE

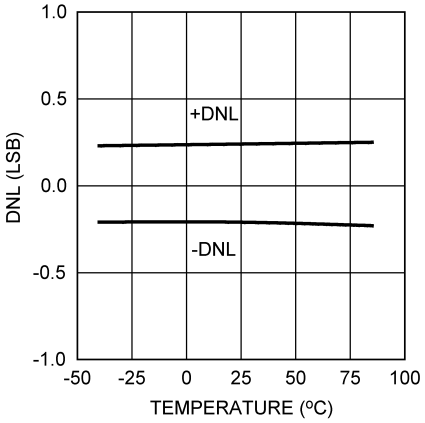


Figure 10.

INL vs. TEMPERATURE

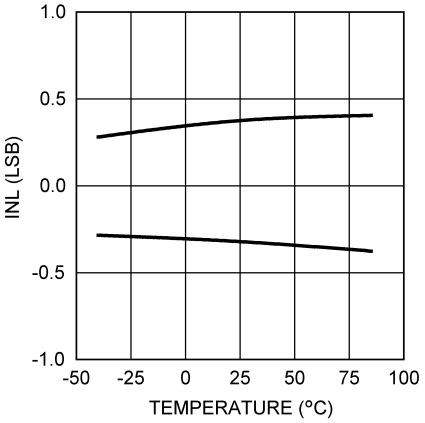


Figure 11.

DNL vs. CODE

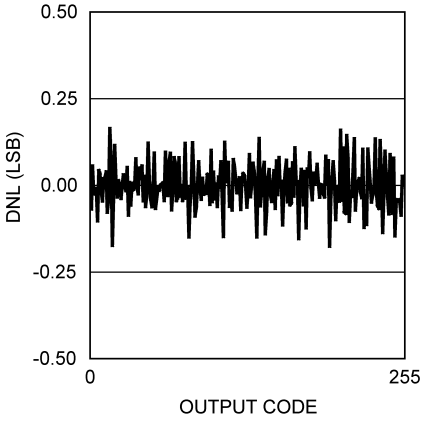


Figure 12.

INL vs. CODE

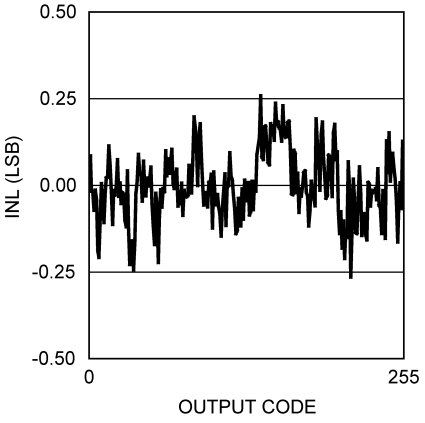


Figure 13.

POWER DISSIPATION vs. SAMPLE RATE

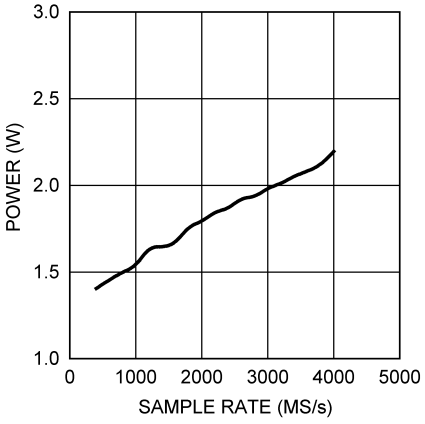


Figure 14.

ENOB vs. TEMPERATURE

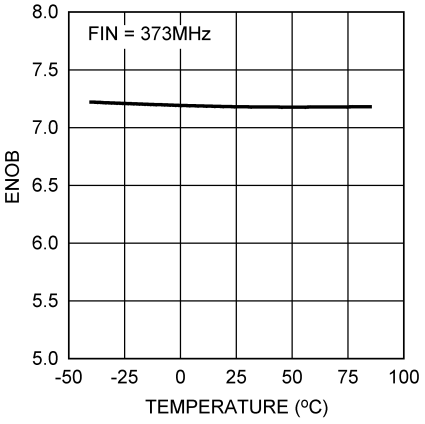


Figure 15.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_A=V_{DR}=1.9V, F_{CLK}=1500MHz, T_A=25°C unless otherwise stated.

ENOB vs. SUPPLY VOLTAGE

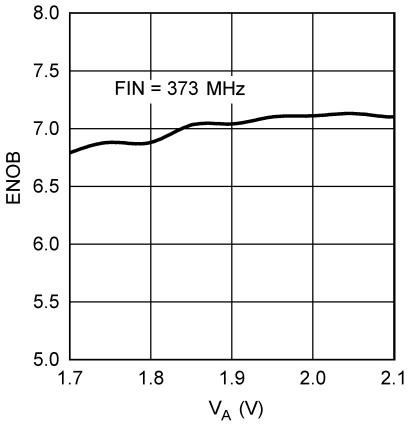


Figure 16.

ENOB vs. SAMPLE RATE

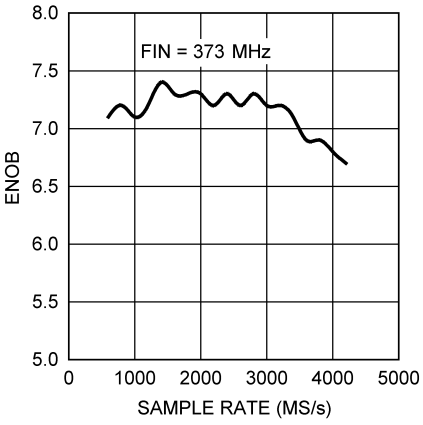


Figure 17.

ENOB vs. INPUT FREQUENCY

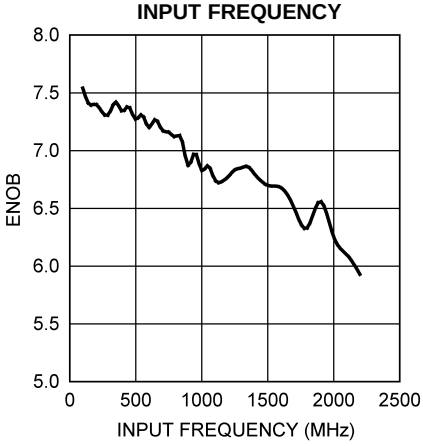


Figure 18.

SNR vs. TEMPERATURE

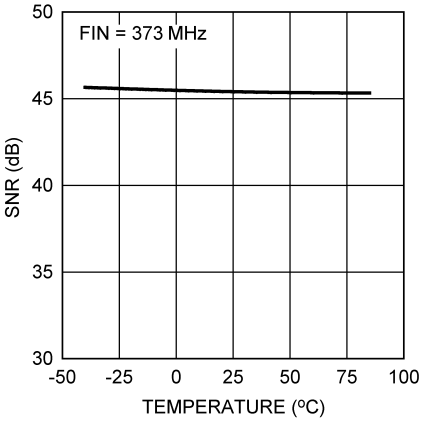


Figure 19.

SNR vs. SUPPLY VOLTAGE

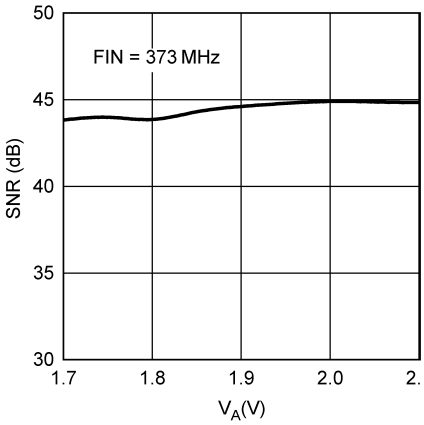


Figure 20.

SNR vs. SAMPLE RATE

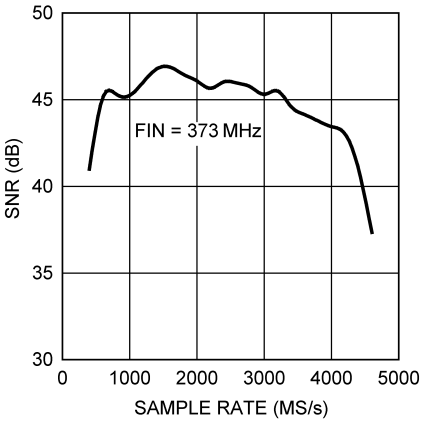


Figure 21.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_A=V_{DR}=1.9V, F_{CLK}=1500MHz, T_A=25°C unless otherwise stated.

SNR vs. INPUT FREQUENCY

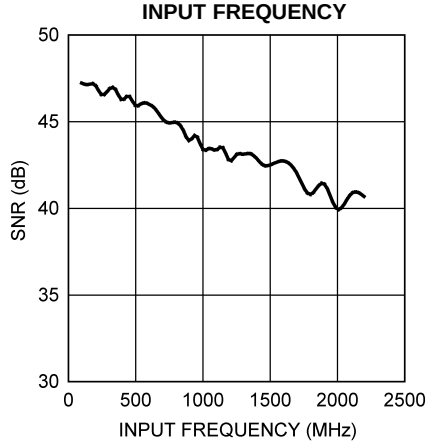


Figure 22.

THD vs. TEMPERATURE

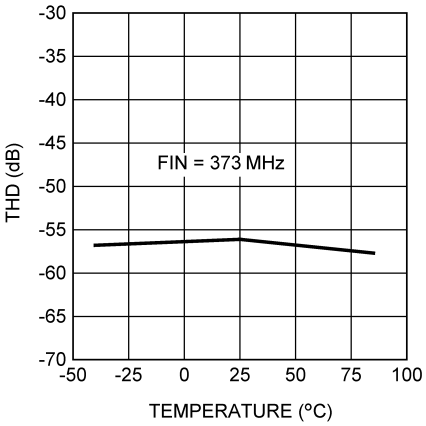


Figure 23.

THD vs. SUPPLY VOLTAGE

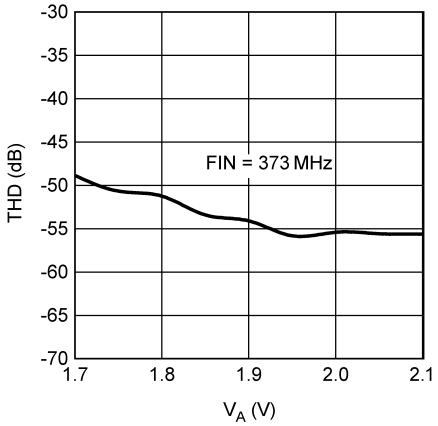


Figure 24.

THD vs. SAMPLE RATE

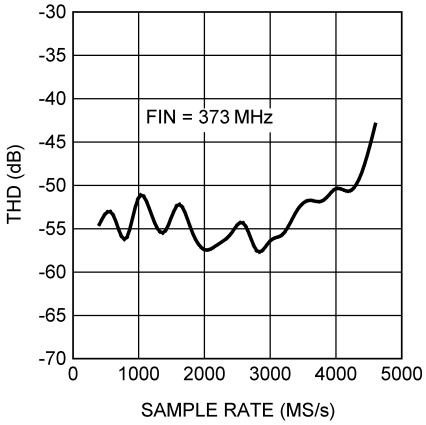


Figure 25.

THD vs. INPUT FREQUENCY

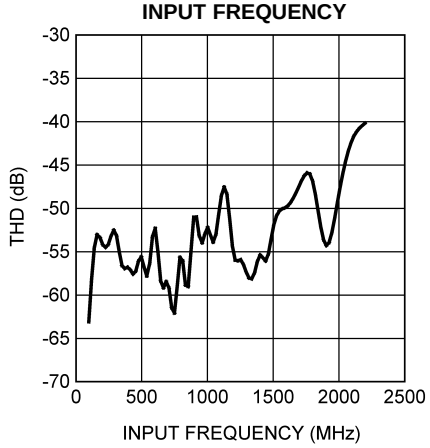


Figure 26.

SFDR vs. TEMPERATURE

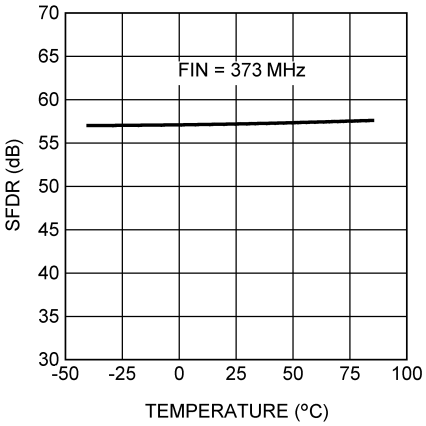


Figure 27.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_A=V_{DR}=1.9V, F_{CLK}=1500MHz, T_A=25°C unless otherwise stated.

SFDR vs. SUPPLY VOLTAGE

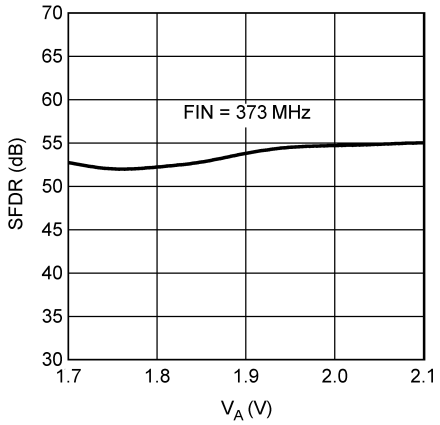


Figure 28.

SFDR vs. SAMPLE RATE

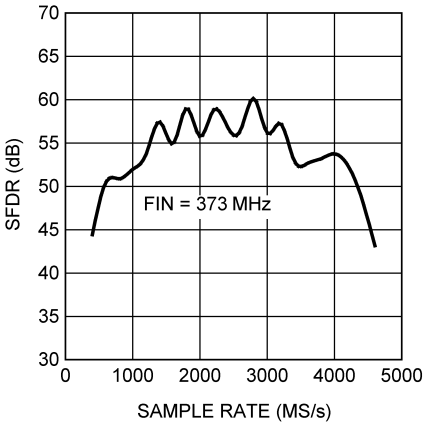


Figure 29.

SFDR vs. INPUT FREQUENCY

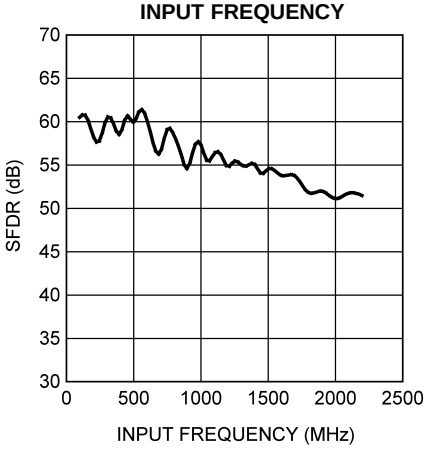


Figure 30.

Spectral Response at FIN = 373 MHz

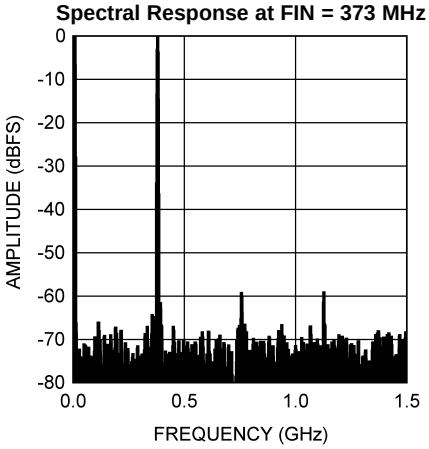


Figure 31.

Spectral Response at FIN = 748 MHz

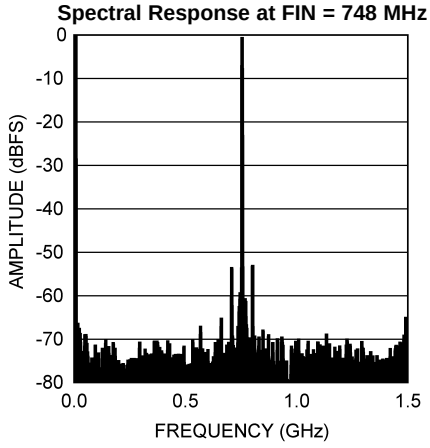


Figure 32.

Spectral Response at FIN = 1497 MHz

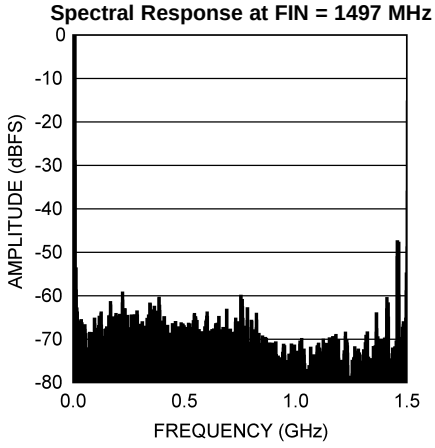


Figure 33.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_A=V_{DR}=1.9V, F_{CLK}=1500MHz, T_A=25°C unless otherwise stated.

FULL POWER BANDWIDTH

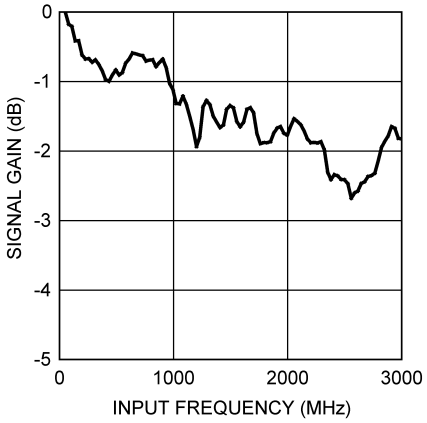


Figure 34.

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FUNCTIONAL DESCRIPTION

The ADC083000 is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section.

While it is generally poor practice to allow an active pin to float, pins 4 and 14 of the ADC083000 are designed to be left floating without jeopardy. In all discussions throughout this data sheet, whenever a function is called by allowing a control pin to float, connecting that pin to a potential of one half the V_A supply voltage will have the same effect as allowing it to float.

OVERVIEW

The ADC083000 uses a calibrated folding and interpolating architecture that achieves 7.2 effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 1.0 GSPS to 3.0 GSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at the analog input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from the converter is below negative full scale or above positive full scale.

The ADC083000 demultiplexes the data at 1:4 and is output on all four output busses at a quarter of the ADC sampling rate. The outputs must be interleaved by the user to provide output words at the full conversion rate.

The output levels may be selected to be normal or reduced voltage. Using reduced levels saves power but could result in erroneous data capture of some or all of the bits, especially at higher sample rates and in marginally designed systems.

Calibration

A calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the 100Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, calibration must be re-run by the user whenever the state of the FSR pin is changed. For best performance, we recommend an on command calibration be run after initial power up and the device has reached a stable temperature. Also, we recommend that an on command calibration be run whenever the operating temperature changes significantly relative to the specific system performance requirements. See On-Command Calibration for more information. Calibration can not be initiated or run while the device is in the power-down mode. See Power Down for information on the interaction between Power Down and Calibration.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least 80 input clock cycles, then hold it high for at least another 80 input clock cycles. The time taken by the calibration procedure is specified in the AC Characteristics Table. Holding the CAL pin high during power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned 80 input clock cycles low followed by 80 cycles high.

CalDly (pin 127) is used to select one of two delay times after the application of power to the start of calibration. This calibration delay is 2^{25} input clock cycles (about 22 ms at 3 GSPS) with CalDly low, or 2^{31} input clock cycles (about 1.4 seconds at 3 GSPS) with CalDly high. These delay values allow the power supply to come up and stabilize before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

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The CAL bit does not reset itself to zero automatically, but must be manually reset before another calibration event can be initiated. If no further calibration event is desired, the CAL bit may be left high indefinitely, with no negative consequences. The RTD bit setting is critical for running a calibration event with the Clock Phase Adjust enabled. If initiating a calibration event while the Clock Phase Adjust is enabled, the RTD bit must be set to high, or no calibration will occur. If initiating a calibration event while the Clock Phase Adjust is not enabled, a normal calibration will occur, regardless of the setting of the RTD bit.

Calibration Operation Notes:

- During the calibration cycle, the OR output may be active as a result of the calibration algorithm. All data on the output pins and the OR output are invalid during the calibration cycle.
- During the power-up calibration and during the on-command calibration when Resistor Trim Disable (address: 1h, bit 13) is not active (0b) , all clocks are halted on chip, including internal clocks and DCLK, while the input termination resistor is trimmed to a value that is equal to R_{EXT} / 33. This is to reduce noise during the input resistor calibration portion of the calibration cycle. See On-Command Calibration for information on maintaining DCLK operation during on-command calibration.
  - R_{EXT} is located between pin 32 and ground and must be 3300 Ω ±0.1%. With this value, the input termination resistor is trimmed to be 100 Ω. Because R_{EXT} is also used to set the proper current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of R_{EXT} should not be used.
- The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

Acquiring the Input

Data is acquired at both the rising and falling edges of CLK (pin 10) and the digital equivalent of that data is available at the digital outputs 13 input clock cycles later for the Dd output bus, 13.5 input clock cycles later for Dc output bus, 14 input clock cycles later for the Db output bus and 14.5 input clock cycles later for the Da output bus. See Table 1. There is an additional internal delay called t_{OD} before the data is available at the outputs. See Figure 3 and Figure 4.

The ADC083000 will convert as long as the input clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with calibration, enables very good SINAD/ENOB response beyond 1.5 GHz. The ADC083000 output data signaling is LVDS and the output format is offset binary.

Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, power down mode and full scale range setting. However, the ADC083000 also provides an Extended Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ either the normal control mode or the Extended Control mode at all times. When the device is in the Extended Control mode, pin-based control of several features is replaced with register-based control and those pin-based controls are disabled. These pins are OutV (pin 3), OutEdge/DDR (pin 4), FSR (pin 14). See NORMAL/EXTENDED CONTROL for details on the Extended Control mode.

The Analog Inputs

The ADC083000 must be driven with a differential input signal. Operation with a single-ended signal is not recommended as performance will suffer. It is important that the input signals are either a.c. coupled to the inputs with the V_{CMO} pin grounded, or d.c. coupled with the V_{CMO} pin left floating or lightly loaded. An input common mode voltage equal to the V_{CMO} output must be provided when d.c. coupling is used.

Two full-scale range settings are provided with pin 14 (FSR). A high on pin 14 causes an input full-scale range setting of 820 mV_{P-P}, while grounding pin 14 causes an input full-scale range setting of 600 mV_{P-P}.

In the Extended Control mode, the full-scale input range can be set to values between 560 mV_{P-P} and 840 mV_{P-P} through a serial interface. See THE ANALOG INPUT.

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Clocking

The ADC083000 sampling clock (CLK+/CLK-) must be driven with an a.c. coupled, differential clock signal. THE SAMPLE CLOCK INPUT describes the use of the clock input pins. A differential LVDS output clock (DCLK) is available for use in latching the ADC output data into whatever device is used to receive the data.

The ADC083000 offers options for CLK+/CLK- and DCLK clocking. For DCLK, the clock edge on which output data transitions, and a choice of Single Data Rate (SDR) or Double Data Rate (DDR) outputs are available.

The sampling clock CLK has optional duty cycle correction as part of its circuit. This feature is enabled by default and provides improved ADC clocking. This circuitry allows the ADC to be clocked with a signal source having a duty cycle of 80 to 20 % (worst case).

Output Demultiplexer

The ADC083000 utilizes both the rising and falling edge of the input clock, resulting in the overall sample rate being twice the input clock frequency or 3GSPS with a 1.5 GHz input clock. The demultiplexer outputs data on each of the four output busses at 750MHz with a 1.5GHz input clock.

All data is available in parallel at the output. The four bytes of parallel data that are output with each clock is in the following sampling order, from the earliest to the latest: Da, Db, Dc, Dd. Table 1 indicates what the outputs represent for the various sampling possibilities.

The ADC083000 includes an automatic clock phase background calibration feature which automatically and continuously adjusts the phase of the ADC input clock. This feature removes the need to manually adjust the clock phase and provides optimal ENOB performance.

Table 1. Input Channel Samples Produced at Data Outputs

Data Outputs (1)	Input/Output Relationship
Dd	ADC1 sampled with the fall of CLK, 13 cycles earlier
Db	ADC1 sampled with the fall of CLK, 14 cycles earlier
Dc	ADC2 sampled with the rise of CLK, 13.5 cycles earlier
Da	ADC2 sampled with the rise of CLK, 14.5 cycles earlier

(1) Always sourced with respect to fall of DCLK

OutEdge Setting

To help ease data capture in the SDR mode, the output data may be caused to transition on either the positive or the negative edge of the output data clock (DCLK). This is chosen with the OutEdge input (pin 4). A high on the OutEdge input pin causes the output data to transition on the rising edge of DCLK+, while grounding this input causes the output to transition on the falling edge of DCLK+. See Output Edge Synchronization.

Double Data Rate

A choice of single data rate (SDR) or double data rate (DDR) output is offered. When the device is in DDR mode, address 1h, bit 8 of the Configuration Register must be set to 0b. With single data rate the output clock (DCLK) frequency is the same as the data rate of the two output buses. With double data rate the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK. DDR clocking is enabled in non-Extended Control mode by allowing pin 4 to float.

The LVDS Outputs

The data outputs, Out Of Range (OR) and DCLK are LVDS. Output current sources provide 3 mA of output current to a differential 100 Ohm load when the OutV input (pin 3) is high or 2.2 mA when the OutV input is low. For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low, which results in lower power consumption. If the LVDS lines are long and/or the system in which the ADC083000 is used is noisy, it may be necessary to tie the OutV pin high.

The LVDS data outputs have a typical common mode voltage of 800mV when the V_{BG} pin is floating. This common mode voltage can be increased to 1.150V by tying the V_{BG} pin to V_A if a higher common mode is required.

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NOTE

Tying the V_{BG} pin to V_A will also increase the differential LVDS output voltage (V_{OD}) by up to 40mV.

Power Down

The ADC083000 is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode. In this power down mode the data output pins (positive and negative) including DCLK+/- and OR +/- are put into a high impedance state and the device power consumption is reduced to a minimal level.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

NORMAL/EXTENDED CONTROL

The ADC083000 may be operated in one of two modes. In the Normal Mode, the user affects available configuration and control of the device through several control pins. The "extended control mode" provides additional configuration and control options through the serial interface and a set of 6 internal registers. The two control modes are selected with pin 14 (FSR/ECE: Extended Control Enable). The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational.

Table 2 shows how several of the device features are affected by the control mode chosen.

Table 2. Features and Modes

Feature	Normal Control Mode	Extended Control Mode
SDR or DDR Clocking	Selected with pin 4	Selected with nDE in the Configuration Register (1h; bit-10). When the device is in DDR mode, address 1h, bit-8 must be set to 0b.
DDR Clock Phase	Not Selectable (0° Phase Only)	Selected with DCP in the Configuration Register (1h; bit-11).
SDR Data transitions with rising or falling DCLK edge	Selected with pin 4	Selected with OE in the Configuration Register (1h; bit-8).
LVDS output level	Selected with pin 3	Selected with the OV in the Configuration Register (1h; bit-9).
Power-On Calibration Delay	Delay Selected with pin 127	Short delay only.
Full-Scale Range	Options (600 mV_{P-P} or 820 mV_{P-P}) selected with pin 14. Selected range applies to both channels.	Up to 512 step adjustments over a nominal range of 560 mV to 840 mV in the Full-Scale Voltage Adjust Register (3h; bits-7 thru 15).
Input Offset Adjust	Not possible	Up to ±45 mV adjustments in 512 steps in the Offset Adjust Register (2h; bits-7 thru 15).
Sampling Clock Phase Adjustment	The Clock Phase is adjusted automatically	The clock phase can be adjusted manually through the Fine & Coarse registers (Dh and Eh).
Test Pattern	Not Possible	A test pattern can be made present at the data outputs by selecting TPO in the Test Pattern Register (Fh; bit-11).
Resistor Trim Disable	Not possible	The DCLK outputs will continuously be present when RTD is selected in the Configuration Register (1h; bit-13)

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The default state of the Extended Control Mode is set upon power-on reset (internally performed by the device) and is shown in Table 3.

Table 3. Extended Control Mode Operation (Pin 14 Floating)

Feature	Extended Control Mode Default State
SDR or DDR Clocking	DDR Clocking
DDR Clock Phase	Data changes with DCLK edge (0° phase)
LVDS Output Amplitude	Normal amplitude ($710\ mV_{P-P}$)
Calibration Delay	Short Delay
Full-Scale Range	700 mV nominal for both channels
Input Offset Adjust	No adjustment for either channel
Resistor Trim Disable	Trim enabled, DCLK not continuously present at output
Test Pattern	Not present at output

THE SERIAL INTERFACE

NOTE

During the initial write using the serial interface, all six registers must be written with desired or default values. Subsequent writes to single registers are allowed.

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$). Eight write only registers are accessible through this serial interface. Registers are write only and can not be read back.

$\overline{SCS}$: This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK: Serial data input is accepted at the rising edge of this signal. There is no minimum frequency requirement for SCLK.

SDATA: Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. SeeFigure 9.

Each Register access consists of 32 bits, as shown in Figure 9 of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a "0" is loaded first. These 12 bits form the header. The next 4 bits are the address of the register that is to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in Table 4.

Refer to the REGISTER DESCRIPTION for information on the data to be written to the registers.

Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

NOTE

The Serial Interface should not be accessed when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

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Table 4. Register Addresses

4-Bit Address					
Loading Sequence: A3 loaded after Fixed Header Pattern, A0 loaded last					
A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0h	Reserved
0	0	0	1	1h	Configuration
0	0	1	0	2h	Offset
0	0	1	1	3h	Full-Scale Voltage Adjust
0	1	0	0	4h	Reserved
0	1	0	1	5h	Reserved
0	1	1	0	6h	Reserved
0	1	1	1	7h	Reserved
1	0	0	0	8h	Reserved
1	0	0	1	9h	Reserved
1	0	1	0	Ah	Reserved
1	0	1	1	Bh	Reserved
1	1	0	0	Ch	Reserved
1	1	0	1	Dh	Extended Clock Phase adjust fine
1	1	1	0	Eh	Extended Clock Phase adjust coarse
1	1	1	1	Fh	Test Pattern

REGISTER DESCRIPTION

Eight write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Normal Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit.

Table 5. Configuration Register

Addr: 1h (0001b)	**W only (0x92FF)**

D15	D14	D13	D12	D11	D10	D9	D8
1	DRE	RTD	DCS	DCP	nDE	OV	OE

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	Must be set to 1b
Bit 14	DRE: Differential Reset Enable. When this bit is set to 0b , it enables the single-ended DCLK_RST input. When this bit is set to 1b , it enables the differential DCLK_RST input.
	POR State: 0b
Bit 13	RTD: Resistor Trim Disable. When this bit is set to 1b, the input termination resistor is not trimmed during the calibration cycle and the DCLK output remains enabled. Note that the ADC is calibrated regardless of this setting.
	POR State: 0b
Bit 12	DCS: Duty Cycle Stabilizer. When this bit is set to 1b , a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disabled.
	POR State: 1b

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Bit 11	DCP: DDR Clock Phase. This bit only has an effect in the DDR mode. When this bit is set to 0b, the DCLK edges are time-aligned with the data bus edges ("0° Phase"). When this bit is set to 1b, the DCLK edges are placed in the middle of the data bit-cells ("90° Phase"), using the one-half speed DCLK shown in Figure 4 as the phase reference.
	POR State: 0b
Bit 10	nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Dual Data Rate) mode whereby a data word is output with each rising and falling edge of DCLK. When the device is in DDR mode, address 1h, bit-8 must be set to 0b. When this bit is set to a 1b, data bus clocking follows the SDR (single data rate) mode whereby each data word is output with either the rising or falling edge of DCLK , as determined by the OutEdge bit.
	POR State: 0b
Bit 9	OV: Output Voltage. This bit determines the LVDS outputs' voltage amplitude and has the same function as the OutV pin that is used in the normal control mode. When this bit is set to 1b, the standard output amplitude of 680 mV_{P-P} is used. When this bit is set to 0b, the reduced output amplitude of 520 mV_{P-P} is used.
	POR State: 1b
Bit 8	OE: Output Edge. This bit has two functions. When the device is in SDR mode, this bit selects the DCLK edge with which the data words transition and has the same effect as the OutEdge pin in the normal control mode. When this bit is set to 1b, the data outputs change with the rising edge of DCLK+. When this bit is set to 0b, the data output changes with the falling edge of DCLK+. When the device is in DDR mode, this bit must be set to 0b.
	POR State: 0b
Bits 7:0	Must be set to 1b

Table 6. Offset Adjust

Addr: 2h (0010b)	**W only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)		Offset Value					(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8	Offset Value. The input offset of the ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.
	POR State: 0000 0000 b (no adjustment)
Bit 7	Sign bit. 0b gives positive offset, 1b gives negative offset.
	POR State: 0b
Bit 6:0	Must be set to 1b

Table 7. Full-Scale Voltage Adjust

Addr: 3h (0011b)	**W only (0x807F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Adjust Value						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

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Bit 15:7	Full Scale Voltage Adjust Value. The input full-scale voltage or gain of the ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV_{P-P} differential value.	
	0000 0000 0	560mV_{P-P}
	1000 0000 0 Default Value	700mV_{P-P}
	1111 1111 1	840mV_{P-P}
	For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.	
	POR State: 1000 0000 0b	
Bits 6:0	Must be set to 1b	

Table 8. Extended Clock Phase Adjust Fine

Addr: Dh (1101b)	**W only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	FAM						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7	Fine Adjust Magnitude. With all bits set, total adjust = 110ps of non-linear clock adjust. Refer to Manual Sample Clock Phase Adjust.
	POR State: 000 0000 0b
Bit 6:0	Must be set to 1b

Table 9. Extended Clock Phase Adjust Coarse

Addr: Eh (1110b)	**W only (0x03FF)**

D15	D14	D13	D12	D11	D10	D9	D8
ENA	CAM				LFS	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	ENAble Clock Phase Adjust, default is 0b. RTD bit **MUST** also be set to ensure proper On Command Calibration with Clock Phase Adjust enabled.
Bit 14:11	Coarse Adjust Magnitude. Each LSB results in approximately 70ps of clock adjust. Refer to Manual Sample Clock Phase Adjust.
	POR State: 0000b
Bit 10	Low Frequency Sample clock. When this bit is set 1b, the dynamic performance of the device is improved when the sample clock is less than 900MHz.
	POR State: 0b
Bits 9:0	Must be set to 1b

Table 10. Test Pattern Register

Addr: Fh (1111b)	**W only (0xF7FF)**

D15	D14	D13	D12	D11	D10	D9	D8
1	1	1	1	TPO	1	1	1

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D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bits 15:12	Must be set to 1b
Bit 11	TPO: Test Pattern Output enable. When this bit is set 1b, the ADC is disengaged and a test pattern generator is connected to the outputs including OR. This test pattern will work with the device in the SDR and DDR modes.
	POR State: 0b
Bit 10:0	Must be set to 1b

Note Regarding Extended Mode Offset Correction

When using the Offset Adjust register, the following information should be noted.

For offset values of +0000 0000 and -0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the Figure below.

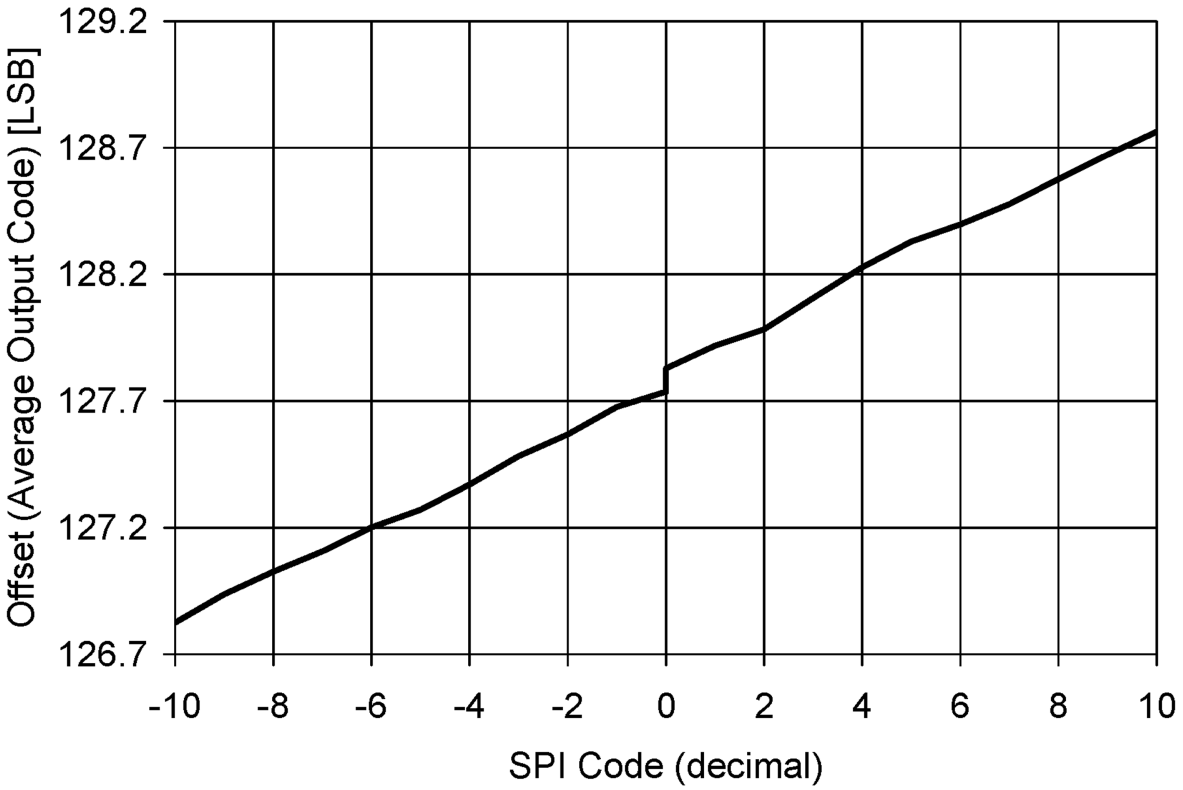


Figure 35. Extended Mode Offset Behavior

MULTIPLE ADC SYNCHRONIZATION

The ADC083000 has the capability to precisely reset its sampling clock (CLK) to synchronize its output clock (DCLK) and data with multiple ADCs in a system. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that they all use for sampling.

The ADC083000 has been designed to accommodate systems which require a single-ended (LVCMOS) DCLK_RST or a differential (LVDS) DCLK_RST.

Single-Ended (LVCMOS) DCLK_RST: The Power on Reset state of DCLK_RST is to have single-ended DCLK_RST activated. Bit 14, (DRE) in the Configuration Register is asserted low, 0b. When not using singled-ended DCLK_RST, the input should be grounded.

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Differential (LVDS) DCLK_RST: Activated by asserting bit 14, (DRE) in the configuration register high, 1b. When the differential DCLK_RST is not activated, the inputs should be grounded. Differential DCLK_RST has an internal 100 ohm termination resistor and should not be AC coupled.

The DCLK_RST signal must observe some timing requirements that are shown in Figure 5, Figure 6 and Figure 7 of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These times are specified in the AC Electrical Characteristics Table.

The DCLK_RST signal can be asserted asynchronous to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state. The state in which DCLK is held during the reset period is determined by the mode of operation (SDR/DDR) and the setting of the Output Edge configuration pin or bit. (Refer to Figure 5, Figure 6 and Figure 7 for the DCLK reset state conditions). Therefore, depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted in synchronization with the CLK rising edge, the next CLK falling edge synchronizes the DCLK output with those of other ADC083000s in the system. The DCLK output is enabled again after a constant delay (relative to the input clock frequency) which is equal to the CLK input to DCLK output delay (t_{SD}). The device always exhibits this delay characteristic in normal operation.

If the device is not programmed to allow DCLK to run continuously, DCLK will become inactive during a calibration cycle. Therefore, it is strongly recommended that DCLK only be used as a data capture clock and not as a system clock.

The DCLK_RST pin should NOT be brought high while the calibration process is running (while CalRun is high). Doing so could cause a digital glitch in the digital circuitry, resulting in corruption and invalidation of the calibration.

ADC TEST PATTERN

To aid in system debug, the ADC083000 has the capability of providing a test pattern at the four output ports completely independent of the input signal. The test pattern is selected by setting bit-11 (TPO) in the Test Pattern Register (address Fh). The test pattern will appear at the digital output about 10 DCLK cycles after the last write to the Test Pattern Register.

The ADC is disengaged and a test pattern generator is connected to the outputs including OR. Each port is given a unique 8-bit word, alternating between 1's and 0's as described in theTable 11.

Table 11. Test Pattern by Output Port(1)

Time	Da	Db	Dc	Dd	OR	Comments
T0	01h	02h	03h	04h	0	Pattern Sequence n
T1	FEh	FDh	FCh	FBh	1	
T2	01h	02h	03h	04h	0	
T3	FEh	FDh	FCh	FBh	1	
T4	01h	02h	03h	04h	0	
T5	01h	02h	03h	04h	0	Pattern Sequence n+1
T6	FEh	FDh	FCh	FBh	1	
T7	01h	02h	03h	04h	0	
T8	FEh	FDh	FCh	FBh	1	
T9	01h	02h	03h	04h	0	
T10	01h	02h	03h	04h	0	Pattern Sequence n+2
T11	...	...	...	...	...	

(1) The same bit pattern repeats when the test pattern sequence is concatenated.

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APPLICATIONS INFORMATION

THE REFERENCE VOLTAGE

The voltage reference for the ADC083000 is derived from a 1.254V bandgap reference, a buffered version of which is made available at pin 31, V_{BG}, for user convenience. This output has an output current capability of ±100 µA. This reference voltage should be buffered if more current is required.

The internal bandgap-derived reference voltage has a nominal value of 600 mV or 820 mV, as determined by the FSR pin and described in The Analog Inputs.

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be adjusted through a Configuration Register in the Extended Control mode, as explained in NORMAL/EXTENDED CONTROL.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output. These large signal excursions will also activate the OR output for the time that the signal is out of range. See Out Of Range (OR) Indication.

One extra feature of the V_{BG} pin is that it can be used to raise the common mode voltage level of the LVDS outputs. The output offset voltage (V_{OS}) is typically 800mV when the V_{BG} pin is used as an output or left unconnected. To raise the LVDS offset voltage to a typical value of 1150mV the V_{BG} pin can be connected directly to the supply rails.

THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. The full-scale input range is selected with the FSR pin to be 600 mV_{P-P} or 820 mV_{P-P}, or can be adjusted to values between 560 mV_{P-P} and 840 mV_{P-P} in the Extended Control mode through the Serial Interface. For best performance, it is recommended that the full-scale range be kept between 595 mV_{P-P} and 805 mV_{P-P} in the Extended Control mode because the internal DAC which sets the full-scale range is not as linear at the ends of its range.

Table 12 gives the input to output relationship with the FSR pin high when the normal (non-extended) mode is used. With the FSR pin grounded, the millivolt values in Table 12 are reduced to 75% of the values indicated. In the Enhanced Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

Table 12. DIFFERENTIAL INPUT TO OUTPUT RELATIONSHIP (Non-Extended Control Mode, FSR High)

V_{IN}+	V_{IN}−	Output Code
V_{CM} − 205mV	V_{CM} + 205mV	0000 0000
V_{CM} − 102.5 mV	V_{CM} + 102.5 mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 102.5 mV	V_{CM} −102.5 mV	1100 0000
V_{CM} + 205mV	V_{CM} − 205mV	1111 1111

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

The Input impedance of V_{IN+} / V_{IN-} in the d.c. coupled mode (V_{CMO} pin not grounded) consists of a precision 100Ω resistor across the inputs and a capacitance from each of these inputs to ground. In the a.c. coupled mode, the input appears the same except there is also a resistor of 50KΩ between each analog input pin and the on-chip V_{CMO} potential.

When the inputs are a.c. coupled, the V_{CMO} output *must* be grounded, as shown in Figure 36. This causes the on-chip V_{CMO} voltage to be connected to the inputs through on-chip 50KΩ resistors.

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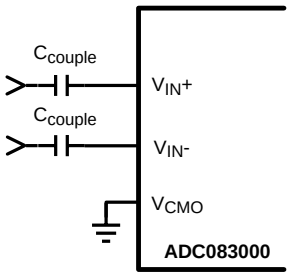


Figure 36. Differential Data Input Connection

When the d.c. coupled mode is used, a precise common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

Handling Single-Ended Input Signals

There is no provision for the ADC083000 to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC.

A.C. Coupled Input

The easiest way to accomplish single-ended a.c. input to differential a.c. signal is with an appropriate balun, as shown in Figure 37.

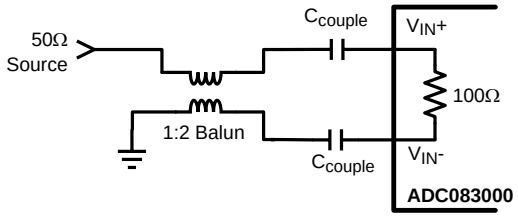


Figure 37. Single-Ended to Differential signal conversion with a balun

Figure 37 is a generic depiction of a single-ended to differential signal conversion using a balun. The circuitry specific to the balun will depend on the type of balun selected and the overall board layout. It is recommended that the system designer contact the manufacturer of the balun they have selected to aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

When selecting a balun, it is important to understand the input architecture of the ADC. There are specific balun parameters of which the system designer should be mindful. They should match the impedance of their analog source to the ADC083000's on-chip 100Ω differential input termination resistor. The range of this input termination resistor is described in the Converter Electrical Characteristics as the specification R_{IN}.

Also, as a result of the ADC architecture, the phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance should be no more than ±2.5° and the amplitude imbalance should be limited to less than 1dB at the desired input frequency range.

Finally, when selecting a balun, the VSWR (Voltage Standing Wave Ratio), bandwidth and insertion loss of the balun should also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss should be considered so that the signal at the balun output is within the specified input range of the ADC as described in the Converter Electrical Characteristics as the specification V_{IN}.

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D.C. Coupled Input

When d.c. coupling to the ADC083000 analog inputs is required, single-ended to differential conversion may be easily accomplished with the LMH6555. An example of this type of circuit is shown in Figure 38. In such applications, the LMH6555 performs the task of single-ended to differential conversion while delivering low distortion and noise, as well as output balance, that supports the operation of the ADC083000. Connecting the ADC083000 V_{CMO} pin to the V_{CM_REF} pin of the LMH6555, through an appropriate buffer, will ensure that the common mode input voltage is as needed for optimum performance of the ADC083000. The LMV321 was chosen to buffer V_{CMO} for its low voltage operation and reasonable offset voltage.

Be sure that the current drawn from the V_{CMO} output does not exceed 100 µA.

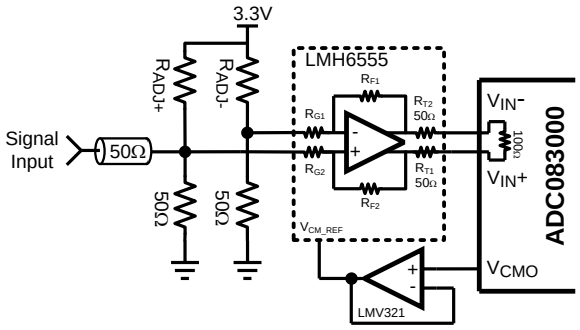


Figure 38. Example of Servoing the Analog Input with V_{CMO}

In Figure 38, R_{ADJ-} and R_{ADJ+} are used to adjust the differential offset that can be measured at the ADC inputs V_{IN+} / V_{IN-}. An unadjusted positive offset with reference to V_{IN-} greater than |15mV| should be reduced with a resistor in the R_{ADJ-} position. Likewise, an unadjusted negative offset with reference to V_{IN-} greater than |15mV| should be reduced with a resistor in the R_{ADJ+} position. Table 13 gives suggested R_{ADJ-} and R_{ADJ+} values for various unadjusted differential offsets to bring the V_{IN+} / V_{IN-} offset back to within |15mV|.

Table 13. D.C. Coupled Offset Adjustment

Unadjusted Offset Reading	Resistor Value
0mV to 10mV	no resistor needed
11mV to 30mV	20.0kΩ
31mV to 50mV	10.0kΩ
51mV to 70mV	6.81kΩ
71mV to 90mV	4.75kΩ
91mV to 110mV	3.92kΩ

Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh. During a calibration cycle, the OR output is invalid. Refer to OVERVIEW for more details.

Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the ADC083000 is derived from an internal band-gap reference. In the normal mode, the FSR pin controls the effective reference voltage of the ADC083000 such that the differential full-scale input range at the analog inputs is 820 mV_{P-P} with the FSR pin high, or is 600 mV_{P-P} with FSR pin low. In the Extended Control Mode, the Full Scale Range can be set anywhere from 560mV to 840mV. Best SNR is obtained with higher Full Scale Ranges, but better distortion and SFDR are obtained with lower Full Scale Ranges. The LMH6555 of Figure 38 is suitable for any Full Scale Range.

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THE SAMPLE CLOCK INPUT

The ADC083000 has a differential LVDS clock input, CLK+ / CLK-, which must be driven with an a.c. coupled, differential clock signal. Although the ADC083000 is tested and its performance is specified with a differential 1.5 GHz clock, it typically will function well with input clock frequencies indicated in the Electrical Characteristics Table. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as indicated in Figure 39.

Operation up to the sample rates indicated in the Electrical Characteristics Table is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management . See Thermal Management.

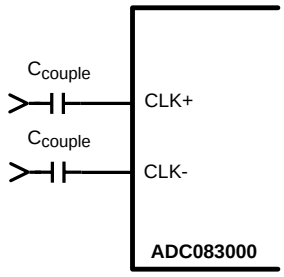


Figure 39. Differential Sample Clock Connection

The differential sample clock line pair should have a characteristic impedance of 100Ω and be terminated at the clock source in that (100Ω) characteristic impedance. The input clock line should be as short and as direct as possible. The ADC083000 clock input is internally terminated with an untrimmed 100Ω resistor.

Insufficient input clock levels will result in poor dynamic performance. Excessively high input clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the input clock level within the range specified in the Electrical Characteristics Table.

The low and high times of the input clock signal can affect the performance of any A/D Converter. The ADC083000 features a duty cycle clock correction circuit which can maintain performance over temperature. The ADC will meet its performance specification if the input clock high and low times are maintained as specified in the Electrical Characteristics Table.

High speed, high performance ADCs such as the ADC083000 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{INFSR}/V_{IN(P-P)}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input.

Note that the maximum jitter described above is the Route Sum Square, (RSS), of the jitter from all sources, including that in the ADC input clock, that added by the system to the ADC input clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added input clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

Input clock amplitudes above those specified in the Electrical Characteristics Table may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 128 when both input pins are at the same potential.

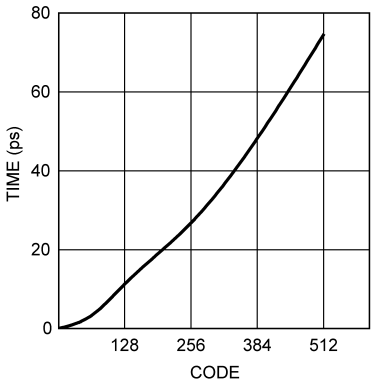
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Manual Sample Clock Phase Adjust

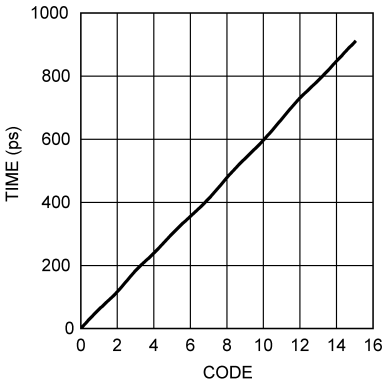
The sample clock phase can be manually adjusted in the Extended Control Mode to accommodate subtle layout differences when synchronizing multiple ADCs. Register addresses Dh and Eh provide extended mode access to fine and coarse adjustments. Use of Low Frequency Sample Clock control, (register Eh; bit-10) is not supported while using manual sample clock phase adjustments.

It should be noted that by just enabling the phase adjust capability (register Eh; bit-15), degradation of dynamic performance is expected, specifically SFDR. It is intended that very small adjustments are used. Larger increases in phase adjustments will begin to affect SNR and ultimately ENOB. Therefore, the use of coarse phase adjustment should be minimized in favor of better system design.

Fine Clock Phase Adjust Range



Coarse Clock Phase Adjust Range



CONTROL PINS

Six control pins (without the use of the serial interface) provide a wide range of possibilities in the operation of the ADC083000 and facilitate its use. These control pins provide Full-Scale Input Range setting, Calibration, Calibration Delay, Output Edge Synchronization choice, LVDS Output Level choice and a Power Down feature.

Full-Scale Input Range Setting

The input full-scale range can be selected to be either 600 mV_{P-P} or 820 mV_{P-P}, as selected with the FSR control input (pin 14) in the Normal Mode of operation. In the Extended Control Mode, the input full-scale range may be set to be anywhere from 560 mV_{P-P} to 840 mV_{P-P}. See THE ANALOG INPUT for more information.

Calibration

The ADC083000 calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is an input clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress. Note that the DCLK outputs are not active during a calibration cycle, therefore it is not recommended as a system clock.

Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly, as described in the Calibration Delay Section, below.

The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The ADC083000 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See On-Command Calibration.

The internal power-on calibration circuitry comes up in an unknown logic state. If the input clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 25 mW. The power consumption will be normal after the clock starts.

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On-Command Calibration

To initiate an on-command calibration, bring the CAL pin high for a minimum of 80 input clock cycles after it has been low for a minimum of 80 input clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of 80 input clock cycles, then brought high for a minimum of another 80 input clock cycles. The calibration cycle will begin 80 input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed.

The minimum 80 input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in OVERVIEW for best performance, a calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly relative to the specific system design performance requirements. ENOB changes slightly with increasing junction temperature and can be easily corrected by performing an on-command calibration.

Considerations for a continuous DCLK and proper CalRun operation:

- During a Power-On calibration cycle, both the ADC and the input termination resistor are calibrated. Because dynamic performance changes slightly with junction temperature, an On-Command calibration can be executed to bring the performance of the ADC in line. By default, On-Command calibration includes calibrating the input termination resistance and the ADC. However, since the input termination resistance changes only marginally with temperature, the user has the option to disable the input termination resistor trim (address: 1h, bit: 13, set to 1b), which will specify that the DCLK is continuously present at the output during calibration. The Resistor Trim Disable can be programmed in the Configuration Register (address: 1h, bit 13) when in the Extended Control mode. Refer to REGISTER DESCRIPTION for register programming information.
- When an on-command calibration is requested while using the Aperture Adjust Circuitry through the Extended Control Mode registers, we recommend that the Resistor Trim Disable bit be set (address: 1h, bit: 13, set to 1b). This allows continuous operation of all clocks in the ADC including DCLK and proper operation of the CalRun output. The Aperture Adjust Circuitry control is resident in the Extended Control Mode registers (addresses: Dh and Eh). Refer to REGISTER DESCRIPTION for register programming information.

Calibration Delay

The CalDly input (pin 127) is used to select one of two delay times after the application of power to the start of calibration, as described in Calibration. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration would begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

Note that the calibration delay selection is not possible in the Extended Control mode and the short delay time is used.

Output Edge Synchronization

DCLK signals are available to help latch the converter output data into external circuitry. The output data can be synchronized with either edge of these DCLK signals. That is, the output data transition can be set to occur with either the rising edge or the falling edge of the DCLK signal, so that either edge of that DCLK signal can be used to latch the output data into the receiving circuit.

When OutEdge (pin 4) is high, the output data is synchronized with (changes with) the rising edge of the DCLK+ (pin 82). When OutEdge is low, the output data is synchronized with the falling edge of DCLK+.

At the very high speeds of which the ADC083000 is capable, slight differences in the lengths of the DCLK and data lines can mean the difference between successful and erroneous data capture. The OutEdge pin is used to capture data on the DCLK edge that best suits the application circuit and layout.

LVDS Output Level Control

The output level can be set to one of two levels with OutV (pin3). The strength of the output drivers is greater with OutV high. With OutV low there is less power consumption in the output drivers, but the lower output level means decreased noise immunity.

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For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low. If the LVDS lines are long and/or the system in which the ADC083000 is used is noisy, it may be necessary to tie the OutV pin high.

Power Down Feature

The Power Down pin (PD) allows the ADC083000 to be entirely powered down. See Power Down for details on the power down feature.

The digital data (+/-) output pins are put into a high impedance state when the PD pin for the respective channel is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

THE DIGITAL OUTPUTS

The ADC083000 demultiplexes the output data of each of the two ADCs on the die onto two LVDS output buses (total of four buses, two for each ADC). For each of the two converters, the results of successive conversions start on the falling edges of the CLK+ pin and are available on one of the two LVDS buses. The results of conversions that start on the rising edges of the CLK+ pin are available on the other LVDS bus. This means that the word rate at each LVDS bus is 1/2 the ADC083000 input clock rate and the two buses must be multiplexed to obtain the entire 3 GSPS conversion result.

Since the minimum recommended input clock rate for this device is 500 MHz, the sampling rate can be reduced to as low as 1 GSPS by using the results available on all four LVDS busses. The effective sampling rate can be reduced to as low as 250 MSPS by decimating the data by using one bus and a 500MHz clock.

There is one LVDS output clock pair (DCLK+/-) available for use to latch the LVDS outputs on all buses. Whether the data is sent at the rising or falling edge of DCLK is determined by the sense of the OutEdge pin, as described in Output Edge Synchronization.

DDR (Double Data Rate) clocking can also be used. In this mode a word of data is presented with each edge of DCLK, reducing the DCLK frequency to 1/4 the input clock frequency. When the device is in DDR mode, register address 1h, bit 8 must be set to 0b. See the Timing Diagram section for details.

The OutV pin is used to set the LVDS differential output levels. See LVDS Output Level Control.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}− will produce an output code of all ones, a full-scale input level with V_{IN}− positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}− are equal, the output code will be 128.

POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the ADC083000 should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the ADC083000. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

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Supply Voltage

The ADC083000 is specified to operate with a supply voltage of 1.9V ±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC083000 power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the ADC083000. The circuit of Figure 40 will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the ADC083000, unless a minimum load is provided for the supply. The 100Ω resistor at the regulator output of Figure 40 provides a minimum output current during power-up to ensure there is no turn-on spiking. Whether a linear or switching regulator is used, it is advisable to provide a slow start circuit to prevent overshoot of the supply.

In the circuit of Figure 40, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V . If a 3.3V supply is used, an LM1086 linear regulator is recommended.

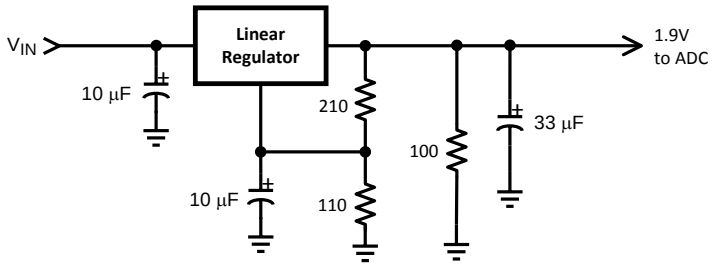


Figure 40. Non-Spiking Power Supply

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in the Operating Ratings table. This voltage should not exceed the V_A supply voltage and should never spike to a voltage greater than (V_A + 100mV).

If the power is applied to the device without an input clock signal present, the current drawn by the device might be below 200 mA. This is because the ADC083000 gets reset through clocked logic and its initial state is unknown. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the input clock is established.

Thermal Management

The ADC083000 is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 130°C. That is, T_A (ambient temperature) plus ADC power consumption times θ_{JA} (junction to ambient thermal resistance) should not exceed 130°C. This is not a problem if the ambient temperature is kept to a maximum of +85°C as specified in the Operating Ratings section and the exposed pad on the bottom of the package is thermally connected to a large enough copper area of the PC board.

Please note that the following are general recommendations for mounting exposed pad devices onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting.

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The package of the ADC083000 has an exposed pad on its back that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional HLQFP, but the exposed pad must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The exposed pad of the device must be soldered down to ensure adequate heat conduction out of the package. The land pattern for this exposed pad should be at least as large as the 5 x 5 mm of the exposed pad of the package and be located such that the exposed pad of the device is entirely over that thermal land pattern. This thermal land pattern should be electrically connected to ground. A clearance of at least 0.5 mm should separate this land pattern from the mounting pads for the package pins.

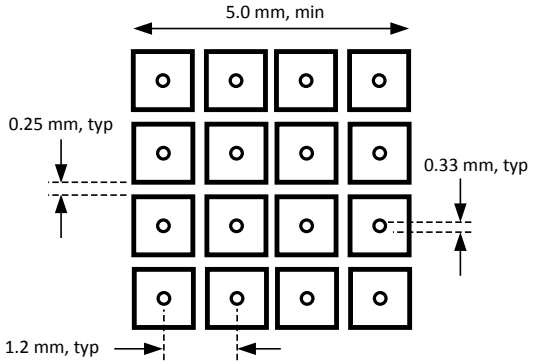


Figure 41. Recommended Package Land Pattern

Since a large aperture opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the land pattern of Figure 41.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area of about 2 square inches (6.5 square cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended.

The thermal vias should be placed on a 1.2 mm grid spacing and have a diameter of 0.30 to 0.33 mm. These vias should be barrel plated to avoid solder wicking into the vias during the soldering process as this wicking could cause voids in the solder between the package exposed pad and the thermal land on the PCB. Such voids could increase the thermal resistance between the device and the thermal land on the board, which would cause the device to run hotter.

If it is desired to monitor die temperature, a temperature sensor may be mounted on the heat sink area of the board near the thermal vias. Allow for a thermal gradient between the temperature sensor and the ADC083000 die of $\theta_{J\text{-}PAD}$ times typical power consumption = 2.8 x 1.9 = 5.3°C. Allowing for 6.3°C, including some margin for temperature drop from the pad to the temperature sensor, then, would mean that maintaining a maximum pad temperature reading of 123.7°C will ensure that the die temperature does not exceed 130°C, assuming that the exposed pad of the ADC083000 is properly soldered down and the thermal vias are adequate. (The inaccuracy of the temperature sensor is additional to the above calculation).

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single ground plane should be used, instead of splitting the ground plane into analog and digital areas.

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Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the ADC083000. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

DYNAMIC PERFORMANCE

The ADC083000 is a.c. tested and its dynamic performance is specified. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in THE SAMPLE CLOCK INPUT.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the input clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is a lower impedance than offered by the package pins.

USING THE SERIAL INTERFACE

The ADC083000 may be operated in the non-extended control (non-Serial Interface) mode or in the extended control mode. Table 14 and Table 15 describe the functions of pins 3, 4, 14 and 127 in the non-extended control mode and the extended control mode, respectively.

Non-Extended Control Mode Operation

Non-extended control mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. That is, the output voltage, full-scale range and output edge selections are all controlled with pin settings. The non-extended control mode is used by setting pin 14 high or low, as opposed to letting it float. Table 14 indicates the pin functions of the ADC083000 in the non-extended control mode.

Table 14. Non-Extended Control Mode Operation (Pin 14 High or Low)

Pin	Low	High	Floating
3	0.52 V_{P-P} Output	0.68 V_{P-P} Output	n/a
4	OutEdge = Neg	OutEdge = Pos	DDR
14	600 mV_{P-P} input range	820 mV_{P-P} input range	Extended Control Mode
127	CalDly Low	CalDly High	Serial Interface Enable

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Pin 3 can be either high or low in the non-extended control mode. Pin 14 must not be left floating to select this mode. See NORMAL/EXTENDED CONTROL for more information.

Pin 4 can be high or low or can be left floating in the non-extended control mode. In the non-extended control mode, pin 4 high or low defines the edge at which the output data transitions. See NORMAL/EXTENDED CONTROL for more information. If this pin is floating, the output clock (DCLK) is a DDR (Double Data Rate) clock (see Double Data Rate) and the output edge synchronization is irrelevant since data is clocked out on both DCLK edges.

Pin 127, if it is high or low in the non-extended control mode, sets the calibration delay. If pin 127 is floating, the calibration delay is the same as it would be with this pin low and this pin acts as the enable pin for the serial interface input.

Table 15. Extended Control Mode Operation (Pin 14 Floating)

Pin	Function
3	SCLK (Serial Clock)
4	SDATA (Serial Data)
127	$\overline{SCS}$ (Serial Interface Chip Select)

COMMON APPLICATION PITFALLS

Failure to write all register locations when using extended control mode. When using the serial interface, all six address locations must be written at least once with the default or desired values before calibration and subsequent use of the ADC.

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the ADC083000. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode. As discussed in The Analog Inputs and THE ANALOG INPUT, the Input common mode voltage must remain within 50 mV of the V_{CMO} output , which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO} .

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC083000 as many high speed amplifiers will have higher distortion than will the ADC083000, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage. As mentioned in THE REFERENCE VOLTAGE, the reference voltage is intended to be fixed to provide one of two different full-scale values (600 mV_{P-P} and 820 mV_{P-P}). Over driving this pin will not change the full scale value, but can be used to change the LVDS common mode voltage from 0.8V to 1.2V by tying the V_{BG} pin to V_A.

Driving the clock input with an excessively high level signal. The ADC input clock level should not exceed the level described in the Operating Ratings Table or the input offset could change.

Inadequate input clock levels. As described in THE SAMPLE CLOCK INPUT, insufficient input clock levels can result in poor performance. Excessive input clock levels could result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in Thermal Management, it is important to provide adequate heat removal to ensure device reliability. This can be done either with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC083000CIYB/NOPB	ACTIVE	HLQFP	NNB	128	60	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	ADC083000CIYB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

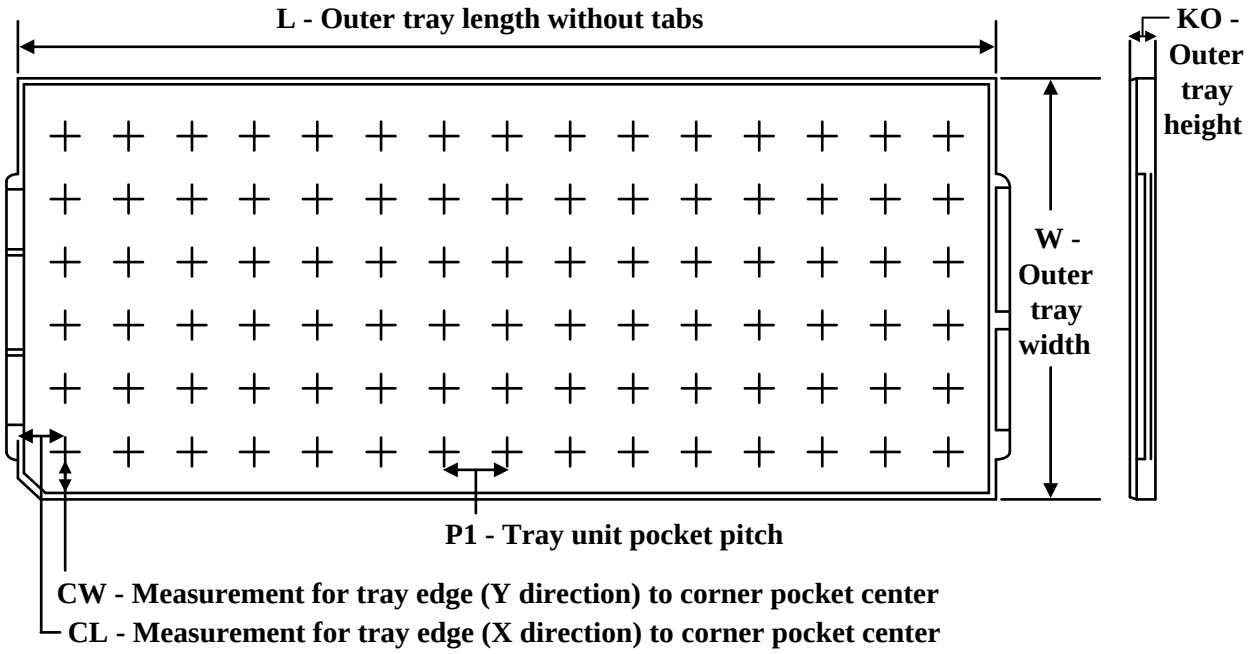
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TRAY

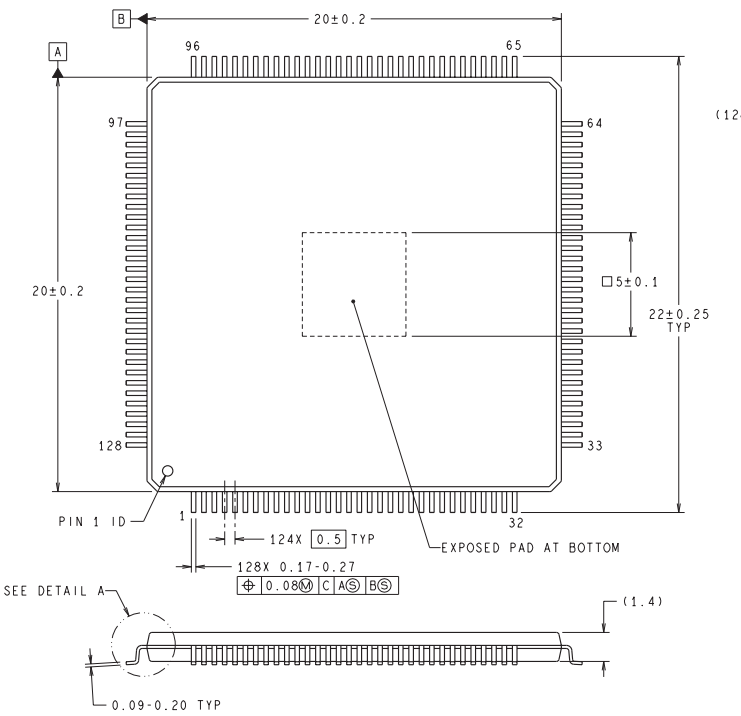


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

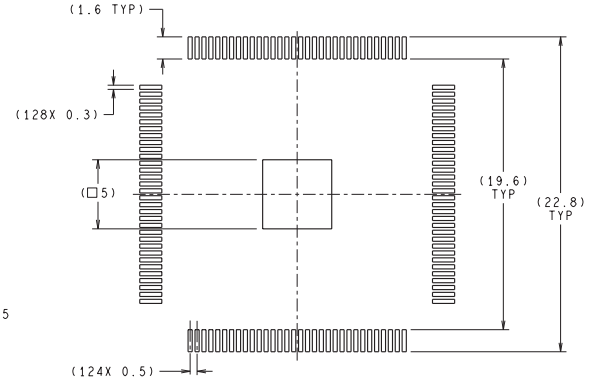
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC083000CIYB/NOPB	NNB	HLQFP	128	60	5 X 12	150	322.6	135.9	7620	25.4	17.8	17.55

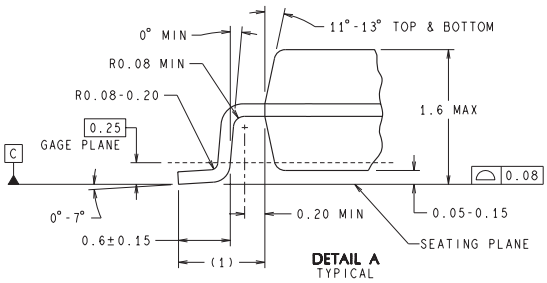
NNB0128A



DIMENSIONS ARE IN MILLIMETERS



RECOMMENDED LAND PATTERN



DETAIL A
TYPICAL

VNX128A (Rev B)

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