LX7309

Advanced Multi-topology Current-Mode Controller

Production Datasheet

Description

The LX7309 is a versatile current-mode DC-DC controller for isolated/non-isolated topologies. It features a low-resistance current-sensing scheme for max 200mV drop, using a differential current-sense amplifier for Kelvin connectivity and low noise pickup.

The LX7309 provides an out-of-phase drive signal for driving a synchronous rectifier or an active clamp. Duty cycle is limited to 50%, which is helpful in implementing a high-power Forward converter topology. It also helps avoid subharmonic instability without requiring slope compensation. The IC has differential voltage sensing for implementing topologies with power-ground separated from IC ground. The switching frequency can be set from 100-500 kHz, externally synchronizable up to 1MHz. It has a programmable UVLO threshold, Power Fail Warning (PFW), and a programmable Low Power (pulse-skip) Mode for better light-load efficiency.

Features

- Current-mode control for fast line and load correction responses
- 50% duty cycle limit for simple Forward converters and for avoiding subharmonic instability in Flyback, Boost and Buck-Boost
- 200mV peak current sense signal with differential Kelvin sensing for noise immunity and higher efficiency
- Two out-of-phase driver stages for synchronous rectification or active clamp
- ROHS-compliant, 24-pin, 4x4 mm QFN

Applications

- Isolated and Non-isolated topologies
- Buck, Boost, Buck-boost, Forward, Flyback
- PoE PD applications

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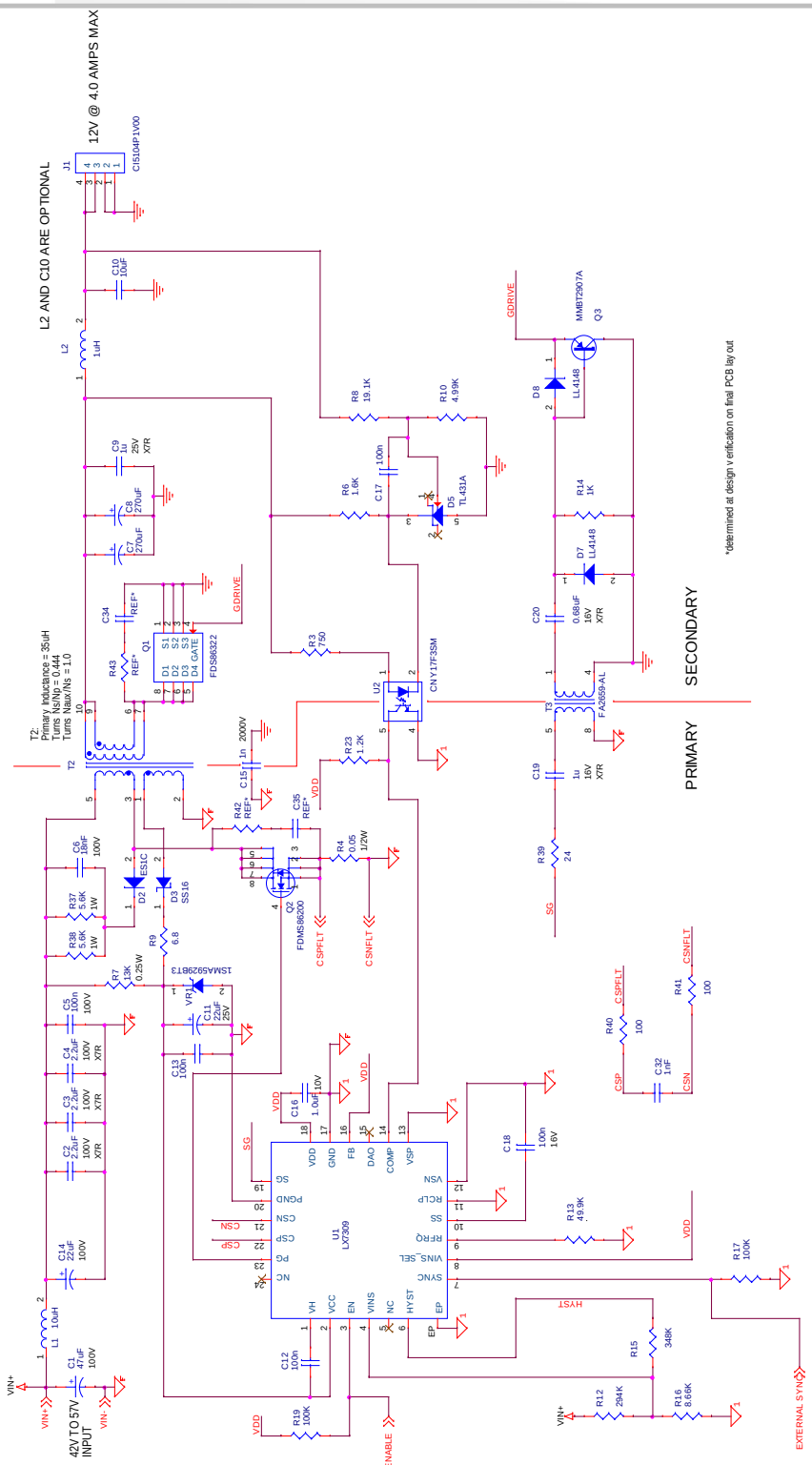


Figure 1: 12V/4A Output Isolated fly-back with Secondary Synchronous Rectification

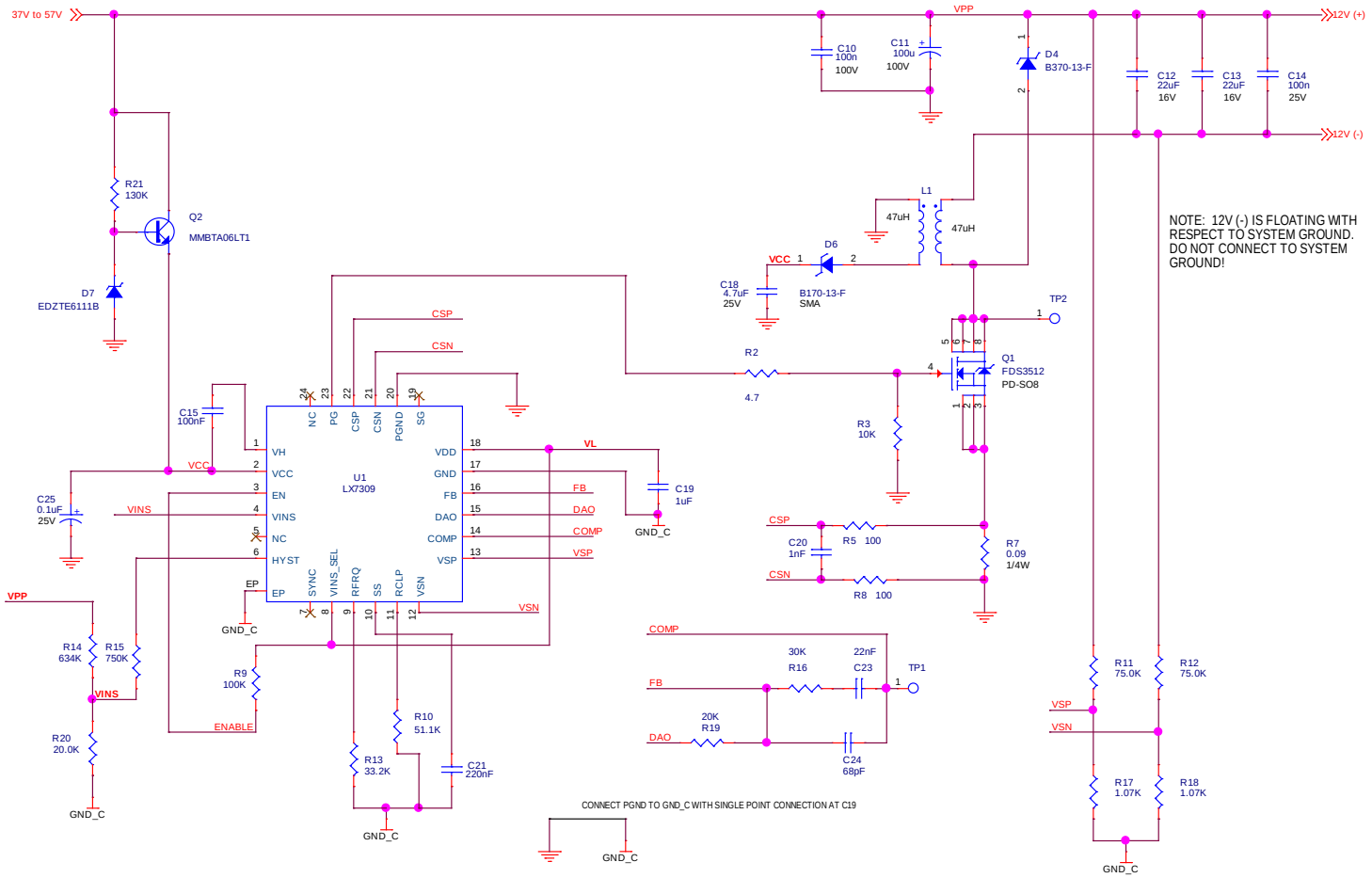
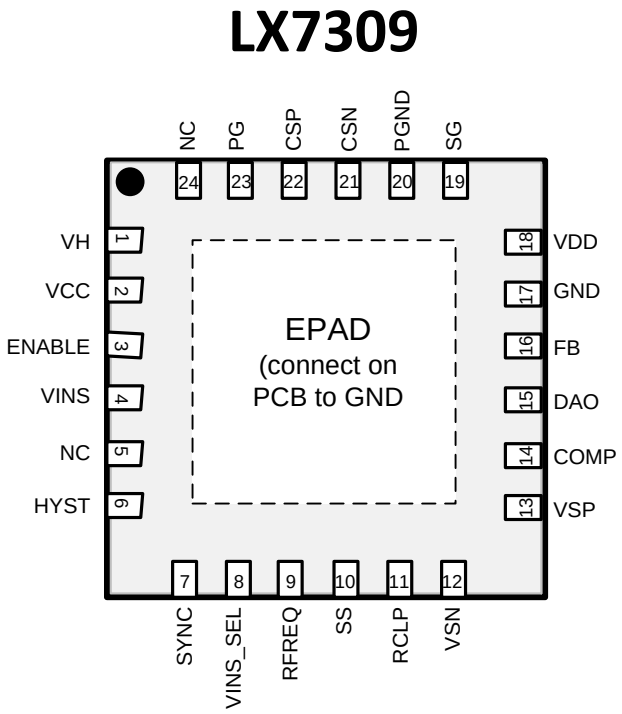


Figure 2: 12V/22W Non-Isolated Buck

Pin Configuration



TOP VIEW
(4x4 QFN – 24)

Figure 3: Pinout

Ordering Information

Ambient Temperature	Type	Package	Part Number	Package Type
-40°C to 85°C	RoHS compliant, Pb-free	QFN-24 (4mm × 4 mm, 0.5mm pitch)	LX7309ILQ	Bulk
			LX7309ILQ-TR	Tape and Reel

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Pin Description (LX7309)

<table>
<tr><th>Pin Number</th><th>Designator</th><th>Description</th></tr>
<tr><td>1</td><td>VH</td><td>Internal rail of -5V with respect to VCC, brought out for decoupling purposes. Connect a 0.1µF ceramic cap very close from this pin to VCC pin.</td></tr>
<tr><td>2</td><td>VCC</td><td>Supply pin of the IC. Provide up to 10mA startup bias current to start PWM switching after UVLO (9.5V max) is reached. Standby current may be lowered using one of the methods outlined on page 25.</td></tr>
<tr><td>3</td><td>ENABLE</td><td>Logic-level input to enable/disable the converter. Connect to Pin 17 GND to disable switching in the LX7309. May be pulled high with a 100k resistor connected to VDD.</td></tr>
<tr><td>4</td><td>VINS</td><td>Input for Power Fail Warning (PFW) or VPP UVLO, depending on state of VINS_SEL pin. The following table describes VINS pin function:
<table>
<tr><th colspan="3">VINS Pin Function</th></tr>
<tr><th>VINS_SEL</th><th>VINS</th><th>Function</th></tr>
<tr><td>VIN_SEL = VDD</td><td>VINS < 1.2V</td><td>VPP UVLO Mode. LX7309 switching is disabled; standby current will be drawn by VCC Pin.</td></tr>
<tr><td>VIN_SEL = VDD</td><td>VINS ≥ 1.2V</td><td>VPP UVLO Mode. LX7309 switching is enabled; full operation current will be drawn by VCC pin.</td></tr>
<tr><td>VIN_SEL = Pin 17 Ground</td><td>VINS < 1.2V</td><td>Power Fail Warning (PFW) Mode. HYST pin is low, indicating VPP power failure. LX7309 switching is enabled.</td></tr>
<tr><td>VIN_SEL = Pin 17 Ground</td><td>VINS ≥ 1.2V</td><td>Power Fail Warning (PFW) Mode. HYST pin is high, indicating VPP power OK. LX7309 switching is enabled.</td></tr>
</table></td></tr>
<tr><td>5</td><td>NC</td><td>No connection internally.</td></tr>
<tr><td>6</td><td>HYST</td><td>Output of the UVLO comparator as shown in Fig. 6 (Block Diagram). In VPP UVLO Mode, a resistor between this pin and VINS programs the rising and falling thresholds of the UVLO. The state of this pin is monitored for Power Fail Warning.</td></tr>
<tr><td>7</td><td>SYNC</td><td>Used to synchronize the LX7309 to a frequency higher than its default value as set on RFREQ pin. The synchronizing clock must be 2x the desired sync frequency, with a maximum synchronizing clock frequency of 1MHz (for 500kHz PWM frequency). The PG pin's rising edge will occur at the same instant as the rising edge of the clock being applied on the SYNC pin.</td></tr>
</table>

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8	**VINS_SEL**	Logic-level pin to select VPP UVLO Mode or Power Fail Warning Mode. See the function description for Pin 4 VINS for further details.
9	**RFREQ**	Connect a programming resistor from this pin to Pin 17 GND to set the switching frequency. A typical value of the programming resistor is 50k (49.9k), and this value will provide a frequency between 200 to 250 kHz. Halving it will roughly double the frequency, whereas doubling it will halve the frequency. Note that the LX7309 is designed to operate from 100kHz to 500 kHz. The switching frequency is approximated by: $Freq(kHz) \approx 10^7/RFREQ$
10	**SS**	Soft Start Pin. A capacitor between this pin and Pin 17 GND controls the rate of soft start during power-up, and provides the recovery period during over-current hiccup mode. Do not leave this pin float even if the soft start function is provided by alternate circuitry. It is advised to place a 0.1uF cap to ground on this pin; however the actual capacitor used will be determined by the application. The soft start period can be approximated by: $Tss \approx Css \times RFREQ$ Hiccup Mode recovery period time will be 10 X the soft start period.
11	**RCLP**	Low power clamp resistor. Connect a resistor from this pin to Pin 17 GND to set the level at which pulse-skipping mode is entered at light loads. Connecting this pin directly to Pin 17 GND, will limit the pulse skip to comp pin voltages of 200mV or less; this effectively disables the pulse skip for most applications. The method to select the threshold (and RCLP resistor value) is described in the Applications Information section of this datasheet.
12	**VSN**	Negative input of the internal differential-sense voltage amplifier. Used for differential sensing of the output voltage in non-isolated applications where output ground is separated from IC ground.
13	**VSP**	Positive input of the internal differential-sense voltage amplifier. Used for differential sensing of the output voltage in non-isolated applications where output ground is separated from IC ground.
14	**COMP**	Output of the internal error amplifier, and the input of the PWM comparator. May be bypassed by an external source, such as an optoisolator output with a pullup resistor to VDD.
15	**DAO**	Output of the internal differential voltage amplifier with a fixed gain of 7. For typical use connect DAO to the feedback pin (FB) as shown in Fig. 2.
16	**FB**	Error Amplifier feedback input. Voltages at this pin are compared to a 1.2V reference internally. If the internal error amplifier is not used and the COMP pin is being driven directly, the FB pin can be either tied high (to VDD), or connected to COMP.
17	**GND**	LX7309 signal ground. Connect GND and PGND together on a copper island on the component side, and then connect that through several vias very close to the chip on to a large ground plane which extends up to the ground side of the current sense resistor.
18	**VDD**	Internal 5V supply output. At least a 1µF ceramic cap placed close to this pin, connected to IC ground is recommended for proper decoupling. This pin can also provide up to 5mA for external circuitry if required.
19	**SG**	Secondary Gate driver. Used to drive a synchronous FET or an active clamp FET. Maximum output voltage is VCC. On resistance is 10Ω for both high and low state. SG is the compliment of PG with a typical 110ns blanking time on both edges, to prevent cross-conduction. SG is held low in pulse-skip mode, and is also low during soft-start. SG pin does

		not support diode-emulation mode (discontinuous conduction mode). Leave floating if unused.
20	**PGND**	Power ground (for internal SG and PG drivers). This is best for VCC decoupling, and the Primary-side current sense resistor's lower terminal.
21	**CSN**	The negative input of the internal current-sense voltage amplifier. May be tied directly to PGND; however, to avoid noise from ground bounce, it is best to route this on the PCB in Kelvin manner to the ground side of the sense resistor to avoid noise related to layout.
22	**CSP**	The positive input of the internal current-sense voltage amplifier. The internal gain of the current sense amplifier is fixed at 5. 240mV between CSP and CSN will cause the PWM output to truncate pulses for current limiting. 360mV between CSP and CSN will trigger hiccup mode.
23	**PG**	Primary FET Gate driver. Maximum output voltage is VCC. On resistance is 10Ω for high state and 5Ω for low state.
24	**NC**	Not connected.
25	**EPAD**	Connect on PCB to GND (Pin 17)

Typical Performance Curves

(Supply Pin Current versus Pin Voltage, Frequency and Loading)

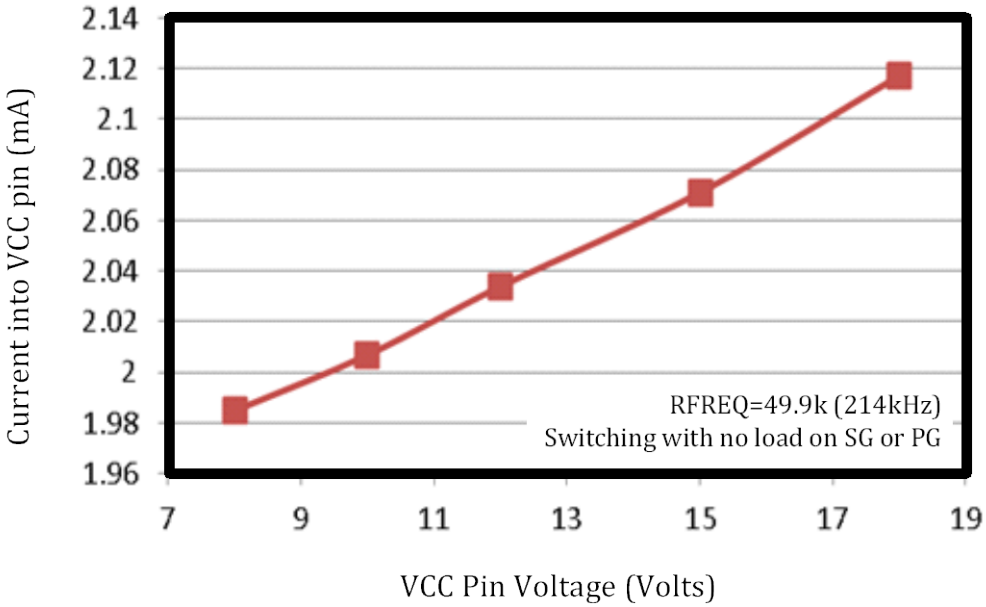

Figure 4: Supply Pin current as a function of its voltage (no load on drivers)

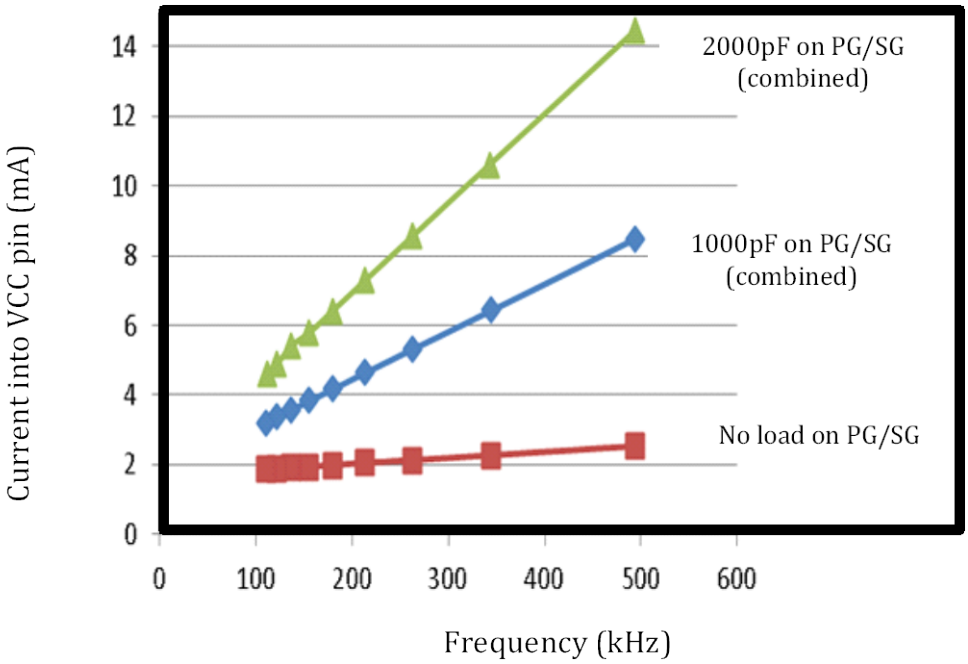

Figure 5: Supply Pin current as a function of its frequency (with different loads on its drivers)

Functional Block Diagram

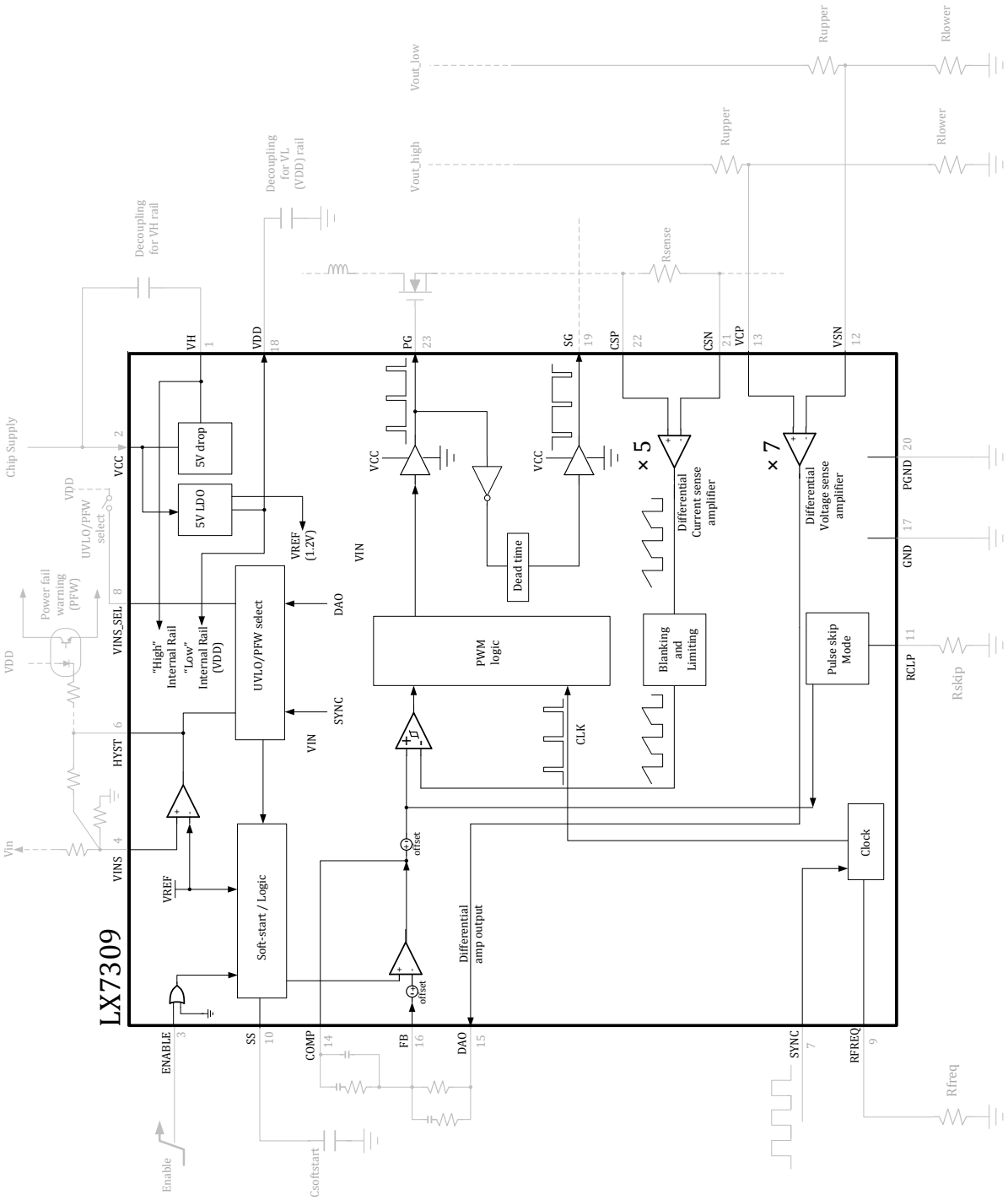

Figure 6: Block Diagram (LX7309)

Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability. The voltages are with respect to IC ground (GND and PGND combined), unless otherwise indicated.

		Min	Max	Units
VCC		-0.3	40	V
PG, SG		-0.3	20	V
VDD		-0.3	6	V
VH (with respect to VCC)		0.3	-6	V
All other pins		-0.3	VDD+0.3	V
Junction Temperature		-40	150	°C
Lead Soldering Temperature (40s, reflow)			260	°C
Storage Temperature		-65	150	°C
ESD rating	HBM		±2	kV
	MM		±200	V
	CDM		±500	V

Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics. The voltages are with respect to IC ground.

	Min	Max	Units
VCC	9.6	20	V
Fsw (adjustable frequency range)	100	500	kHz
Max Duty Cycle		44.5	%
f_{sw_synch} (synchronization frequency range)	200	1000	kHz
Ambient Temperature*	-40	85	°C

* Corresponding Max Operating Junction Temperature is 125°C.

Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ_{JA}		36		°C/W

Note: The θ_{JA} number assumes no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device (i.e. -40°C ≤ T_A ≤ +85°C , 7V ≤ VCC ≤ 20V). Typ values stated, are either by design or by production testing at 25°C ambient. The voltages are with respect to IC ground.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Current						
$V_{CC\_UVLO\_UP}$	UVLO threshold with input rising	V_{CC} rise time ≥ 0.5 ms;	8.85	9.15	9.5	V
$V_{CC\_UVLO\_DN}$	UVLO threshold with input falling	V_{CC} rise time ≥ 0.5 ms	7	7.3	7.6	V
I_{VCC_SD}	IC input current PG and SG = 1nF load to ground, No Load on VDD. RFREQ = 49.9k	V_{ENABLE} or VINS = Low. See Note 2		220	2000	µA
		V_{ENABLE} and VINS = High; V_{VCC} < $V_{CC\_UVLO\_UP}$; -40°C ≤ Temp ≤ +55°C. See Note 2			2000	uA
		V_{ENABLE} and VINS = High; V_{VCC} < $V_{CC\_UVLO\_UP}$; +55°C < Temp ≤ +85°C See Note 1,2			4.5	mA
I_{VCC_Q}	IC input current (switching, no load on SG, PG, VDD)	V_{ENABLE} = High, and V_{VCC} > $V_{CC\_UVLO\_UP}$, fsw = 500kHz			3.5	mA
Input UVLO/PFW						
VINS_TH	Threshold on VINS pin	Rising or falling	1.171	1.200	1.229	V
V_{HYST_HIGH}	Hysteresis pin high voltage	$I_{HYST\_SOURCING}$ = 1mA	2.8			V
V_{HYST_LOW}	Hysteresis pin low voltage	$I_{HYST\_SINKING}$ = 3mA			0.4	V
LDOs						
VDD	VDD rail	I_{VDD_EXT} < 5mA (current out of pin)	4.75	5	5.25	V
VH	VH rail (with respect to VCC)		20.9		23.9	V
VL	Hysteresis of V_{CLS_ON} threshold	No current in/out of pin		-5		V

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
Soft Start						
I_{SS_CH}	Current out of SS pin during charging phase	RFREQ=33.3k, V_{SS}=0.5V	32	36	40	µA
I_{SS_DISCH}	Current into SS pin during discharging phase	RFREQ=33.3k, V_{SS}=0.5V		10		% of I_{SS_CH}
V_{SS_CH}	Soft start charge completed threshold	By design only	90		95	% of VREF
V_{SS_DISCH}	Soft start discharge completed threshold			50		mV
R_{SS_DISCH}	Soft-start pin discharge FET resistance			50		Ω
t_{DISCH}	Soft-start discharge FET on- time			32		Switch cycles
Switching Frequency and Synchronization						
f_{sw_range}	Switching frequency accuracy	RFREQ=33.2k See Note 3	285	315	345	KHz
f_{sync_max}	Max synchronization frequency		1			MHz
V_{SYNC_HI}	SYNC pin high threshold		2.4			V
V_{SYNC_LO}	SYNC pin low threshold				0.8	V
t_{sync}	Minimum pulse width of SYNC pulse		100			ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D_{sync_max}	Max SYNC pulse duty cycle				90	%
Error Amplifier						
VREF	Reference voltage		1.171	1.200	1.229	V
$Gain_{DC\_OPL}$	DC Open-loop gain	Rload=100k	70	100		dB
AV_{UGBW}	Unity Gain Bandwidth	Cload=10pF (By design only)	2	5		MHz
I_{COMP_OUT}	Output sourcing current	$0.2V \leq V_{COMP} \leq 1.3V$	110		620	µA
I_{COMP_IN}	Output sinking current	$0.2V \leq V_{COMP} \leq 1.3V$	145		495	µA
$V_{EA\_CMR\_MAX}$	Max of input common-mode range		2			V
V_{CLAMP}	COMP pin high clamp		1.8	2.1	2.6	V
PWM Comparator						
V_{OFFSET}	Inserted offset in inverted input		200		300	mV
V_{RCLP}	Voltage set on RCLP pin by external resistor to GND		0		1	V
Current Sense Amplifier						
$Gain_{CSA}$	DC Gain		4.75	5	5.25	V
I_{AUX}	Max continuous current from V_{AUX}		4			mA
$V_{CSA\_CMR\_MAX}$	Max input common-mode range		2			V
t_{BLANK}	Blanking time		50		100	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ILIM}	Current limit threshold on output of current sense amplifier	Where PWM pulses start to get truncated	1.1	1.2	1.3	V
$V_{ILIMHICCUP}$	Current Limit threshold on output of current sense amplifier capability	Where PWM pulses start to get omitted in hiccup mode	1.7	1.8	1.9	V
Differential Voltage Amplifier						
$Gain_{DA}$	DC gain of differential voltage amp		6.68	7.0	7.14	
AV_{UGBW_DA}	Unity Gain Bandwidth of differential voltage amp			5		MHz
$V_{DA\_CMR\_MAX}$	Max of input common-mode range		3.5			V
Drivers						
R_{PG_HI}	Drive resistance when PG is high			10		Ω
R_{PG_LO}	Drive resistance when PG is low			5		Ω
t_{PG_MIN}	Minimum on-time of PG				120	ns
D_{MAX}	PG max duty cycle		44.5		50	%
R_{SG_HI}	Drive resistance when SG is high			10		Ω
R_{SG_LO}	Drive resistance when SG is low			10		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DEAD}	Deadtime	PG low to SG high or PG high to SG low	60	110	190	ns
Logic Levels on VINS and ENABLE						
V_{HI}	Input high threshold		2			V
V_{LO}	Input low threshold				0.8	V
Thermal Protection						
T_{SD}	Thermal shutdown (rising)			157		°C
T_{HYST}	Thermal shutdown hysteresis			15	30	°C

NOTES:
1) Current may be reduced using a simple circuit covered on page 25.
2) Min and Maximum current are guaranteed by design.
3) Switching Frequency Equation:

$$Freq = \frac{1}{(90pF \times R_{FREQ}) + 150ns}$$ where Freq is [Hz]

Applications Information

Setting Switching Frequency

A resistor, RFREQ, is connected from RFREQ pin to IC ground. Based on that, we get the following frequency

$$\text{fsw} = \frac{1}{(90\text{pf} \times \text{R}_{\text{FREQ}}) + 150\text{nSec}}$$ where Freq is [Hz]

For example, by setting RFREQ=33.2k, we get

$$\text{fsw} = \frac{1}{(90\text{pf} \times 33.2 \times 10^3) + 150\text{nSec}} = \frac{1}{(2.988\mu S + 150nS)} = 318.7\ \text{kHz}$$

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We can set any frequency between 100 to 500 kHz. Note that when synchronizing, the default frequency (as set by RFREQ) must be lower than the synchronization clock. In case the synchronization breaks, the converter will lapse back to the default value. When synchronizing, the switching frequency is ½ the synchronizing frequency.

Setting Soft-Start

A capacitor is connected between SS pin and IC ground. The current the cap is charged by is

$$I_{SS\_CHG} = \frac{1.2V}{RFREQ} \text{ (in seconds)}$$

For example, if RFREQ=49.9k, we get

$$I_{SS\_CHG} = \frac{1.2V}{49.9\times10^{3}} \text{ (in Amperes)} = 2.4\times10^{-5} \Rightarrow 24\mu A$$

So, to charge a 0.1µF ceramic cap on the soft-start pin from 0 to 1.2V will take

$$t_{SS} = \frac{C\times\Delta V}{I_{SS\_CHG}} \text{ (in seconds)} = \frac{0.1\mu\times1.2}{24\mu} \text{ (in seconds)} = \frac{0.12}{24} \text{ (in seconds)} = 5\times10^{-3} \text{(in seconds)} \Rightarrow 5ms$$

This is the soft-start time in this case.

Setting Pulse-skip Mode threshold

If a programming resistor RCLP is placed between RCLP pin and IC ground, the clamping voltage level is given by

$$V_{CLP} = \frac{0.3\times RCLP}{RFREQ} \text{ (in Volts)}$$

For example, if RCLP = RFREQ, say both are 49.9k, then the converter will enter pulse skipping when the output of the current sense amplifier drops to 0.3V. Note that the gain of this current amplifier is 5, so in terms of the voltage on the sense resistor (input of the current amp), we get 0.3V/5 = 0.06V. Since we usually design the converter so that its peak is around 0.2V (the peak of Rsense voltage before it starts to current limit), we are getting a ratio of 0.06V/0.2V = 0.3. In other words, the converter will enter pulse-skipping when the output current is 30% of the max designed output current.

Setting VPP UVLO/Hysteresis thresholds

Suppose we have a divider connected to input at the VINS pin. Suppose we call the resistors R_{UPPER} and R_{LOWER}. We also have a hysteresis resistor, R_{HYST}, from the output of the UVLO comparator, which provides positive

feedback on to the VINS pin, as explained in the Pin Description section. So, when the input voltage is rising, in effect the hysteresis resistor is in parallel to the lower resistor R_{LOWER}. When the voltage on the VINS pin rises above 1.2V, the UVLO comparator flips and the hysteresis resistor appears connected to 5V (output of the UVLO comparator).

Example for Setting the UVLO Thresholds:

VDD = 5.0V
VCC_{RISING} = 39.8V
$VCC_{FALLING}$ = 34.8V

Establish the Hysteresis:

$$Vh = V_{RISING} - V_{FALLING} = 39.8 - 34.8 = 5$$

Set R_{HYST} for 10µA current when HYST pin is high:

$$R_{HYST} = \frac{VDD-1.2}{10\times10^{-6}} = \frac{5-1.2}{10\times10^{-6}} = 380k \text{ ; use 374k}$$

Establish R_{UPPER} and R_{LOWER}:

$$R_{UPPER} = R_{HYST} \times \frac{Vh}{VDD} = 374 \times 10^3 \times \frac{5}{5} = 374k \text{ ; use 374k}$$

$$R_{LOWER} = \frac{1.2 \times R_{UPPER} \times R_{HYST}}{R_{HYST} \times V_{RISING} - 1.2(R_{UPPER} + R_{HYST})} = \frac{1.2 \times 374k \times 374k}{374k \times 39.8 - 1.2(374k + 374k)} = 12k$$

use 12.1k

So with the selected resistors, we get a rising threshold of 39.8V, and a falling threshold of 34.8V. Note that unless we tie VINS_SEL high (to VDD), the converter will not stop switching below 34.8V, but will stop only when VCC falls below its lower operating range of 7.6V.

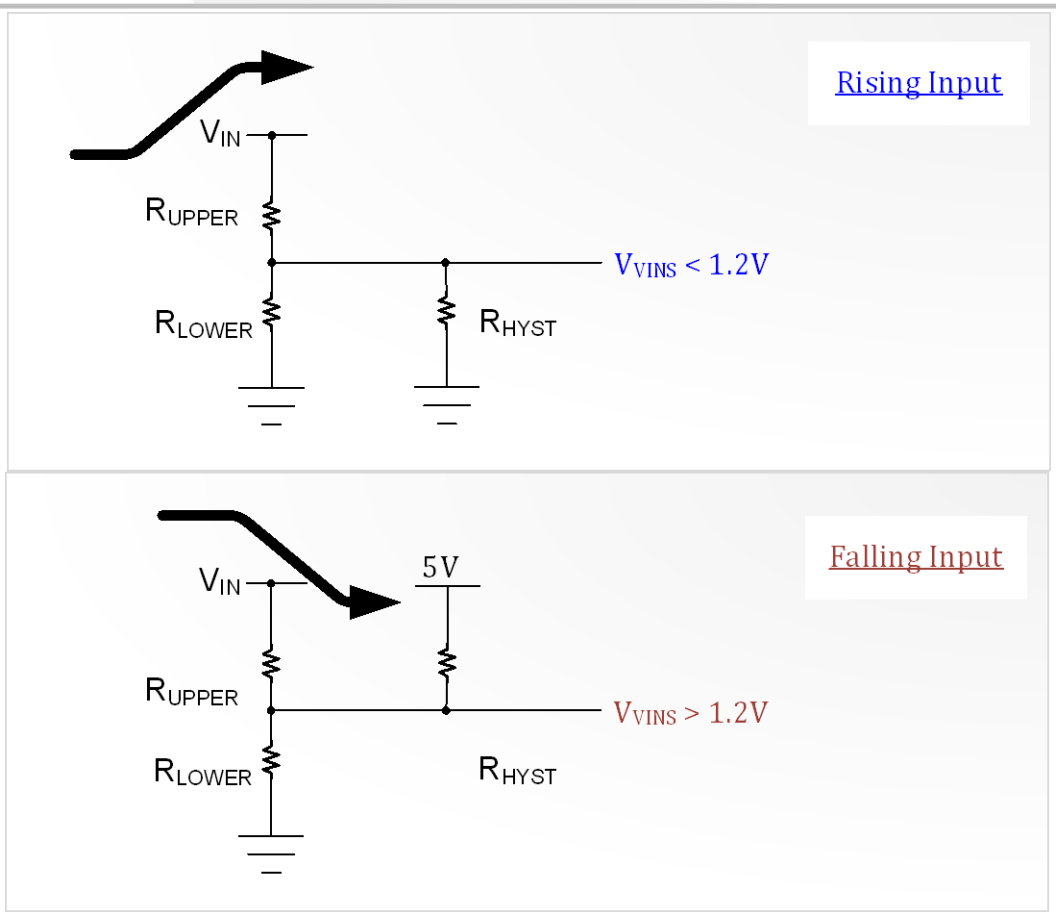


Figure 7: Equivalent Diagrams for UVLO and Hysteresis

Setting the Voltage Divider for Output Rails

Generically, we can state the equation for setting the output voltage to be

$$V_{OUT} = V_X \times \frac{R_{UP} + R_{LOW}}{R_{LOW}}$$

Where R_{UP} is the name we have given to the upper resistor (connected to output rail) and R_{LOW} is the name we have given here to the resistor connected to the lower rail (usually IC ground). Vx is the reference the feedback voltage is compared too. This is application dependent, but can be summarized for three cases:

a) Non-isolated topologies with simple divider connected to FB pin directly. For this use V_X = 1.2V.

b) Isolated topologies with divider to another reference (such as TL431 with an internal reference of 2.5V), as in Fig. 1. For this use V_X = 2.5V.

c) Non-isolated topologies with a differential divider connected to differential voltage amplifier of the LX7309 . Here we use the same divider equation provided above, but using V_X = 0.171V (that is 1.2V divided down by the gain of the diff-amp, i.e. by 7). We need two identical dividers as shown in Fig.2.

Selecting the Sense Resistor

In a Buck topology, the center of the switch current ramp equals the output current. To that we need to add about 30% for the peak current "I_{PEAK+}" because of the rising ramp caused by the inductor. That is a factor of 1.3. We also need to include some headroom for proper transient response at max load. Since the peak voltage on the sense resistor is 0.2V, to leave headroom, we should plan that the switch current peak stays at around 0.18V max at max load. This means that

$$I_{PEAK} = 1.3 \times I_O, \text{ So}$$

$$R_{SENSE} = \frac{0.18}{1.3 \times I_O} = \frac{0.138}{I_O}$$

$$R_{SENSE} = \frac{0.138}{I_O} \text{ (Buck)}$$

Assuming we have designed the converter to operate up to 44% max duty cycle, we can quickly estimate the peak current as follows.

For example, if we have a Buck application for 5A output, irrespective of the input and output voltage conditions (as long as they are not violating the min and max duty cycle limits of the converter), and assuming we have selected inductance appropriately, we should pick a sense resistor of

$$R_{SENSE} = \frac{0.138}{5A} = 0.028\,\Omega$$

For a Forward converter (Buck with a transformer), instead of the load current I_{OR} in the above equation, use the reflected load current of I_O/n, where n is the turns ratio (number of Primary-side turns divided by number of Secondary-side turns). You will also need to lower the sense resistance further to account for the magnetization current component on the switch side. So roughly

$$R_{SENSE} \approx \frac{0.138}{I_O} \times \frac{N_P}{N_S} \quad \text{(Forward)}$$

For a Boost or Buck-Boost, we have to account for the fact that the peak current is not just 1.3 times max load current, but is actually

$$I_{PEAK} = 1.3 \times \frac{I_O}{1-D} \quad \text{(where D can be as high as 44\%)}$$

So we should use the following equation for sense resistor

$$R_{SENSE} = \frac{0.18 \times (1-D)}{1.3 \times I_O} = \frac{0.101}{1.3 \times I_O} = \frac{1}{13 \times I_O}$$

$$R_{SENSE} = \frac{0.077}{I_O} \quad \text{(Boost, Buck-Boost)}$$

For example, if the max load current is 5A, the sense resistor value to use is

$$R_{SENSE} = \frac{0.077}{5A} = 0.015\ \Omega$$

As we can see, this is roughly half of what we got for the Buck (same load current).

For a Flyback topology (Buck-Boost with a transformer), we have to use the reflected output current. So we get

$$R_{SENSE} \approx \frac{0.077}{I_O} \times \frac{N_P}{N_S} \quad \text{(Flyback)}$$

Input Feedfoward

One of the 'tricks' to more effective current limiting in Flyback converters is to place a resistor from V_{IN} to the I_{SENSE} pin. The purpose of this is to reduce the current limit and thus also effectively limit the maximum available duty cycle at high line. At high line the steady operating duty cycle is naturally lower, and so is the peak current.

But under overloads, the converter will try to hit any available brickwall, whichever comes up first. So it will try to reach maximum duty cycle or hit current limit, all this happening till the slower Secondary-side current limit can start to work and limit the output power. But even during this interval, damage can occur.

This situation cannot be understood in terms of any steady state scenario. For example if the output voltage is zero (perfect short), then the down-slope of the Primary-side inductor current V_{OR}/L_P (or equivalently the down-slope of the Secondary-side current V_O/L_S) is almost zero (actually it is V_D/L). Therefore the current can never reach the state it started the cycle off with, and steady-state by definition does not exist. So we will ultimately get a 'flux-walking'/'current staircasing' condition. Till we hit the current limit. But now, though the peak Primary-side peak current is supposedly fast and limited precisely by the sense resistor, and should therefore protect the switch and the transformer from saturation, this does not happen in practice. It can be shown that the blanking time requirement of all current mode control ICs such as the LX7309 translates to a minimum pulse width. And it can be shown that that can *effectively over-ride any set current limit*, in this condition. The current limit, whenever reached, can only respond by commanding the controller to limit the duty cycle further. Which it may not be able to do anymore. Even during this minimum pulse width of 100 ns to 150 ns or so, the slope of the up-ramp which is V_{IN}/L, is very high. And there is also virtually no down-ramp. So the current will actually continue to staircase beyond the set current limit. Many modern current mode DC-DC controllers/switchers respond by initiating a 'frequency foldback' whenever the voltage on the feedback pin falls below a certain threshold. In doing so they effectively reduce the duty cycle under current limit, and this extends the off-time by a typical factor of 4 to 6, giving enough time for the current to ramp down to a value less than what it started the cycle with, thereby quashing staircasing. But note that the effectiveness of this technique depends largely on the diode drop! So 'good' diodes (with lower forward drops) actually make the fault currents even more severe, as they do not provide enough down-slope.

In the case of the LX7309 we can protect ourselves from this situation by *reducing the current limit at high line, so we have some enforced headroom available before the transformer can saturate*. We now give the equations to implement this.

Basically, by introducing a 'feedforward' resistor R_{FF}, the current sense signal is DC shifted a little higher by an amount $R_{FF} \times I_{FF}$, so it will hit the current limit a little earlier. Note that we do not want to affect the current limit at lower input voltages. If R_{BL} is the resistor normally connected between the sense resistor and the current sense pin of the IC (CSP), (typically 100 Ω to 1 kΩ or so), the current limit at high line V_{IN_MAX} as a ratio of the current limit at V_{IN_LO} is

$$\frac{CLIM_{VIN\_MAX}}{CLIM_{VIN\_LO}} = \frac{V_{CLIM} - \left(\frac{V_{IN\_MAX}}{R_{FF}} \times R_{BL} \right)}{V_{CLIM} - \left(\frac{V_{IN\_LO}}{R_{FF}} \times R_{BL} \right)}$$

where V_{CLIM} is the voltage on the current sense pin corresponding to current limit (0.2V in the case of the LX7309). So if for example, in a universal input AC-DC application, V_{IN_MAX} = 389VDC, V_{IN_LO} = 85VDC, R_{BL}=1k, V_{CLIM} = 1V, we get the required value of the feedforward resistor for reducing the current limit threshold from 0.2V to 0.15 V (factor of 0.75V)

$$0.75=\frac{1-\left(\frac{389}{R_{FF}}\times 1000\right)}{1-\left(\frac{85}{R_{FF}}\times 1000\right)}$$

Solving we get

$$R_{FF}=1.3M$$

At 60VAC (85VDC) this will also lower the current limit threshold slightly below 0.2V. The current I_{FF} is 85VDC/1.3M=65µA. Passing through the blanking resistor 1kΩ, it causes a drop of 0.065V. So the current limit threshold is now 0.2-0.065 = 0.135V. Note that the current limit threshold actually has a typical tolerance of ±10%. Knowing this we can correctly set R_{SENSE} (in series with FET).

Start-up Circuits

Many applications use input voltages higher than the rated maximum voltage for VCC. For these applications, VCC must be provided by means of an external regulator or voltage source. Most Flyback and Forward applications use an additional winding on the power transformer or inductor to generate VCC. This method is shown in both Figures 1 and 2. Generating VCC by means of an additional winding, (sometimes called a "bootstrapped" supply), requires that the converter must be running and at the correct output voltage for the generated VCC to be stable and at the correct voltage. For these applications a method to start-up the controller and keep it running long enough for the bootstrapped supply to provide stable VCC must be implemented.

The most simple of these methods is shown in Figure 8. This simple resistor-capacitor circuit, connected between the input voltage and ground, provides enough current at VCC UVLO to start the controller and keep it running until the bootstrap supply is stable. The resistor is sized to provide enough current to charge the VCC capacitor and satisfy the maximum standby current requirement; the capacitor is sized to hold up the voltage long enough for the bootstrap supply to take over.

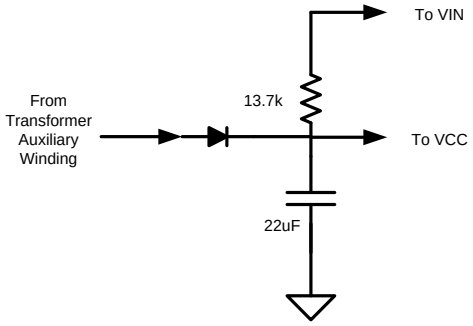


Figure 8: Simple Start-Up Circuit

The start-up resistor's value is calculated using the difference of the minimum input voltage, the maximum UVLO rising threshold divided by the maximum standby current:

$$R_{START} = \frac{V_{MIN} - V_{UVLOMAX}}{I_{STANDBYMAX}}$$

For minimum input voltage of 37V, and using the values found in the Electrical Characteristics Table for V_{UVLO} and maximum standby current:

$$R_{START} = \frac{37V - 9.5V}{2mA} = 13.7k$$

The absolute worst case power dissipation of the start-up resistor will be at maximum input voltage, with the VCC capacitor fully discharged. To account for this condition the power is simply $Vmax^2/R_{START}$. However, this equation accounts for the worse case condition with VCC = 0, and doesn't take into account the steady state power dissipation, which is less. In actual applications the period of time taken to charge the VCC cap to the UVLO level is short, in which case the steady state power dissipated by the resistor can be found by:

$$P_{R_{START}} = \frac{(V_{MAX} - V_{UVLOMINFALL})^2}{R_{START}}$$

For example: If VMAX = 57V, and using the minimum threshold for falling UVLO from the Electrical Characteristics Table:

$$P_{R_{START}} = \frac{(57V - 7V)^2}{13.7k} = 183mW$$

The user needs to take into account the surge rating of start-up resistor used and the period of time taken to charge VCC to the UVLO point to insure that the maximum surge rating of the resistor is not exceeded. When in doubt, it is best to use the worse case power dissipation at VCC = 0.

Sizing the VCC capacitor requires knowledge of operating current during the start-up phase. Operating current is application dependent, in that it is affected by number of FETs used and their respective gate charges, as well as external loads on VDD and VCC . Using the value of operating current (either estimated or measured), the capacitor needs to be sized to keep VCC from dropping below the maximum UVLO falling limit during the soft start period, which starts at the minimum UVLO rising threshold. For example, assuming that all of the operating current is provided by the capacitor, and using an estimated operating current of 5mA, soft start time of 5ms and the value for minimum rising UVLO and maximum falling UVLO found in the Electrical Characteristics Table:

$$C_{VCC} = \frac{T_{SS} \times I_{OP}}{V_{UVLOMINRISE} - V_{UVLOMAXFALL}} = \frac{5ms \times 5mA}{8.85V - 7.6V} = 20\mu F$$

For this example we would use a 22uF capacitor.

The above method requires minimum parts; however, the start-up resistor dissipates unneeded power after the converter has started, and it's large value and large VCC capacitor creates a long delay time from the initial application of voltage to the UVLO threshold. Adding a zener diode and pass transistor creates a more efficient start-up method. This method is outlined in Figure 9.

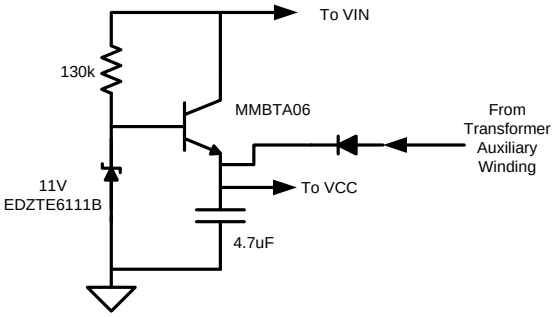


Figure 9: Efficient Start-Up Circuit

For the above circuit, the zener is sized such that after start-up (during normal operation) the pass transistor's Base-Emitter junction is reversed biased. Under this condition VCC current flows from the bootstrap supply only. With this method the only power loss is through the zener and resistor, which can be reduced to a minimum. Also smaller VCC capacitor can be used, due to the fact that the current required to hold up VCC during start-up is sourced by the pass transistor.

The pass transistor is sized to provide the operating current during start-up, with a maximum collector-emitter voltage rating greater than the maximum input voltage.
The current limiting resistor is sized at minimum input voltage to provide the minimum required zener current for regulation, as well as the minimum base current to meet the DC gain required by the transistor. Using our example:

With V_{MAX} = 57V, we choose an 80V transistor. The transistor chosen has a maximum current capability of 100mA, which more than meets our needs. Our bootstrap supply is designed with an average steady state output of 12V. The zener voltage needs to be a minimum of 0.7V below this. An 11V zener will meet this requirement. During the soft start period, the transistor will provide VCC current. VCC voltage during this period needs to be above the maximum UVLO and will be approximately:

$$\mathrm{VCC}=V_{\mathrm{ZENER}}\text{-}\mathrm{VBE} \cong 11V - 0.7V = 10.3V$$

10.3V is above the maximum UVLO of 9.6V.

The current limiting resistor is calculated based on the DC gain of the transistor and the zener current requirements. Using the datasheet for the chosen zener, the zener voltage is acceptable at 100uA. The DC gain of the transistor at 10mA is specified at 100, which will require a minimum base current of 100uA. This transistor has plenty of margin, so we can use a base current of 100uA. The minimum required current provided by the resistor at the minimum input voltage is 200uA. For a minimum input voltage of 37V:

$$\mathrm{R_{LIM}}=\frac{\mathrm{V_{MIN}}-\mathrm{V_{ZENER}}}{I_{\mathrm{MIN}}}=\frac{37\mathrm{V}-11\mathrm{V}}{200\mu\mathrm{A}}=130k$$

The power dissipated by the limiting resistor and zener are determined at the maximum input voltage. For maximum input voltage of 57V:

$$\mathrm{P_{R_{LIM}}}=\frac{(57\mathrm{V}-11\mathrm{V})^2}{130\mathrm{k}}=16\mathrm{mW}$$

$$\mathrm{P_{ZENER}}=\frac{(57\mathrm{V}-11\mathrm{V})}{130\mathrm{k}}\times 11\mathrm{V}=4\mathrm{mW}$$

Note: Care must be taken that the voltage generated by the bootstrap supply does not exceed the maximum specified reverse breakdown voltage for the transistor's base-emitter junction. If the voltage exceeds the specified reverse VBE, then a small signal diode, such as a MMBD4148 may be placed in series with the emitter and VCC. If this extra diode is needed, the zener voltage may need to be increased to account for the extra voltage drop.

Controlling Standby Current

The LX7309 standby current at temperatures greater than +55°C may be improved by replacing the typical 100k pull-up resistor connected between VDD and Enable with a simple RC connected between VDD and Pin 17 GND. For this method, size the resistor and capacitor such that the voltage at the enable is delayed with respect to the rising VCC voltage. Set the delay such that the voltage at VCC reaches 5.0V before the voltage at enable is above 1.1V. The following component values may be used for a start-up resistor of 13k and a 22uF VCC filter:

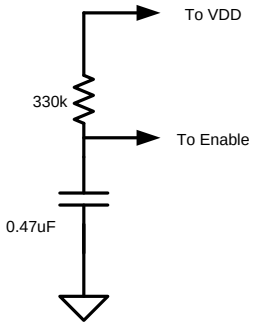


Figure 10: Enable Delay Circuit for Reducing High-Temperature Standby Current

Using the above method will reduce the maximum VCC standby current to 2mA at temperatures greater than +55°C.
Note: this method is only needed if the simple start-up circuit shown in Figure 8 is used; this method is not necessary if using the start-up circuit shown in Figure 9.

The value of the above capacitor needed for proper delay may be estimated using the following method:

Example Parameters:
VCC cap = 22uF
R_{START} = 13k
V_{MIN} = 37V
Enable Pullup Resistor = 330k
I_{CC} = 2mA

First determine the starting and finishing current when charging VCC capacitor to 5V:

$$I_{CAP_{START}} = \frac{V_{MIN}}{R_{START}} - I_{CC} = \frac{37V}{13k} - 2mA = 846\mu A$$

$$I_{CAP_{FINISH}} = \frac{V_{MIN} - V_{FINISH}}{R_{START}} - I_{CC} = \frac{37V - 5V}{13k} - 2mA = 462\mu A$$

Next, determine the time required for the VCC voltage to reach 5V:

$$T_{5V} = \ln\left(\frac{I_{CAP_{FINISH}}}{I_{CAP_{START}}}\right) \times R_{START} \times CAP_{VCC} = \ln\left(\frac{462\mu A}{846\mu A}\right) \times 13k \times 22uF = 173ms$$

There is an approximate 2 diode drop (1.4V) between VCC and VDD at voltages below 7V. This voltage offset will delay the start of VDD rising by:

$$I_{CAP_{1.4V}} = \frac{V_{MIN} - 1.4V}{R_{START}} - I_{CC} = \frac{35.6V}{13k} - 2mA = 738\mu A$$

$$T_{DLY} = \ln\left(\frac{I_{CAP_{1.4V}}}{I_{CAP_{START}}}\right) \times R_{START} \times CAP_{VCC} = \ln\left(\frac{738\mu A}{846\mu A}\right) \times 13k \times 22uF = 39ms$$

The average VDD voltage during the time period required for VCC to reach 5V is determined:

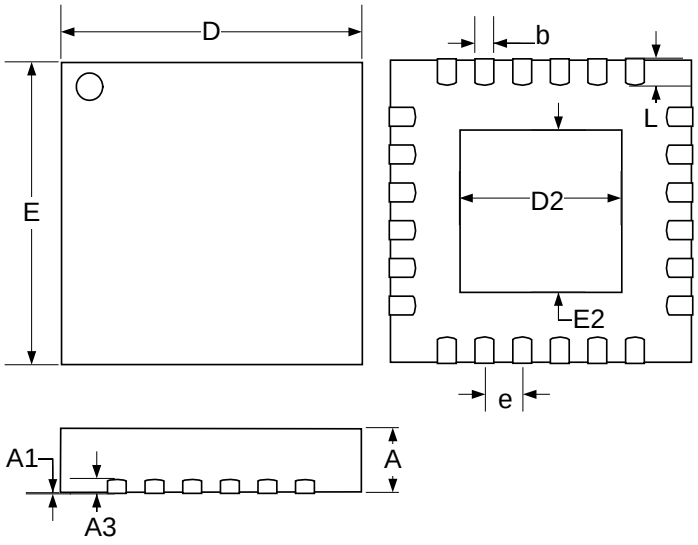
$$VDD_{AVG} = \frac{5V - 1.4V}{2} = 1.8V$$

Finally the estimated capacitor required on Enable pin for the proper delay:

$$C_{DLY} = \frac{T_{5V} - T_{DLY}}{\left|\ln\left(1 - \frac{V_T}{VDD_{AVG}}\right)\right| \times R_{PULLUP}} = \frac{173ms - 39ms}{\left|\ln\left(1 - \frac{1.1V}{1.8V}\right)\right| \times 330k} = 0.39\mu F$$

For margin, use a 0.47uF.

Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.011
D	4.00 BSC		0.157 BSC	
E	4.00 BSC		0.157 BSC	
e	0.50 BSC		0.019 BSC	
D2	2.30	2.55	0.090	0.100
E2	2.30	2.55	0.090	0.100
L	0.30	0.50	0.012	0.020

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.