I²C to CAN-Physical Transceiver

FEATURES

- **Protected from Overvoltage Line Faults to ±40V**
- **Up to 400kbps I²C Communications**
- **4V to 60V Power Supply Range with Internal 3.3V Regulator**
- **3.3V or 5V Bus Voltage**
- **Extended Common Mode Range (±36V)**
- Current Limited Drivers with Thermal Shutdown
- Power-Up/Down Glitch Free Driver Outputs
- Low Current Shutdown Mode
- Transmit Data Dominant Timeout Function
- E- and J-Grades Available
- Available in a 10-Lead MSOP Package
- AEC-Q100 Qualification in Progress

DESCRIPTION

The LT®3960 is a robust high speed transceiver that extends a single-master I²C bus through harsh or noisy environments at up to 400kbps using the CAN-physical layer. One LT3960 sits near the I²C master, creating from SCL and SDA equivalent differential buses (I²CAN) on two twisted pairs. At the other end of the twisted pairs, a second LT3960 recreates the I²C bus locally for any slave I²C devices. A built-in 3.3V LDO powers both the I²C and I²CAN buses from a single input supply from 4V to 60V. Alternatively, the LT3960 can be powered directly from a 3.3V or 5V supply.

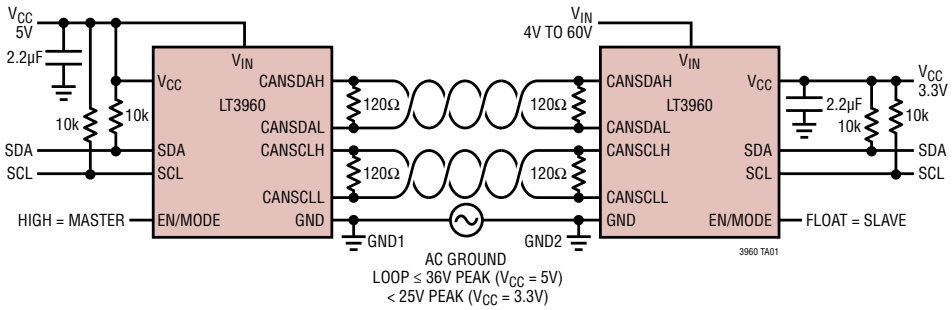
The LT3960 is available in a 10-lead MSOP package.

APPLICATIONS

- Industrial Networking
- Automotive Networking
- Remote Sensors

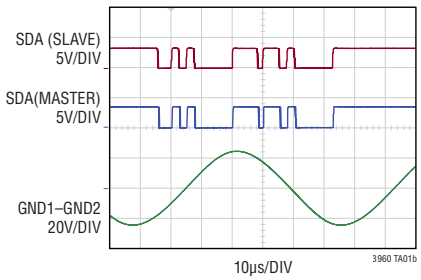
TYPICAL APPLICATION

I²CAN Bus Link with Large Ground Loop Voltage



AC GROUND
LOOP ≤ 36V PEAK (V_{CC} = 5V)
< 25V PEAK (V_{CC} = 3.3V)

Receiving I²C Traffic Across ±25V Common-Mode Differential



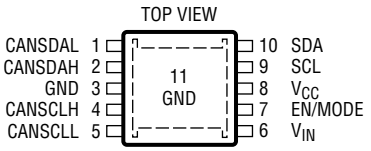
SLAVE-MODE LT3960
POWERED BY INTERNAL LDO (V_{CC} = 3.3V)

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{IN} 60V
V_{CC}, EN/MODE 5.5V
SDA, SCL .....–0.3V to V_{CC} + 0.3V
CANSDAH, CANSDAL, CANSCLH, CANSCLL .....–40V to 40V
Operating Junction Temperature Range
LT3960E .....–40°C to 125°C
LT3960J.....–40°C to 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3960EMSE#PBF	LT3960EMSE#TRPBF	LTHJP	10-Lead Plastic MSOP	–40°C to 125°C
LT3960JMSE#PBF	LT3960JMSE#TRPBF	LTHJP	10-Lead Plastic MSOP	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT3960EMSE#WPBF	LT3960EMSE#WTRPBF	LTHJP	10-Lead Plastic MSOP	–40°C to 125°C
LT3960JMSE#WPBF	LT3960JMSE#WTRPBF	LTHJP	10-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{CC} = 3.3V, Figure 1 Applies with R_{PU} = 4.99k, R_L = 60Ω, EN/MODE = V_{CC}, TYP values unless otherwise specified.

SYMBOL	PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IN} Low Dropout Regulator									
V_{IN}	Input Voltage Operating Range		V_{CC} Regulated Internally from V_{IN} V_{IN} Tied to V_{CC}, 3.3V Range V_{IN} Tied to V_{CC}, 5V Range		● ● ●	4 3 4.5		60 3.6 5.5	V V V
$I_{IN(SD)}$	V_{IN} Shutdown Current		EN/MODE = 0V				20	26	µA
V_{CC}	LDO Regulation Voltage		4V ≤ V_{IN} ≤ 60V, I_{LDO} = 1mA			3.1	3.3	3.5	V
V_{LINE}	LDO Line Regulation		4V ≤ V_{IN} ≤ 60V, I_{LDO} = 1mA				0.05		%/V
V_{LOAD}	LDO Load Regulation		0.1mA < I_{LDO} < 100mA				0.05		%/mA
$V_{CC,LOW}$	LDO Voltage at Low V_{IN}		I_{LDO} = 85mA, V_{IN} = 4V			3			V
$ILIM_{CC}$	LDO Current Limit LDO Foldback Current Limit		V_{CC} = 3.0 V_{CC} = 0.5V			100	130 25	160	mA mA
V_{UVLO}	V_{CC} Undervoltage Lockout Threshold V_{CC} Undervoltage Lockout Hysteresis		V_{CC} Falling		●	2.6	2.7 75	2.9	V mV
I_{CC}	V_{CC} Shutdown Supply Current V_{CC} Operating Supply Current		EN/MODE = 0V, V_{CC} = V_{IN} EN/MODE ≥ 0.7V, V_{CC} = V_{IN}				 4.2	3 6	mA mA
EN/MODE Selection									
V_{SHDN}	EN/MODE Shutdown Threshold Falling				●	400	700	800	mV
$V_{SHDN-HYS}$	EN/MODE Shutdown Hysteresis						50		mV
V_{MSTR}	EN/MODE Master Threshold				●	1.9	2	2.2	V
I_{EN-UP}	EN/MODE Pin Bias Current Low		EN/MODE = 350mV				2		µA
CAN Drivers									
$V_{O(D)}$	Bus Output Voltage (Dominant)	CANxH	t < $t_{TO:CAN}$	V_{CC} = 3.3V	●	2.15	2.9	3.3	V
				V_{CC} = 5V	●	2.75	3.6	4.5	V
		CANxL	t < $t_{TO:CAN}$	V_{CC} = 3.3V	●	0.5	0.9	1.65	V
				V_{CC} = 5V		0.5	1.4	2.25	V
$V_{O(R)}$	Bus Output Voltage (Recessive)		V_{CC} = 3.3V, No Load (Figure 1) V_{CC} = 5V, No Load (Figure 1)		● ●	1.45 2	1.95 2.5	2.45 3	V V
$V_{OD(D)}$	Differential Output Voltage (Dominant)		R_L = 50Ω to 65Ω	V_{CC} = 3.3V	●	1.5	2.2	3	V
$V_{OD(D)}$	Differential Output Voltage (Dominant)			V_{CC} = 5V		2.7	3.1	3.5	V
$V_{OD(R)}$	Differential Output Voltage (Recessive)		No Load (Figure 1)		●	–500	0	50	mV
$V_{OC(R)}$	Common Mode Output Voltage (Dominant)		V_{CC} = 3.3V, (Figure 1) V_{CC} = 5V, (Figure 1)		● ●	1.45 2	1.95 2.5	2.45 3	V V
$I_{OS(D)}$	Bus Output Short-Circuit Current (Dominant)	CANxH	CANxH = 0V		●	–150	–75	–40	mA
		CANxH	–40V < CANxH < $V_{O(R)}$		●	–150		3	mA
		CANxL	CANxL = 5V		●	25	75	100	mA
		CANxL	V_{CC} < CANxL < 40V		●	–3		100	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{CC} = 3.3V, Figure 1 applies with R_{PU} = 4.99k, R_L = 60Ω, EN/MODE = V_{CC}, TYP values unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CAN Receivers							
V_{CM}	Bus Common Mode Voltage = (CANxH+CANxL)/2 for Data Reception	V_{CC} = 3.3V V_{CC} = 5V	● ●			±25 ±36	V V
V_{TH}+	Bus Input Differential Threshold Voltage (Positive Going)	V_{CC} = 3.3V, –25V ≤ V_{CM} ≤ 25V V_{CC} = 5V, –36V ≤ V_{CM} ≤ 36V	● ●		775 775	900 900	mV mV
V_{TH}–	Bus Input Differential Threshold Voltage (Negative Going)	V_{CC} = 3.3V, –25V ≤ V_{CM} ≤ 25V V_{CC} = 5V, –36V ≤ V_{CM} ≤ 36V	● ●	500 500	625 625		mV mV
ΔV_{TH}	Bus Input Differential Hysteresis Voltage	V_{CC} = 3.3V, –25V ≤ V_{CM} ≤ 25V V_{CC} = 5V, –36V ≤ V_{CM} ≤ 36V			150 150		mV mV
R_{IN}	Input Resistance (CANxH and CANxL)	SCL = SDA = V_{CC}; R_{IN} = ΔV/ΔI; ΔI = ±20 µA	●	25	35.7	50	kΩ
R_{ID}	Differential Input Resistance	SCL = SDA = V_{CC}; R_{IN} = ΔV/ΔI; ΔI = ±20 µA	●	50	71.4	100	kΩ
ΔR_{IN}	Input Resistance Matching	R_{IN} (CANxH) to R_{IN} (CANxL)	●			±3	%
C_{IH}	Input Capacitance to GND (CANxH)	(Note 4)			32		pF
C_{IL}	Input Capacitance to GND (CANxL)	(Note 4)			8		pF
C_{ID}	Differential Input Capacitance	(Note 4)			8.4		pF
I_L	Bus Leakage Current (Power Off)	V_{CC} = 0V, CANxH = CANxL = 5V				±10	µA
		V_{CC} = 0V, CANxH = CANxL = 5V, t < 150°C	●			±50	µA
I^2C Port							
V_{IL}	SDA, SCL Input Low Voltage		●			0.4	V
V_{IH}	SDA, SCL Input High Voltage		●	1.5			V
I_i	SDA, SCL Input Leakage Current	SDA = SCL = 0V to 5.5V		–50		50	nA
Vhys	SDA, SCL Input Hysteresis		●	0.05 • V_{CC}			V
V_{OL1}	SDA, SCL Output Low Voltage	I_{SDA} = 3mA	●			0.4	V
t_r	Clock/Data Rise Time	C_B = Capacitance of One Bus Line (pF) (Note 5)		20 + 0.1C_B		300	ns
t_f	Clock/Data Fall Time	C_B = Capacitance of One Bus Line (pF) (Note 5)		20 + 0.1C_B		300	ns

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{CC} = 3.3V, Figure 2 applies with R_{PU} = 4.99k, R_L = 60Ω, EN/MODE = V_{CC}, TYP values unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Transceiver Timing								
f_{SCL}	SCL Clock Frequency (Notes 5,6)			●	0		400	kHz
t_{PI2CBD}	I^2C to I^2CAN Dominant Propagation Delay	(Figure 2, Figure 3)	V_{CC} = 3.3V	●	45	80	130	ns
			V_{CC} = 5V	●	45	75	115	ns
t_{PI2CBR}	I^2C to I^2CAN Recessive Propagation Delay	(Figure 2, Figure 3)	V_{CC} = 3.3V	●	80	120	170	ns
			V_{CC} = 5V	●	60	90	120	ns
t_{PBI2CD}	I^2CAN Dominant to I^2C Propagation Delay	(Figure 2, Figure 3)	V_{CC} = 3.3V	●	25	40	65	ns
			V_{CC} = 5V	●	25	40	65	ns
t_{PBI2CR}	I^2CAN Recessive to I^2C Propagation Delay	(Figure 2, Figure 3)	V_{CC} = 3.3V	●	25	45	80	ns
			V_{CC} = 5V	●	20	35	60	ns
$t_{TO;CAN}$	I^2CAN Dominant Timeout Time	(Figure 2, Figure 4)		●	0.5	1.5	2	ms
$t_{EN;I2C}$	I^2C Driver Enable from Shutdown	V_{CC} = 3.3V or 5V (Figure 2, Figure 5)		●			40	µs
$t_{EN;CAN}$	I^2CAN Driver Enable from Shutdown	V_{CC} = 3.3V or 5V (Figure 2, Figure 6)		●			40	µs
$t_{SHDN;I2C}$	Time to Shutdown, I^2C	(Figure 2, Figure 5)		●			500	ns
$t_{SHDN;CAN}$	Time to Shutdown, I^2CAN	(Figure 2, Figure 6)		●			500	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3960E is guaranteed to meet specified performance from 0°C to 125°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT3960J is guaranteed to meet performance specifications over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: The LT3960 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature is active. Continuous operating above the specified maximum operating junction temperature may impair device reliability.

Note 4: Pin capacitance given for reference only and is not tested in production.

Note 5: Rise and fall times are measured at 30% and 70% levels.

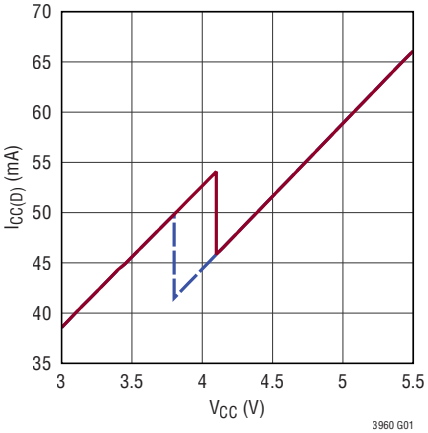
Note 6: Maximum SCL clock frequency will be affected by delays through the twisted-pair interface and I/O circuitry of other devices on the bus. These delays may limit the operation frequency to below the LT3960 maximum specification.

Note 7: The LT3960 does not support clock stretching. SCL should not be pulled low by slave devices.

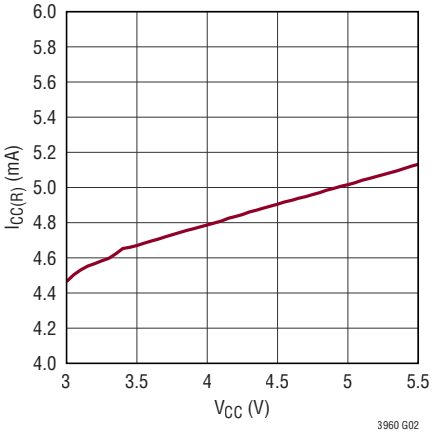
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V, R_{PU} = 60Ω unless otherwise noted.

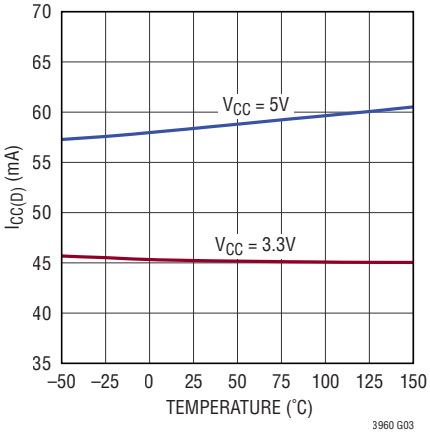
Supply Current (I^2CAN Dominant) vs V_{CC}



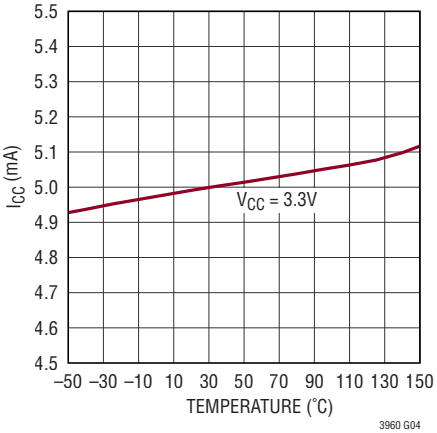
Supply Current (I^2CAN Recessive) vs V_{CC}



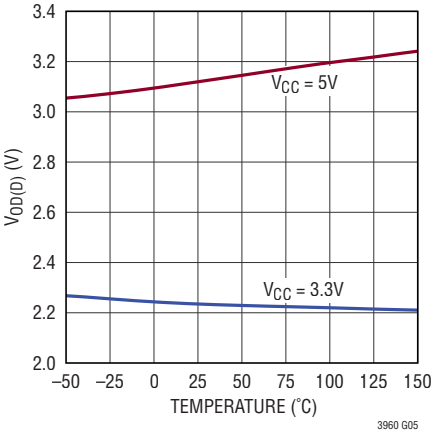
Supply Current (I^2CAN Dominant) vs Temperature



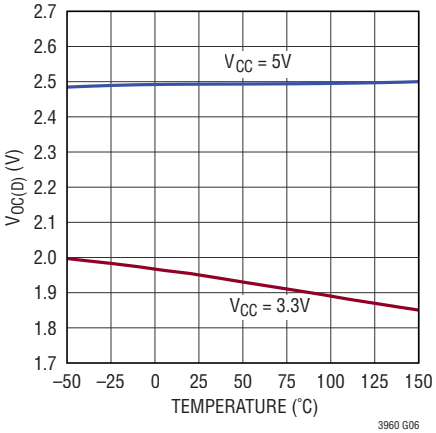
Supply Current (I^2CAN Recessive) vs Temperature



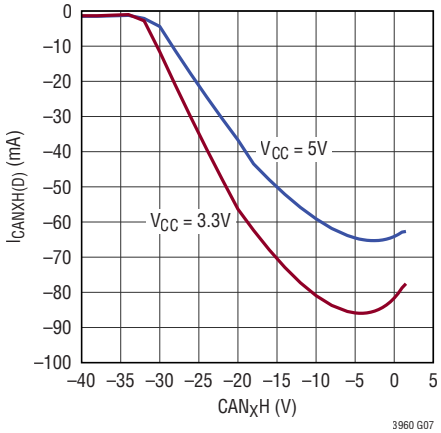
I^2CAN Differential Output Voltage (Dominant) vs Temperature



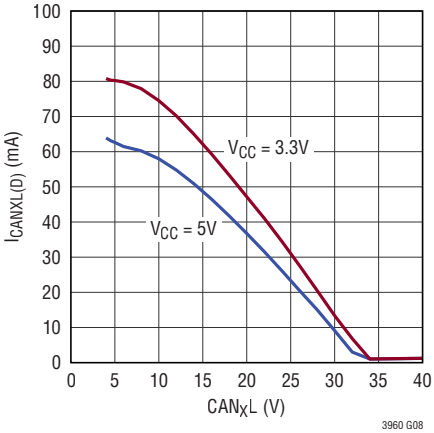
I^2CAN Common Mode Voltage (Dominant) vs Temperature



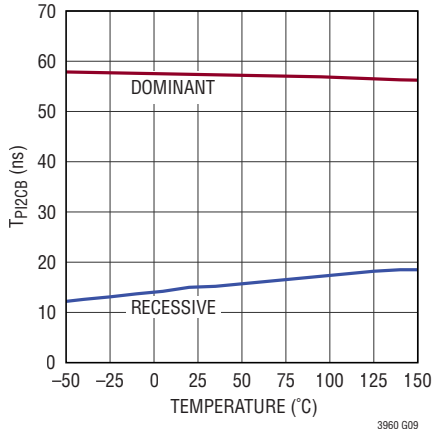
CANxH Short-Circuit Current (Dominant) vs CANxH Voltage



CANxH Short-Circuit Current (Dominant) vs CANxH Voltage



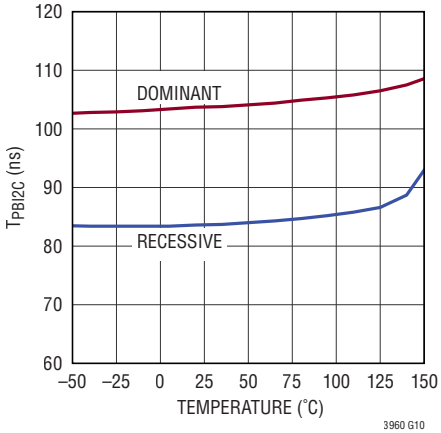
I^2C to CAN Propagation Delay vs Temperature



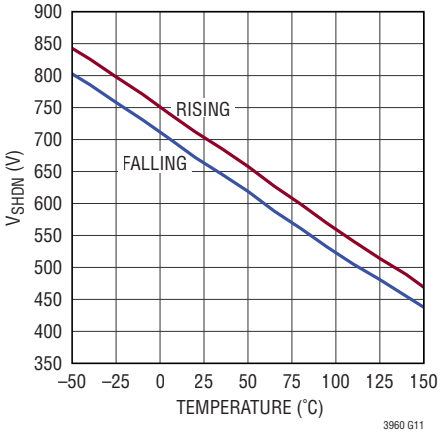
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V, R_{PU} = 60Ω unless otherwise noted.

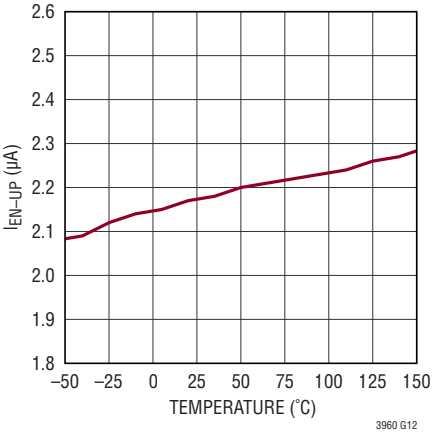
CAN to I²C Recessive Propagation vs Temperature



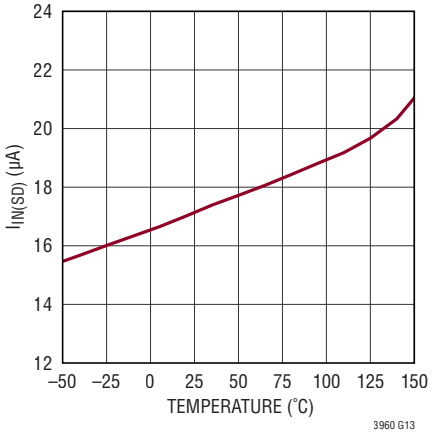
EN/MODE Shutdown Thresholds vs Temperature (V_{CC} = 3.3V, 5V)



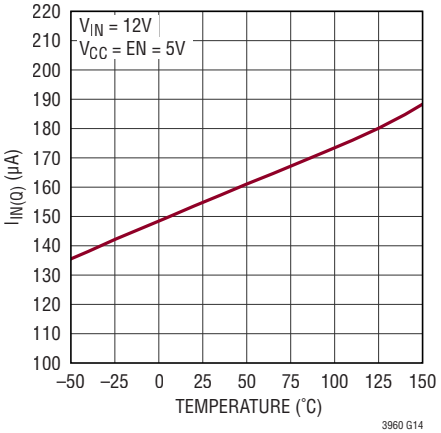
EN/MODE Current vs Temperature ($V_{EN/MODE}$ = 0.35V)



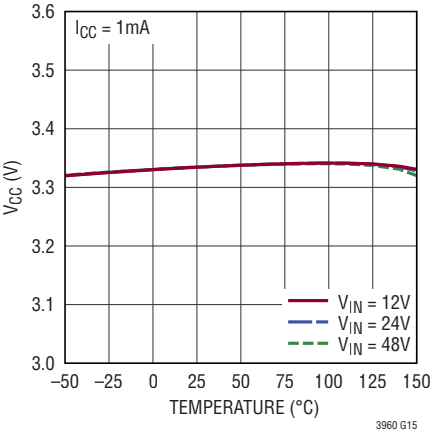
V_{IN} Shutdown Current vs Temperature



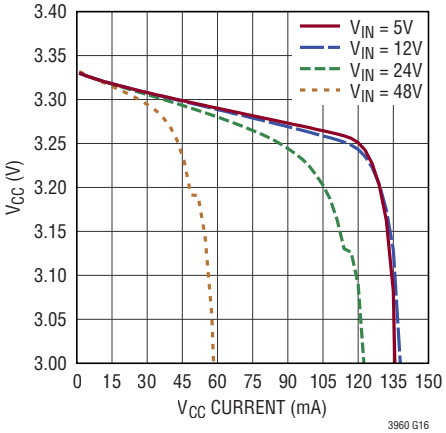
V_{IN} Quiescent Current vs Temperature



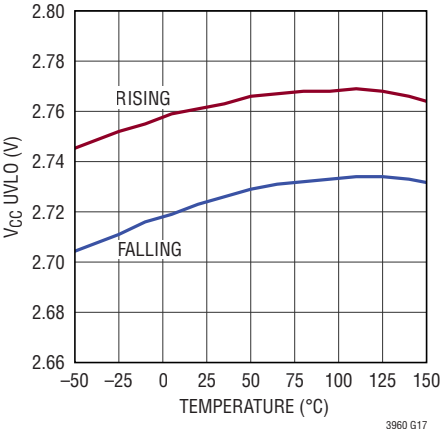
V_{CC} vs Temperature (Various V_{IN})



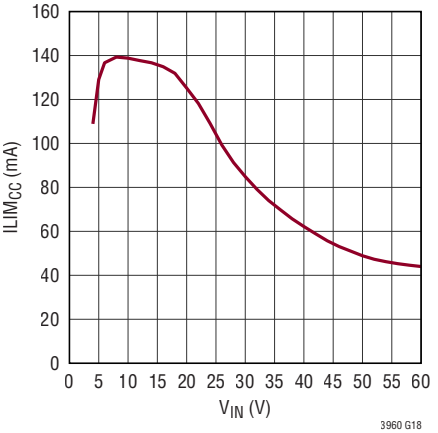
V_{CC} vs Current (Various V_{IN})



V_{CC} UVLO vs Temperature



V_{CC} Current Limit vs V_{IN}



PIN FUNCTIONS

CANSDAL (Pin 1): Low Level CAN Bus Line. Carries the I^2C data bus.

CANSDAH (Pin 2): High Level CAN Bus Line. Carries the I^2C data bus.

CANSCLH (Pin 4): High Level CAN Bus Line. Carries the I^2C clock bus.

CANSCLL (Pin 5): Low Level CAN Bus Line. Carries the I^2C clock bus.

GND (Pin 3 and Exposed Pad): Ground. Solder the exposed pad and pin directly to the ground plane.

V_{IN} (Pin 6): Input Voltage Supply. This pin is the power supply input to the LDO. It must be locally bypassed with a 1µF filter capacitor to GND as close to the pin as possible. If the LDO function is unused, tie V_{IN} to V_{CC}.

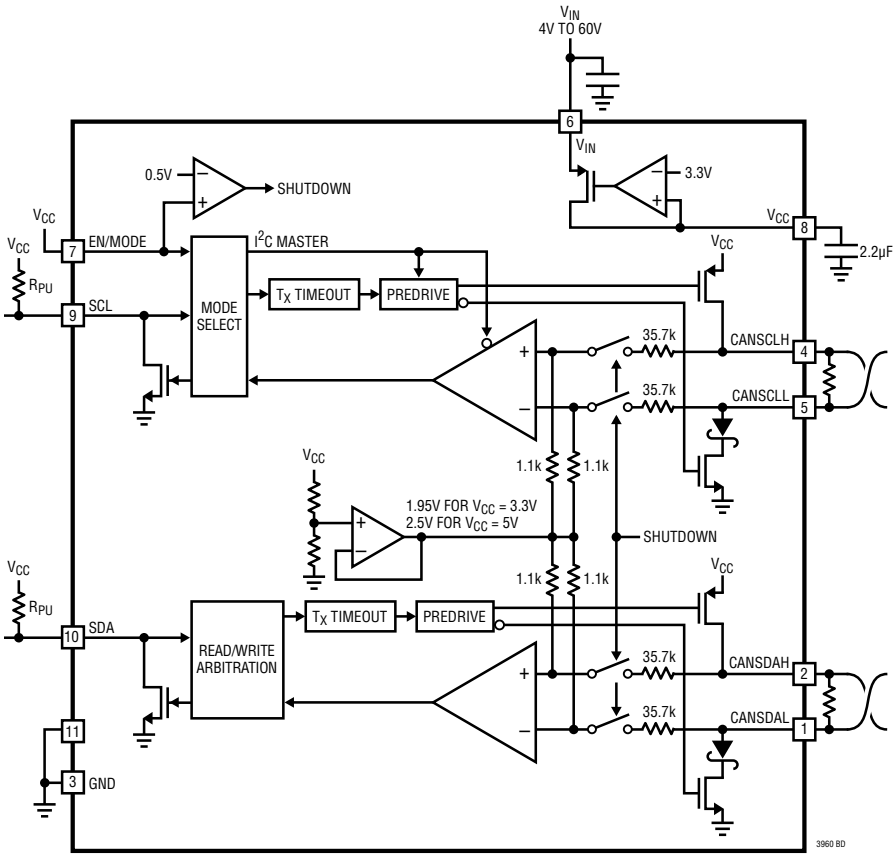
EN/MODE (Pin 7): MODE/Shutdown pin. Tie above 2.5V to select master mode, float pin to select slave mode, or pull this pin to ground for low-power shutdown mode.

V_{CC} (Pin 8): Low Dropout Regulator Output and Device Power Supply Input. Bypass this pin with a 2.2µF or greater capacitor to ground. Any bypass capacitors must be located as close to the pin as possible.

SCL (Pin 9): Clock Input or Output Pin for the I^2C Serial Port. When EN/MODE is 2.5V or above, the SCL pin is an input for the master clock. When EN/MODE is floating, the SCL pin is an output for data received on the CANSCLH/L pins.

SDA (Pin 10): Data Input and Output Pin for the I^2C Serial Port.

BLOCK DIAGRAM



TEST CIRCUITS

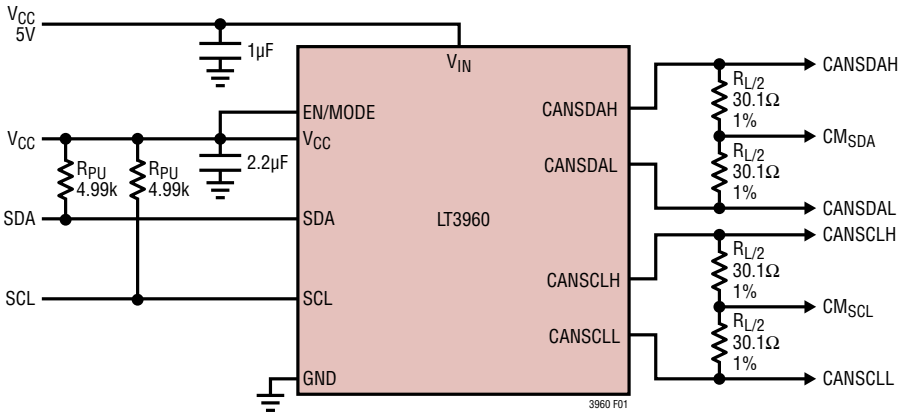


Figure 1. All Electrical Characteristic Measurements

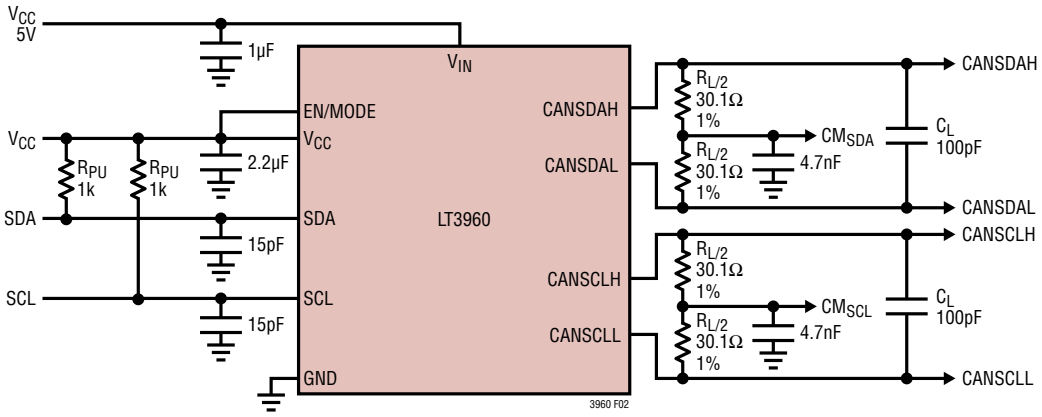


Figure 2. All Switching Characteristic Measurements

TIMING DIAGRAMS

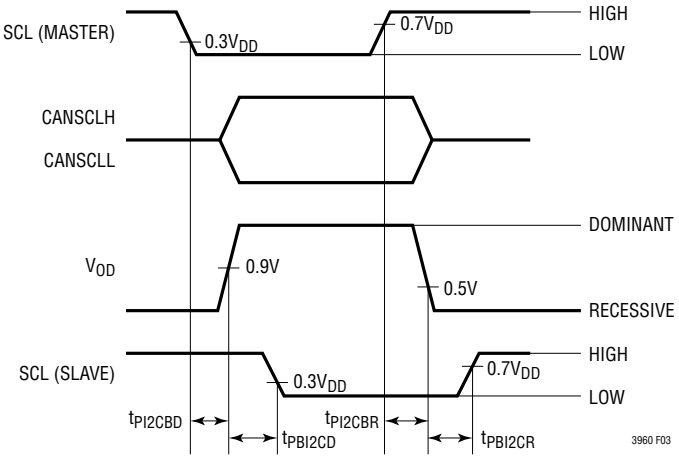


Figure 3. Transceiver Data Propagation Timing Diagram

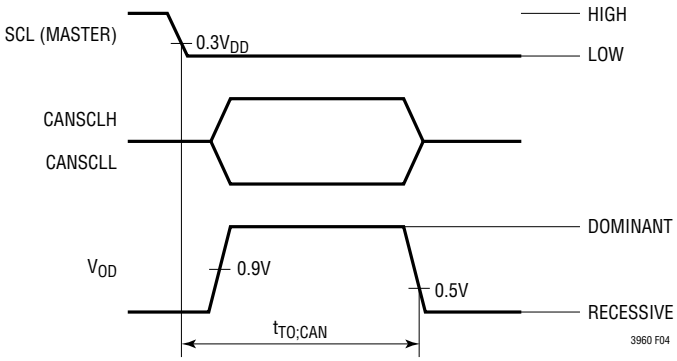


Figure 4. I²CAN Dominant Timeout

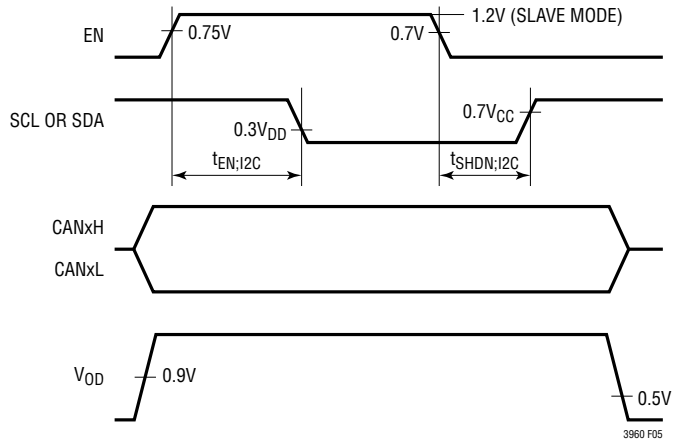


Figure 5. I²CAN Enable and Disable Times

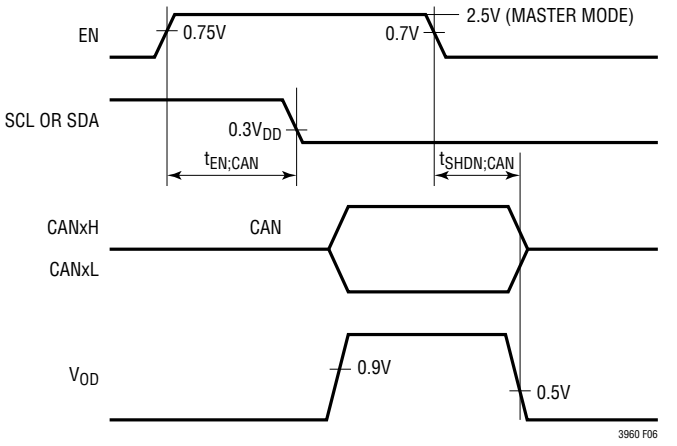


Figure 6. I²CAN Enable and Disable Times

OPERATION

The LT3960 is a high-speed transceiver which creates the functional equivalent of a single-master I²C bus in the CAN physical layer and is powered from a single wide-ranging input voltage. Using two integrated CAN transceivers, the LT3960 creates a differential proxy for each of the single-ended I²C clock and data signals which is capable of traversing harsh or noisy environments across two twisted pairs.

Each transceiver consists of a transmitter and receiver, capable of quickly converting a single-ended I²C dominant signal into a differential dominant signal, and vice versa. The transmitter is a current-regulated differential driver that generates a differential voltage between the CANxH and CANxL pins determined by drive current and the equivalent resistive load on the CANx bus. Common-mode voltage of the CANx bus is regulated by the transmitter when driving dominant as described in the applications section. The receiver is a CAN compatible differential receiver with a wide common-mode range of ±25V or ±36V, depending on V_{CC} voltage.

In the simplest setup, two LT3960 devices are used (Figure 7). The first is connected to the I²C master (microcontroller or otherwise). The second LT3960 is connected to the first by two twisted pairs and regenerates the I²C bus locally for one or more I²C slave devices. The LT3960 devices transmit the clock signal in only one direction, from master to slave. Bidirectional communication of the data signal is always permitted.

The LT3960 contains an integrated LDO which regulates an input from the V_{IN} pin between 4V and 60V to 3.3V on the V_{CC} pin from which the transceivers and bus lines are powered. Alternatively, the LT3960 can by powered from a supply voltage of 3.3V or 5V on V_{IN}, bypassing the LDO by shorting V_{CC} to V_{IN}.

The EN/MODE pin is used to put the LT3960 in low power shutdown mode and selects between Master and Slave modes of operation when enabled. When the EN/MODE pin is below 0.7V, (typical) the LT3960 is in shutdown mode, disabling both the LDO and transceivers. When V_{IN} is powered, floating the EN/MODE pin or driving it between 0.7V and 2.0V (typical) enables the LDO and sets the transceiver in Slave Mode. An EN/MODE voltage above 2.0V (typical) with V_{IN} is powered sets the LT3960 in Master Mode.

Bidirectional communication is supported on the data channel (SDA and CANSDA) regardless of the mode of operation. Communication on the clock channel (SCL and CANSCL) is unidirectional, with the direction determined by the selected mode of operation. In Slave Mode, an LT3960 only communicates clock signals from the CANSCL bus to the SCL bus. Any LT3960 connected to slave I²C devices should be operated in Slave Mode. In Master Mode, an LT3960 only communicates clock signals from the SCL bus to the CANSCL bus. The LT3960 connected to the I²C master device should always be operated in Master Mode. Regardless of the number of LT3960 devices tied to a I²CAN bus in a given application, exactly one will operate in Master Mode, driving the clock signal to the I²CAN bus and, ultimately, to all I²C slave devices. The LT3960 does not support multi-master I²C systems.

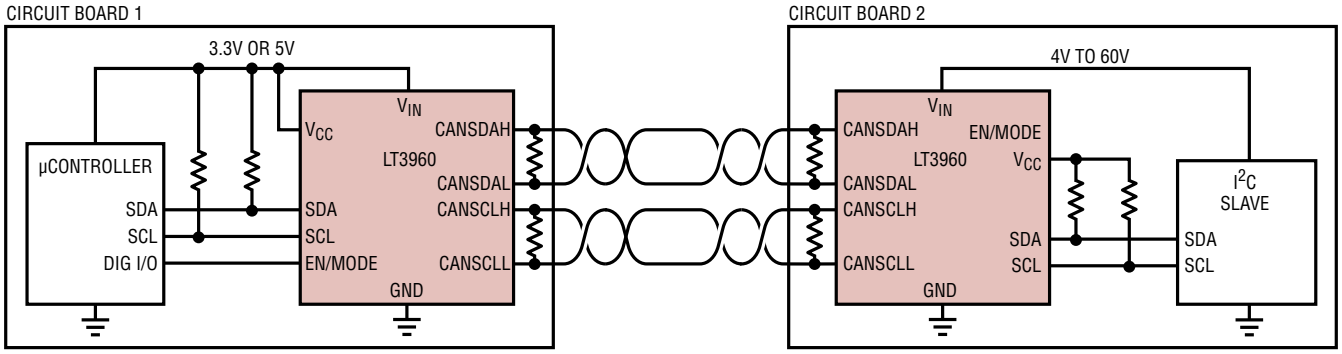


Figure 7. Simple Single-Slave Application

OPERATION

Data Transmission Detail

The timing diagram in Figure 8 shows how a byte of data is sent by the I²C master and acknowledged by the I²C slave in the single-master single-slave system described in Figure 7. The I²C master issues a start command to initiate a communication frame. The LT3960 connected to the master drives the CANSCL and CANSDA buses dominant in response to the change in state on the SCL and SDA pins without interpretation or delay. The LT3960 connected to the I²C slave receives the dominant signals on the CANSCL and CANSDA buses and drives the slave SCL and SDA pins dominant without interpretation or delay. The result on the slave I²C bus is an I²C Start command nearly identical to that generated by the master, delayed by propagation delays of the master LT3960, twisted pairs, and slave LT3960.

As additional clock and data edges are written by the I²C master, they too are recreated, first on the CANSCL and CANSDA buses and then on the slave I²C bus. Once the entire byte of data is written on the slave I²C bus, the I²C slave device issues an ACK, pulling down SDA to acknowledge receipt of a valid byte. The slave LT3960 recognizes that a slave I²C device is driving the SDA line dominant and switches from receiving to transmitting to drive the CANSDA bus dominant. The master LT3960 then receives the ACK on the CANSDA bus and pulls the master SDA low, communicating the ACK to the master.

Note that clock data is always transmitted from master to slave, but the LT3960 dynamically switches the direction of SDA communication based primarily on the time of arrival of dominant signals on its inputs.

Bidirectional Arbitration of SDA

The LT3960 facilitates bidirectional SDA communication between master and slave I²C devices by dynamically controlling the direction of traffic between SDA and the CANSDA bus. The primary factor determining the direction of communication is the time of arrival of dominant signals on SDA and CANSDA. The first of SDA and CANSDA to be asserted dominant by an external device will cause the LT3960 to drive the other dominant, establishing the direction of communication until it is released and returns to a recessive state. The transmitter which opposes the established direction of communication will be blocked until it can be safely re-enabled without locking up a bus or misinterpreting the direction of communication. To fully describe the method of arbitration, communication in each direction is described in detail below.

In the default state, SDA and CANSDA are in a recessive state and no direction of communication is set. If SDA is asserted dominant (low) by an external I²C device from a default state, the LT3960 will drive CANSDA dominant and the LT3960's receiver on CANSDA is blocked from driving SDA. When the SDA line is eventually released by the external I²C device and returns to a recessive state, the LT3960 stops driving the CANSDA bus dominant. After allowing the CANSDA bus sufficient time to return to a passive state as required by the CAN physical layer specifications, the LT3960 reopens the possibility of bidirectional traffic and waits for a dominant signal on SDA or CANSDA to once again set a direction for communication.

If, from the default state, CANSDA is asserted dominant by another LT3960 on the bus while SDA remains recessive (high), the LT3960 will drive SDA dominant (low) and the CAN transmitter is blocked from driving CANSDA based on its input while CANSDA is held dominant. When the CANSDA bus returns to a recessive state, the LT3960 stops driving the other dominant. When it is safe to do so without causing glitches or latch up, the LT3960 reopens the possibility of bidirectional traffic and waits for a dominant signal on SDA or CANSDA to once again set a direction for communication.

OPERATION

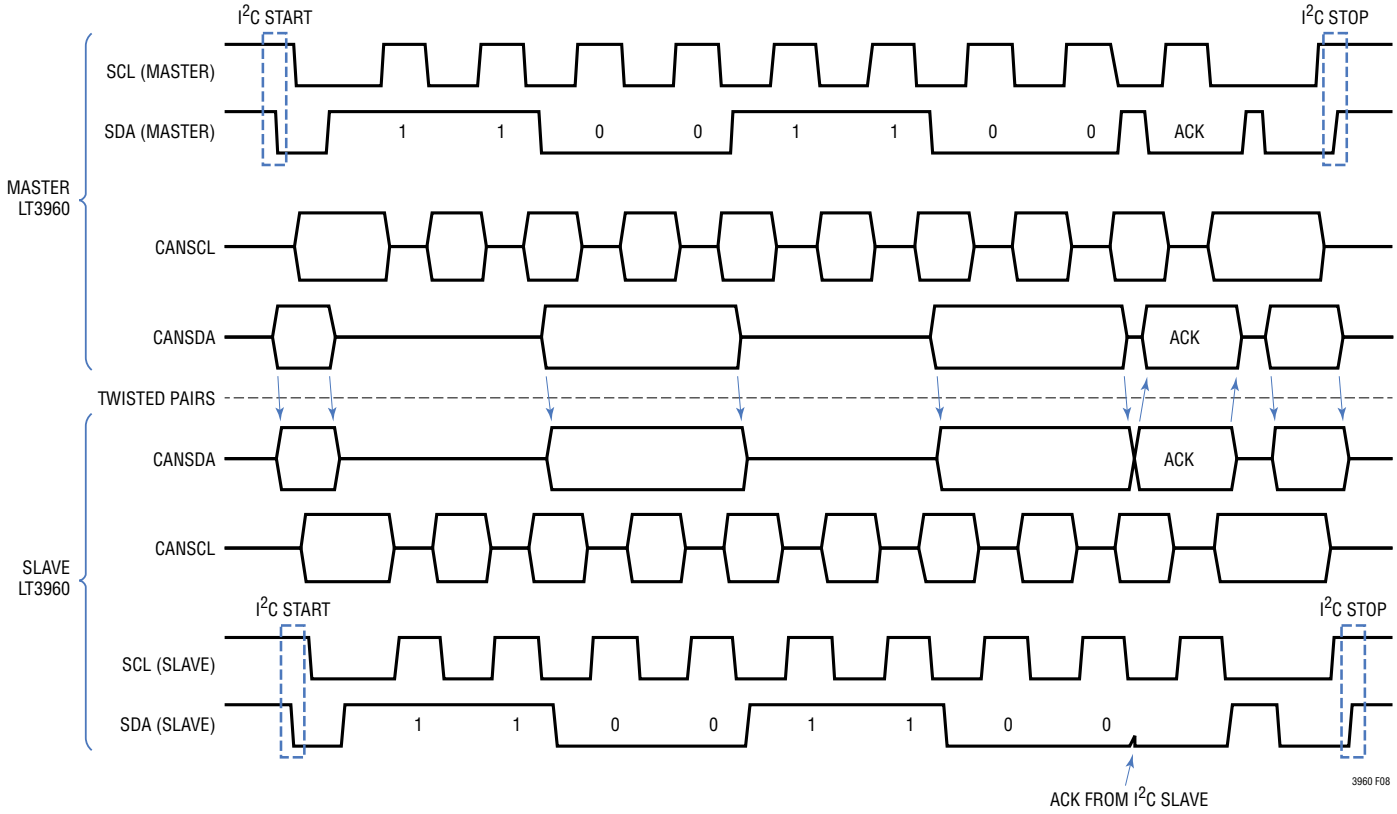


Figure 8. Simple Single-Slave Application

APPLICATIONS INFORMATION

Supply Voltage Ranges

The LT3960 can be operated with or without using its internal LDO. Tying V_{IN} to V_{CC} and powering directly from a 3.3V or 5V supply will bypass the LDO. With a 5V supply on V_{CC}, transmitter common-mode voltage and receiver common-mode input range are increased from their 3.3V values. In this configuration, an internal comparator monitors the supply voltage and switches internal reference voltages and output drive strengths at approximately 4.1V. Operation with a supply between 3.6V and 4.5V is not recommended, because of the discontinuity in the internal voltages at this switch point.

When using the internal LDO to generate the 3.3V bus supply on V_{CC}, any V_{IN} supply voltage between 4V and 60V is allowed. In this configuration, the switch point mentioned above is avoided since V_{CC} is regulated to a fixed 3.3V.

An LT3960 operating with a V_{CC} at 5V may share an I²CAN bus with an LT3960 operating with V_{CC} at 3.3V. However, the fluctuation in common mode voltage between 1.95V (when an LT3960 with V_{CC} = 3.3V is dominant) and 2.5V (when an LT3960 with V_{CC} = 5V is dominant) may increase electromagnetic emissions.

Master and Slave Mode Configurations

The LT3960 connected to the I²C master must be operated in Master Mode, with the EN/MODE pin driven greater than 2.5V. When operating in Master Mode, it is recommended that V_{CC} be tied to V_{IN} and driven from a bus voltage of 3.3V or 5V. Additionally, EN/MODE should be driven from a digital output pin from the I²C Master as shown below. In this configuration, EN/MODE can be held low until the V_{CC} cap is fully charged.

Do not tie the EN/MODE pin directly to V_{CC} when operating in Master Mode. With EN/MODE and V_{CC} shorted, every power-up sequence will set the LT3960 into slave mode for many microseconds while the V_{CC} capacitor charges between the enable threshold and the Master Mode threshold.

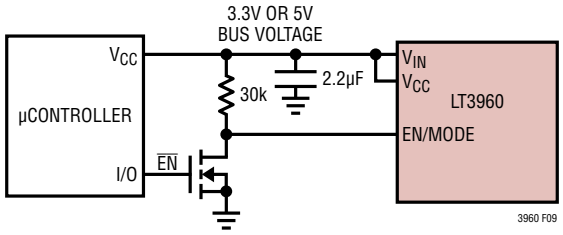


Figure 9. Recommended Master Mode Power Setup

An LT3960 connected to slave I²C devices must be operated in Slave Mode, with the EN/MODE pin between 0.7V and 2V. When left floating, the EN/MODE pin will pull up to approximately 1.2V, enabling the LT3960 and setting it in Slave Mode, whenever the V_{IN} pin is powered above approximately 2V. It is recommended that the EN/MODE pin be left floating for Slave Mode LT3960 devices, regardless of whether the internal LDO is employed.

LT3960 and Standard CAN Transceivers

It should be noted that while the LT3960 uses the CAN physical layer to conduct bidirectional I²C data, the CANSCL and CANSDA buses created by the LT3960 are not traditional CAN buses carrying traditional CAN data. As such, the CANSCL and CANSDA buses between LT3960 devices cannot be shared with standard CAN transceivers in a multidrop configuration.

±40V Fault Protection

The LT3960 provides ±40V fault protection on the I²CAN interface pins (CANSCLH, CANSCLL, CANSDAH, CANSDAL), allowing I²C communication in applications where it was previously impractical. Addressing the need the overvoltage tolerance in many industrial and automotive applications, the driver outputs use a progressive foldback current limit to protect against overvoltage faults while still allowing high current output drive. The LT3960 is protected from ±40V faults powered or unpowered, even in the case of V_{CC} open or shorted to ground. When V_{CC} is open or shorted to GND, the transceivers are off and the I²CAN bus pins remain in the high impedance state.

APPLICATIONS INFORMATION

±36V Extended Common-Mode Range

The LT3960 receiver features an extended common mode range of -36V to 36V when operating from a 5V V_{CC} and -25V to 25V when operating from a 3.3V V_{CC}. The wide common mode increases the reliability of operation in environments with electrical noise or local ground potential differences due to ground loops. This extended common mode range allows the LT3960 to conduct I^2C communication in environments inhospitable to standard I^2C, such as between two distant PCBs in an automobile.

I^2CAN Driver

When the SCL or SDA pin is asserted low by external I^2C device and the conditions are met (whether by mode selection or bidirectional arbitration) to propagate this data from I^2C to CAN, the I^2CAN driver asserts the dominant state on the corresponding bus lines; the CANxH driver pulls high and the CANxL driver pulls low. When the SCL or SDA pin is high under these same conditions, the I^2CAN driver is in the recessive state; both the CANxH and CANxL drivers are in the high impedance state and the bus termination resistor equalizes the voltage on CANxH and CANxL. In the recessive state, the impedance on CANxH and CANxL is determined by the receiver input resistance, R_{IN}. When EN/MODE is low or the V_{CC} is in UVLO, the LT3960 is in shutdown; all I^2CAN drivers are in the high impedance state, and the receiver input resistance R_{IN} is disconnected from the bus by a FET switch.

Transmit Dominant Timeout Function

Both transceivers in the LT3960 include a 1.5ms (typical) timer to limit the time that driver can hold the I^2CAN bus in the dominant state. For example, if the SCL line is held low in Master Mode, a dominant state is asserted on the CANSCL bus until the timer expires, after which the driver releases the bus to a recessive state. The timer is reset when SCL is brought high.

I^2CAN Driver Overvoltage, Overcurrent, and Overtemperature Protection

The I^2CAN driver outputs are protected from short circuits to any voltage within the absolute maximum range of -40V to 40V. The maximum current on I^2CAN interface pins in a fault condition is ±150mA. The drivers include a progressive foldback current limiting circuit that continuously reduces the driver current with increasing output fault voltage. The fault current is typically ±2mA for faults at the absolute maximum voltages of ±40V.

The LT3960 also features thermal shutdown protection that disables the chip in the case of excessive power dissipation from the drivers. When the die temperature exceeds 168 ° C (typical), the LT3960 is forced into shutdown mode and the I^2CAN drivers enter a high impedance state.

Power-Up/Down Glitch-Free Outputs

The LT3960 employs an undervoltage monitoring circuit on the V_{CC} supply to control the activation of the transceiver circuitry. During start-up SDA, SCL, and all I^2CAN outputs are in a high impedance state until V_{CC} reaches a voltage sufficient to reliably operate the chip. At this point, if EN/MODE is out of its shutdown region, the chip activates. The CANSCL and CANSDA receivers activate after a short delay $t_{EN;I2C}$ allowing SCL or SDA to follow the state of CANSCL or CANSDA. The CANSCL and CANSDA drivers power up in the transmit dominant timeout state regardless of the state of SCL or SDA and remain in the recessive state until the first high to low transition of SCL or SDA, respectively. This assures that the LT3960 does not disturb the I^2CAN bus by glitching to the dominant state during start-up.

During power-down, similar protection exists. When the undervoltage detection circuit senses low supply voltage on V_{CC}, it immediately puts the chip into shutdown. All I^2C and I^2CAN pin outputs go the high impedance state.

APPLICATIONS INFORMATION

Passive Leakage on I²CAN Bus Pins

When the power supply is removed or the chip is in shutdown, the I²CAN pins are in a high impedance state. The I²CAN receiver inputs are isolated from the CANxH and CANxL pins by FET switches which open in the absence of power, preventing the resistor dividers on the receiver inputs from loading the bus. The high impedance state of I²CAN pins is maintained over a range determined by the ESD protection of the pins, typically -0.3V to 7V. For bus voltages outside this range, the current flowing into the receiver is governed by the conduction voltages of the ESD device and the 35.7k nominal I²CAN receiver input resistance.

I²CAN Bus Termination

I²CAN buses must be terminated at the ends of each twisted pair with a 120Ω resistor. Split termination is an optional termination technique to reduce common mode voltage perturbations that can produce EME. A split terminator divides the single line-end termination resistor (nominally 120Ω) into two series resistors of half the value of the single termination resistor (Figure 10).

The center point of the two resistors is connected to a 4.7nF capacitor. Split termination suppresses common mode voltage perturbations by providing a low impedance load to common mode noise sources such as transmitter noise or coupling to external noise sources. In the case of single resistor termination, the only load on a common mode noise source is the parallel impedance of the input resistors of the I²CAN transceivers on the bus. This results in a common mode impedance of several kΩ for a small network. The split termination, on the other hand, provides a common mode load equal to the parallel resistance of the two split termination resistors (30Ω). This low common mode impedance results in a reduction of the common mode noise voltage compared to the much higher common mode impedance of the single resistor termination. Figure 11 and Figure 12 compare the common mode noise of an application with and without split cap termination.

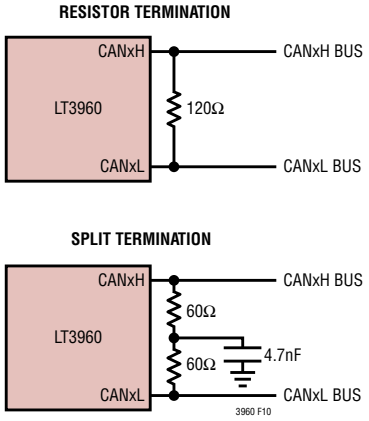


Figure 10. Split Termination for Improved Common Mode Behavior

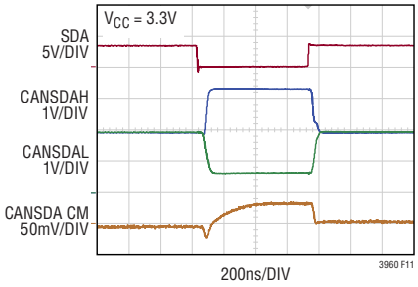


Figure 11. I²CAN Common Mode Noise (4.7nF Split Cap)

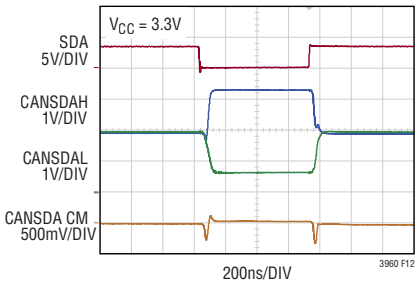


Figure 12. I²CAN Common Mode Noise (No Split Cap)

APPLICATIONS INFORMATION

Multidrop Applications

The LT3960 can be used in a multidrop setup, employing multiple slave-mode LT3960's to generate multiple local I²C buses on multiple PCBs along the length of the I²CAN bus lines. No additional termination is required in a multidrop system, but some care must be taken in the design of such systems. The stub length, or the distance from twisted pairs to any additional LT3960, should be less than 0.3m. Stub lengths to the CANSDA and CANSCL buses should be as close as possible in length to avoid adding unequal transmission delays to the clock and data signals.

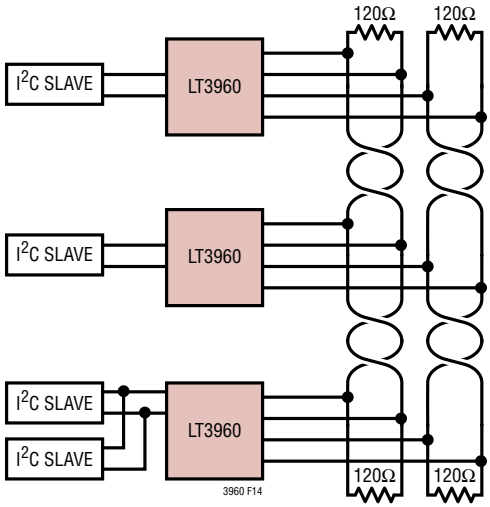


Figure 13. Multidrop Setup

Maximum Data Transmission Rate

Successful communication in any I²C application is dependent on slave I²C devices' timely acknowledgment (or ACK) upon receiving a byte of data. Specifically, I²C slaves must assert the SDA line after the eighth clock pulse leaving enough setup time before the ninth rising edge of SCL to guarantee that the ACK will be received by the I²C master. This requirement is straightforward when all I²C devices share the same I²C bus, but in LT3960 applications where master and slave I²C buses are separated by various propagation delays, extra care must be taken to ensure that ACKs from slave I²C devices will be received by the I²C master at the desired transmission rate. In LT3960 applications, the SCL low period between successive clock pulses (t_{LOW})must be less than the sum of the propagation delays (t_{PI2CBD} and t_{PBI2CD}), slave ACK time ($t_{VD;ACK}$), and master data setup time ($t_{SU;ACK}$). This requirement is shown explicitly in Equation 1.

$$t_{LOW} > 2\left(t_{PI2CBD,max} + t_{CABLE} + t_{PBI2CD,max}\right) + t_{VD;ACK,max} + t_{SU;ACK} \quad (1)$$

A conservative estimate of propagation delay through a twisted pair based on cable length is shown in Equation 2. Equation 2 is useful for rough estimates, but when designing applications always calculate propagation delay based on the actual physical properties of the cabling used for the I²CAN bus lines.

$$t_{CABLE} = \frac{l_{CABLE}}{0.15m/ns} \quad (2)$$

Fast-mode (400kHz capable) I²C devices are allowed 0.9µs to acknowledge a valid data byte, even while ACK times ($t_{VD;ACK}$) are often much shorter in practice. A $t_{VD;ACK}$ of 0.9µs would limit the data transmission rate of a LT3960 application to under 400kHz for even one meter of twisted pair. For this reason, it is recommended that all I²C slaves be Fast-mode Plus (1MHz) devices instead of Fast-mode (400kHz) devices when attempting to maximize transmission rate. The shorter maximum $t_{VD;ACK}$ (450ns) of Fast-mode plus devices allows for communication across a greater distance at any given clock speed. Figure 14 consolidates the information above, plotting maximum clock speeds for a given bus length for applications with fast-mode and fast-mode plus devices.

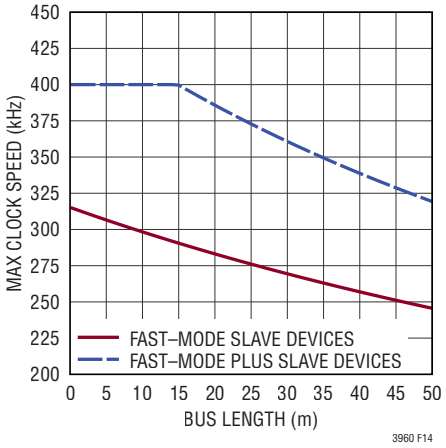
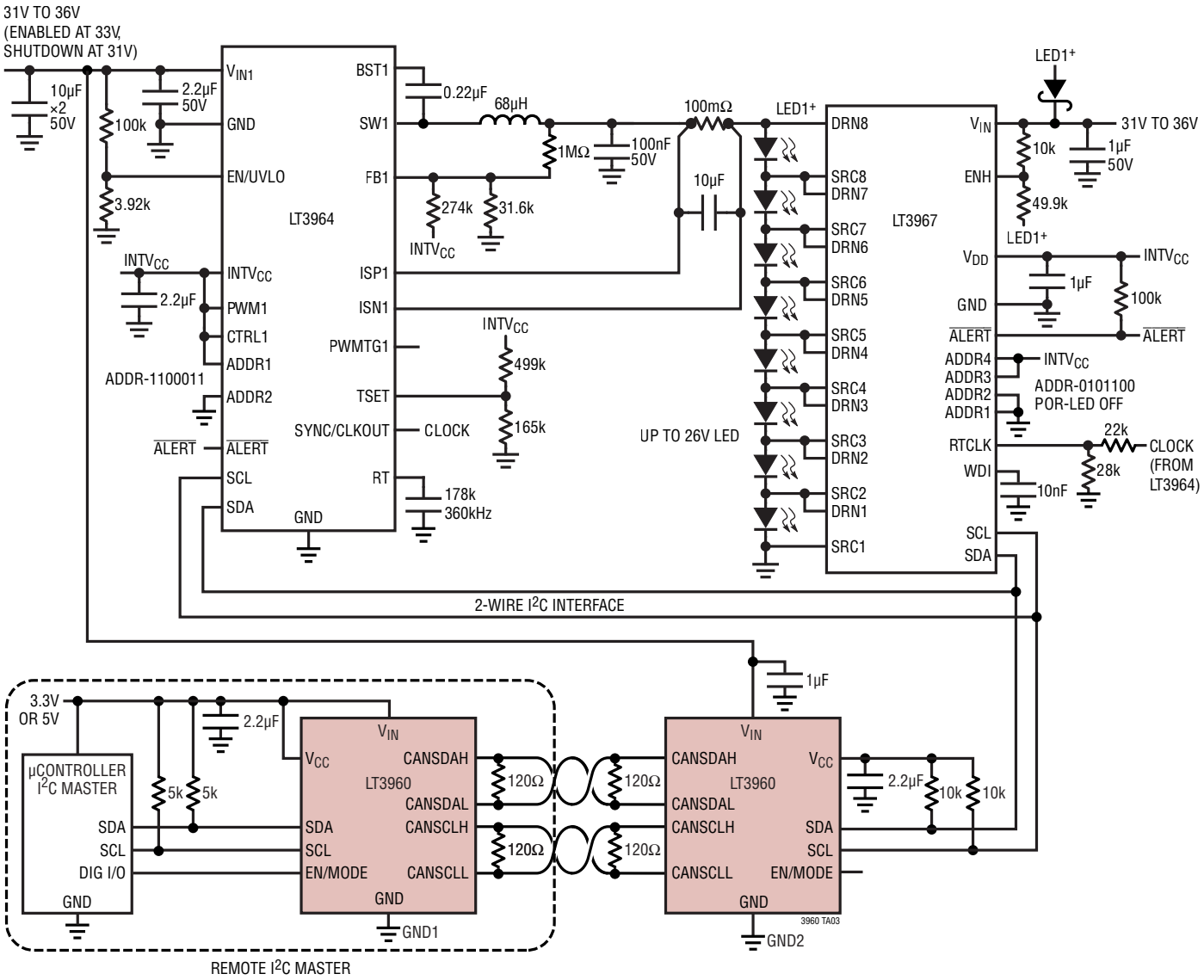


Figure 14. Maximum I²CAN Clock Speed

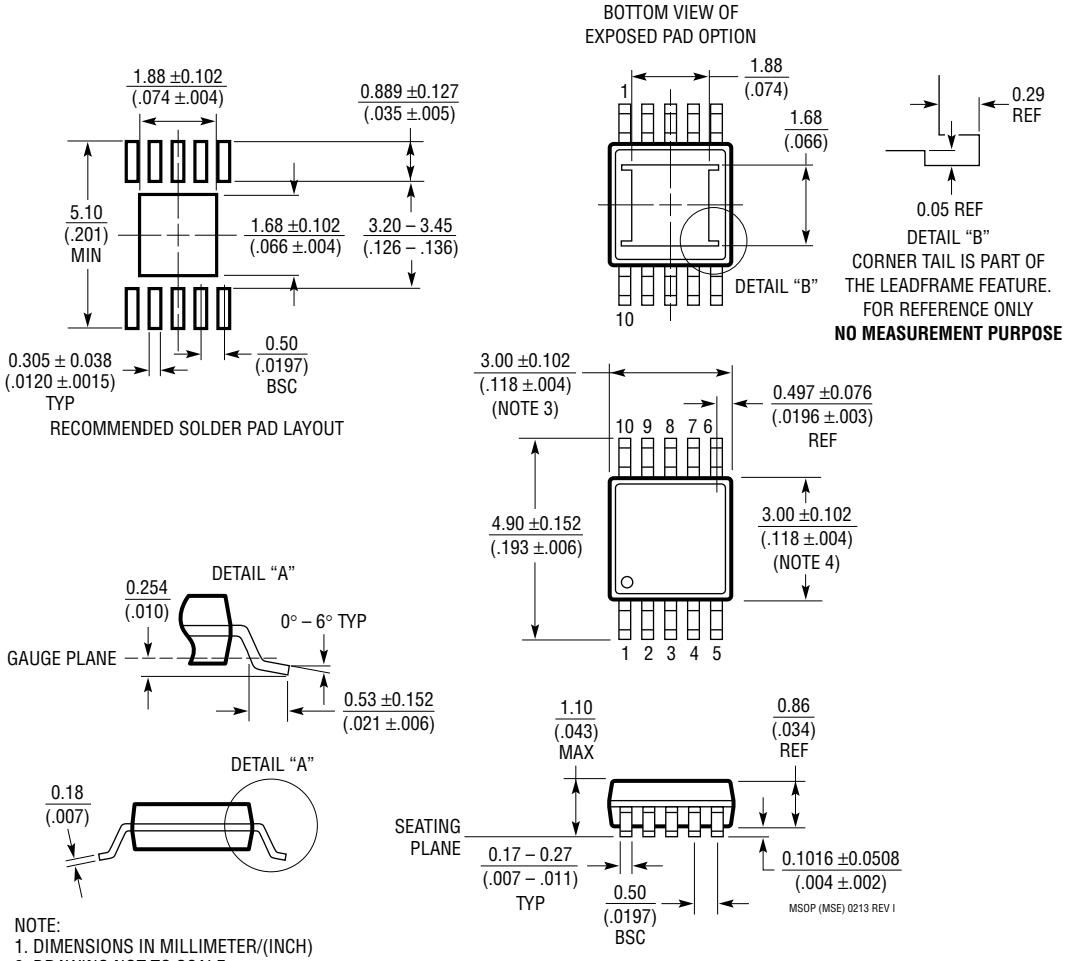
TYPICAL APPLICATIONS

1A Matrix LED Dimmer with Remote I²C Control



PACKAGE DESCRIPTION

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



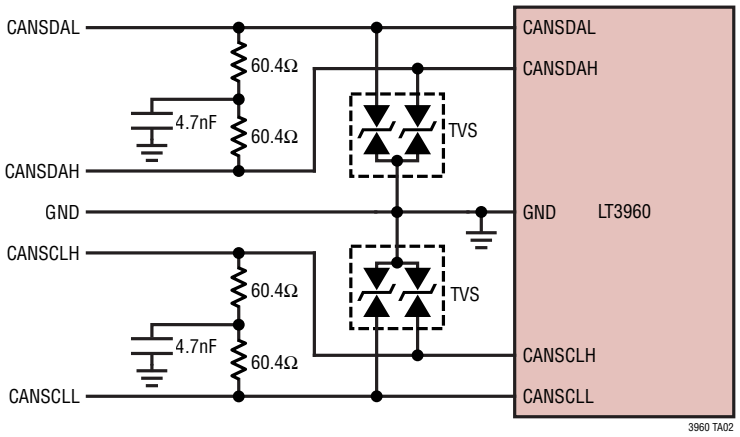
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/21	Changed topmark from LHJP to LTHJP.	2
B	10/21	Removed ESD rating. Updated TVS circuit.	1, 16, 22

TYPICAL APPLICATION

Network for IEC 6100-4-2 Level 4 ESD Protection



TVS: ON SEMI NUP2105L, 350W DUAL BIDIRECTIONAL TVS DIODE, SOT-23

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3965	8-Switch Matrix LED Dimmer	I^2C Multidrop Serial Interface, 16 Unique I^2C Addresses, V_{DD} Range: 2.7V to 5.5V, V_{IN} Range: 8V to 60V, Digital Programmable 256:1 PWM Dimming, 28-Lead TSSOP
LT3967	1.3A Eight-Switch Matrix LED Dimmer with CRC-8	Controls LED Dimming of Strings Up to 54V, I^2C Serial Interface with Programmable Address, 28-Lead TSSOP
LT3964	Dual 36V Synchronous 1.6A Buck LED Driver with I^2C	Wide Input Voltage Range: 4V to 36V, Two Independent 1.6A/40V Synchronous Bucks, I^2C Interface for Internal True Color PWM™ Dimming (8192:1), 36-Lead QFN
LTC4331	I^2C Slave Device Extender Over Rugged Differential Link	Up to 1MHz Serial Clock, Fast-Mode Plus (FM+), Selectable Link Baud Rates Extend I^2C Up to 1200m, 20-Lead QFN