Scope

The present specifications shall apply to a 3 phase brushless motor driver IC, SI-6633M.
The present specifications shall apply to SI-6633M which is performed RoHS instructions.

Outline

Type	Monolithic integrated circuit
Structure	Plastic molded (transfer mold)
Applications	3 phase brushless motor driver (Trapezoidal Current Control.)

Absolute maximum ratings

Items	Symbol	Condition	Limit	Unit
Power supply voltage	V_{BB}		38	V
Output voltage	V_{OUT}		V_{BB}	V
Output current (※)	$I_{OUT(Ave)}$		±2	A
	$I_{OUT(Peak)}$	tw<500msec/Duty<10%	±4	A
Logic input voltage	$V_{IN(Logic)}$		-0.3~5.5	V
Analog voltage	$V_{IN(Analog)}$		-0.3~6	V
Sense voltage	V_{SENSE}		±0.5	V
Power dissipation	PD	SK evaluation board	2.9	W
Junction temperature	T_J		150	℃
Storage temperature	T_{stg}		-40~150	℃
Ambient temperature	T_A		-20~85	℃

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking.
Under any set of conditions, do not exceed the specified junction temperature (T_j).

Peak current is guaranteed by design.

Electrical characteristics

Recommendable Operating Range

Item	Symbol	Limit	Unit	Remark
Power supply voltage	V_{BB}	10 to 30	V	Normal operation
Logic input voltage	$V_{IN(Logic)}$	0 to 5.5	V	
Analog input voltage	$V_{IN(Analog)}$	0 to 5.5	V	Except for Ref pin
Ref input voltage	V_{Ref}	0.5 to 5.5	V	Current accuracy is going down under 0.5V.
Sense voltage	V_{SEN}	±0.5	V	
Package temperature	T_C	105	℃	
Ambient temperature	T_A	-20 to 85	℃	

Especially, care should be taken with output current on condition over recommendation range and below absolute max rating. In this case, enough evaluation is needed with thermal design data below and application note to avoid the device being over absolute max rating for other item.

Electrical Characteristic (T_a=25°C, V_{BB}=24V, V_{DD}=5V, Unless Otherwise Noted.)

Item	Symbol	Limit			Unit	Condition	
		Min.	Typ.	Max.			
Power supply voltage range	V_{BB}	10	-	V_{BBOV}	V	Motor operation	
Charge pump voltage	V_{CP}	6	7.5	9	V	Output disable, VCP-VBB voltage	
Charge pump frequency	f_{CP}	90	120	150	kHz		
Power supply current	I_{BB}	5	10	15	mA	Output disable	V_{BB}=38V
	I_{BBSTBY}	-	100	500	μA	V_{STBY}=2.5V	
Output leak current	I_{OLKL}	-200	-100	-50	μA	V_{BB}=38V、V_{OUT}=0V	
	I_{OLKH}	50	100	200	μA	V_{BB}=V_{OUT}=38V	
MOSFET ON resistance	$R_{DS(on)}$	0.1	0.2	0.3	Ω	I_{DS}=2.0A、S pin connected to GND	
Body diode forward voltage	V_{SD}	0.8	1.1	1.4	V	I_{SD}=2.0A	
STBY pin input voltage	V_{STBYL}	0	-	0.8	V		
	V_{STBYH}	2.5	-	V_{DD}	V		
	ΔV_{STBY}	0.1	0.25	0.4	V	Hysteresis	
STBY pin input current	I_{STBYL}	0	±1	±10	μA		
	I_{STBYH}	20	50	100	μA	V_{STBY}=5V	
Logic input voltage	V_{INPL}	0	-	0.8	V		Enable、Brake、Dir、SRMD、Decay、PWM
	V_{INPH}	3.5	-	V_{DD}	V		
	ΔV_{INP}	1	1.5	2	V	Hysteresis	
Logic input current	I_{INPL}	0	±1	±10	μA	V_{IN}=0V	
	I_{INPH}	0	±1	±10	μA	V_{IN}=5.5V	
REF pin input current	I_{REF}	-5	-0.5	1	μA	V_{REF}=0 to 5.5V	
REF pin input current	V_{REF}	0.5	-	5.5	V		
SEN pin input current	I_{SEN}	0	±2.5	±10	μA	V_{SEN}=0 to 0.5V	
Current sensing divider ratio	V_{SEN}/V_{REF}	-10	-	10	%	V_{REF}=5.5V	
Current sensing filter time	t_{LPFSEN}	0.6	1.8	3	μs		
CPWM pin threshold voltage	V_{CPWML}	1.1	1.5	1.9	V		
	V_{CPWMH}	3	3.5	4	V		
CPWM pin frequency	f_{CPWM}	15	25	35	kHz	C_{PWM}=1000pF	
CLD pin frequency	f_{CLD}	54	64	74	Hz	C_{LD}=0.1μF	
Power supply voltage range	V_{BB}	10	-	V_{BBOV}	V	Motor operation	
Charge pump voltage	V_{CP}	6	7.5	9	V	Output disable, VCP-VBB voltage	
Charge pump frequency	f_{CP}	90	120	150	kHz		
AIN pin input current	I_{AIN}	-1	-0.5	1	μA	AINP、AINN pin, V_{AIN}=0 to 5.5V	
AOUT pin threshold voltage	V_{AOENA}	-	1.2	V_{CPWML}	V	AOUT pin voltage rising	
	$V_{AOENAhys}$	0.05	0.1	0.15	V	Hysteresis	Guaranteed by design
AOUT pin max output voltage	V_{AOUTH}	V_{CPWMH}	4	4.45	V	Output PWM operating	
AOUT pin input voltage range	V_{AOUTEI}	4.5	-	5.5	V	Output 100% ON	
AOUT pin max output current	I_{AOUT}	7.5	-	-	mA	V_{AOUT}=0V	
AOUT pin pull-down resistance	R_{AOUT}	25	32.5	40	kΩ	V_{AOUT}=2.5V	
FLAG pin output voltage	$V_{FLAG(ON)}$	0.1	0.2	0.5	V	I_{FLAG}=2mA	FLAG
FLAG pin leak current	$I_{FLAG(OFF)}$	0	-	20	μA	V_{FLAG}=5.5V	
FG pin output voltage	$V_{FG(ON)}$	0.1	0.2	0.5	V	I_{FG}=2mA	FG
FG pin leak current	$I_{FG(OFF)}$	0	-	20	μA	V_{FG}=5.5V	

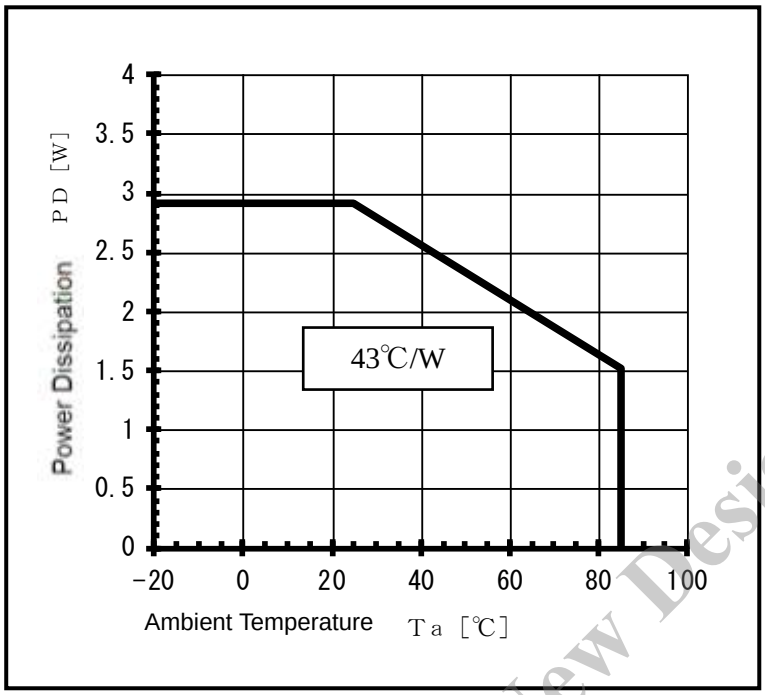
- Typ data is for reference only.
- Negative current is defined as coming out of the specified pin.

Electrical Characteristic(continued) (T_a=25°C, V_{BB} =24V, V_{DD}=5V, Unless Otherwise Noted.)

Item	Symbol	Limit			Unit	Condition	
		Min.	Typ.	Max.			
VBB under voltage lock out	V_{BBUVH}	7	7.5	9	V	VBB rising	V_{CP}= V_{BB}+7V
	$V_{BBUVhys}$	0.1	0.3	0.5	V	Hysteresis	
Over voltage threshold	V_{BBOV}	34	35	37.5	V	VBB rising	Stop operation
	$V_{BBOVhys}$	1.5	2	2.5	V	Hysteresis	
Over current detect voltage	V_{OCPLS}	1	1.3	1.5	V	OUT-GND voltage, Low side detect	
	V_{OCPHS}	0.7	1.0	1.3	V	VBB-OUT voltage, High side detect	
Over current filter time	t_{LPFOC}	-	0.6	t_{LPFSEN}	µs		
Thermal shutdown	T_{TSD}	150	165	-	°C	Temperature rising	Guaranteed by design
	ΔT_{TSD}	-	50	-	°C	Hysteresis	
Thermal alarm	T_{TA}	-	120	-	°C	Temperature rising	
	ΔT_{TA}	-	10	-	°C	Hysteresis	
Propagation delay	t_{PDON}	-	2.3	-	µs	HALL input to output ON	
	t_{PDOFF}	-	2.1	-	µs	HALL input to output OFF	
	$t_{PDPWMON}$	-	1.1	-	µs	PWM input to output ON	
	$t_{PDPWMOFF}$	-	0.9	-	µs	PWM input to output OFF	
Dead time	t_{DEAD}	100	300	800	ns		
Hall input current	I_{HALL}	-2	-0.5	1	µA	V_{IN}=0.2 to 4.2V	
Common mode voltage range	V_{CMR}	0.2	-	3.5	V		
AC input voltage range	V_{HALL}	60	-	-	mV		
Hysteresis	V_{HYS}	-	20	V_{HALL}	mV	Guaranteed by design	
Pulse reject filter	t_{pulse}	1	2	3	µs		

- Typ data is for reference only.
- Negative current is defined as coming out of the specified pin.

Power dissipation



Excitation control input (Hall and Logic input)

Truth table

Status	Input					Output status DIR=H (L)		
	HallU※1	HallV※1	HallW※1	Enable	Brake	OUTU	OUTV	OUTW
F1	+	−	+	L	H	H (L)	L (H)	Z
F2	+	−	−	L	H	H (L)	Z	L (H)
F3	+	+	−	L	H	Z	H (L)	L (H)
F4	−	+	−	L	H	L (H)	H (L)	Z
F5	−	+	+	L	H	L (H)	Z	H (L)
F6	−	−	+	L	H	Z	L (H)	H (L)
Error	−	−	−	X	H	Z	Z	Z
Error	+	+	+	X	H	Z	Z	Z
Brake	X	X	X	L	L	L	L	L
Disable※2	X	X	X	H	X	Z	Z	Z

※1 HallU、HallV、HallW ： ’+’=H+>H- 、’-’ =H+<H-

※2 There are conditions for the device to be disable

- HallU, HallV and HallW are internal logic signal made from HU+, HU-, HV+, HV-, HW+ and HW-
- Refer to “10.12 Enable and Brake” for disable operation

Stand-By pin

Truth table

STBY	Status
L	Operation mode
H	Stand-By mode

- In stand-by mode, some internal circuits are shut down with bias current being cut.

FLAG output

Truth table

Status	Fault
Normal	Output OFF (High impedance)
Fault	L

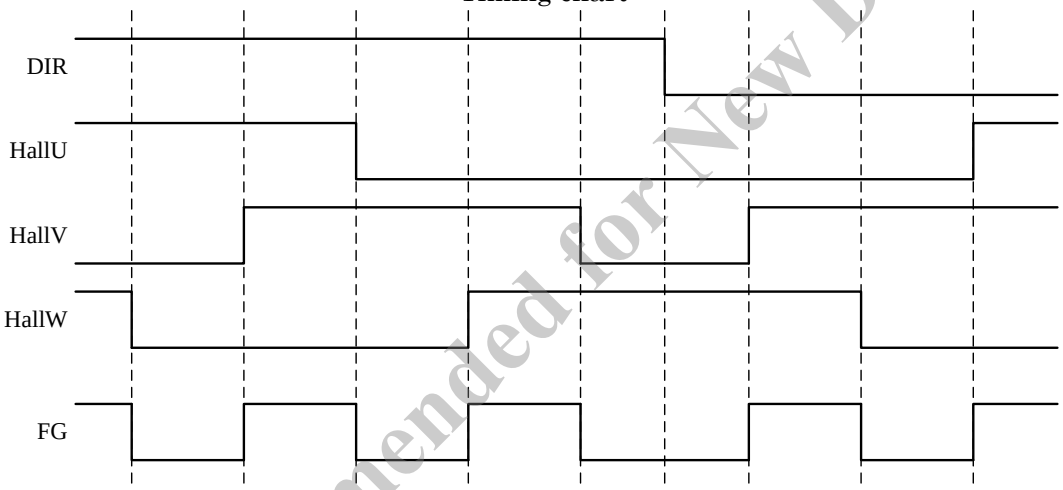
Below are the fault conditions.

① Under voltage lock out for VBB (internal regulator)
② Under voltage lock out for charge pump
③ Overvoltage
④ Thermal alarm
⑤ t_{OFFOCP} after over current detection
⑥ Lock detection

・ Please take care for FLAG output due to the internal circuit may not be fixed with VBB being low.

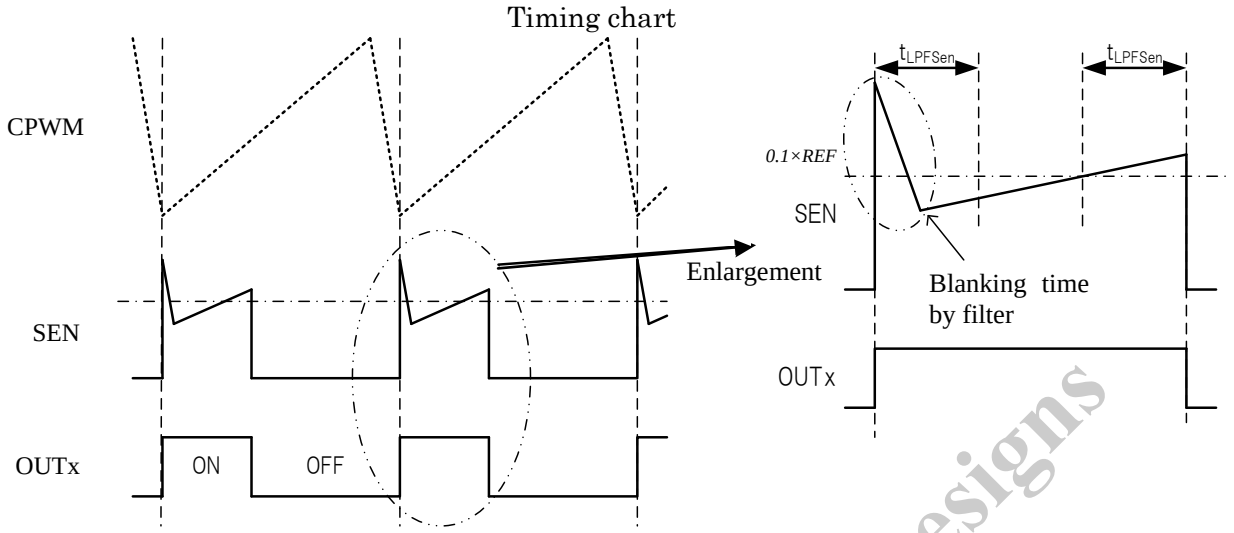
FG signal

Timing chart



・ Refer to "10.1 Hall and Logic input" on HalU, HallV and HallW
・ FG is toggled by each phase changed

Internal PWM control



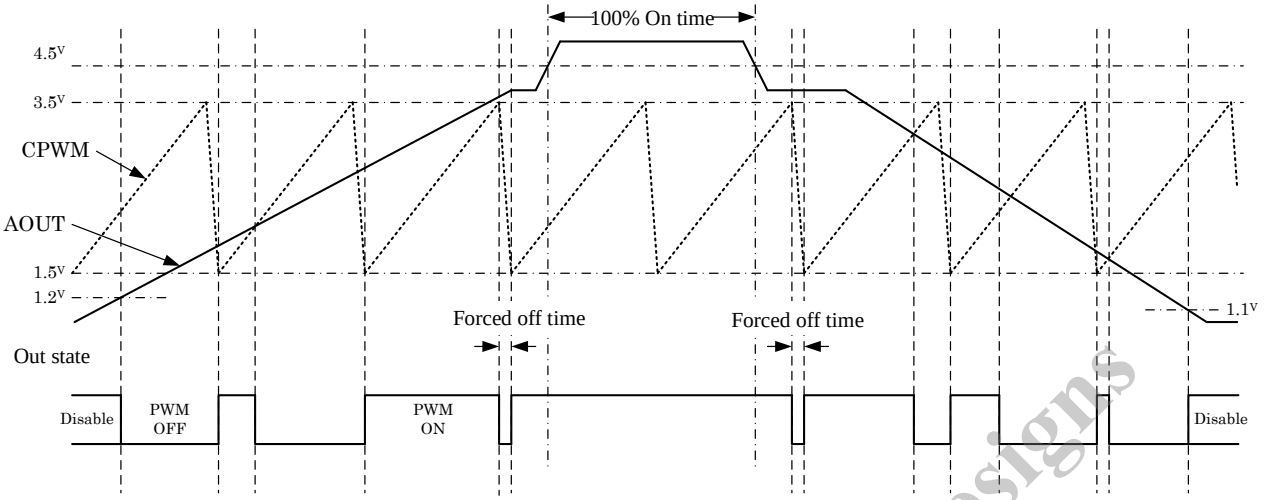
(※The value is typical in the timing chart)

- If not using this function, you should connect SEN pin to GND and put some voltage (from 1V to max in VREF voltage range) to REF pin.

. Internal PWM is active in off time, but the device has blanking time that is almost same as t_{LPFSen}.

External PWM control

Timing chart



(※The value is typical in the timing chart)

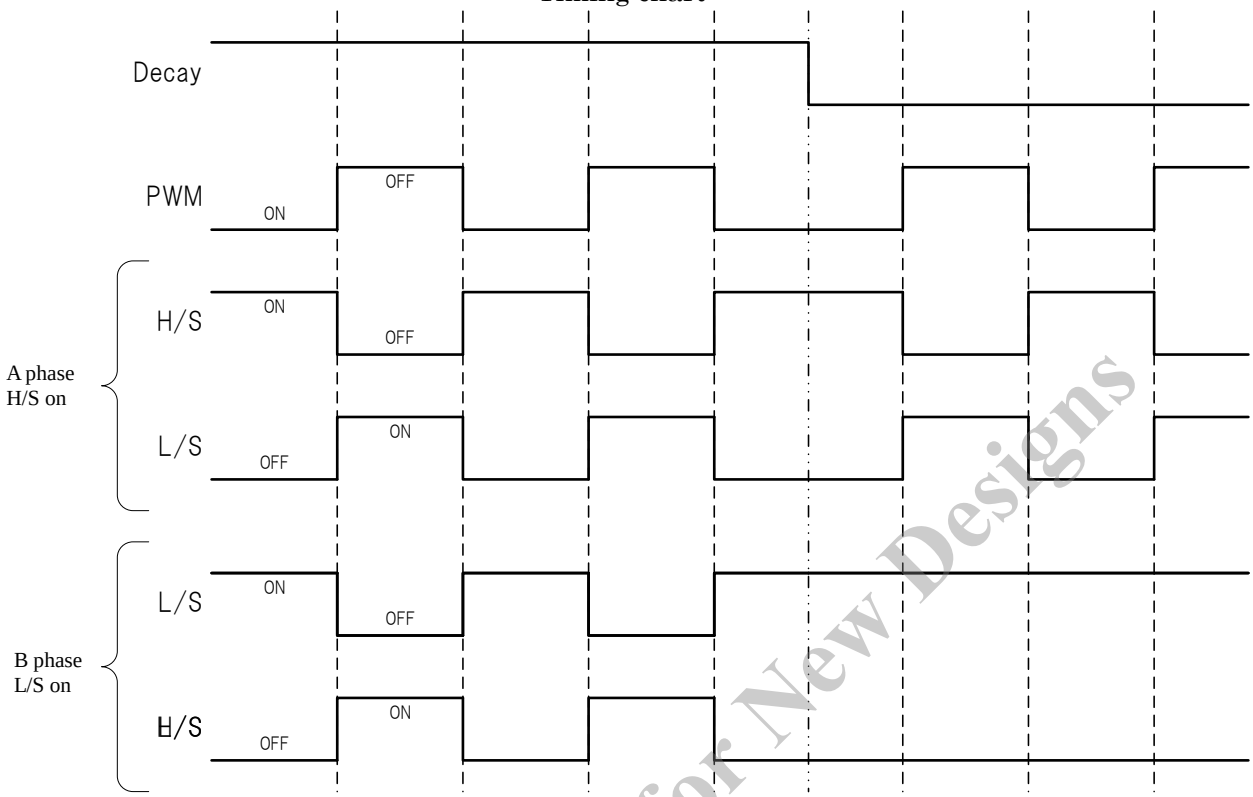
・ Outputs are disable below 1.2V (typ, the voltage rising) on AOUT pin.

・ The max duty is 95% (typ, design value) due to the forced off time. The forced off time is active even if not using this function.

・ To make 100% ON duty, you should put the external voltage over 4.5V on AOUT. However, the voltage range to make 100% ON is from 4.5V to 5.5V.

PWM control (PWM and Decay)

Timing chart



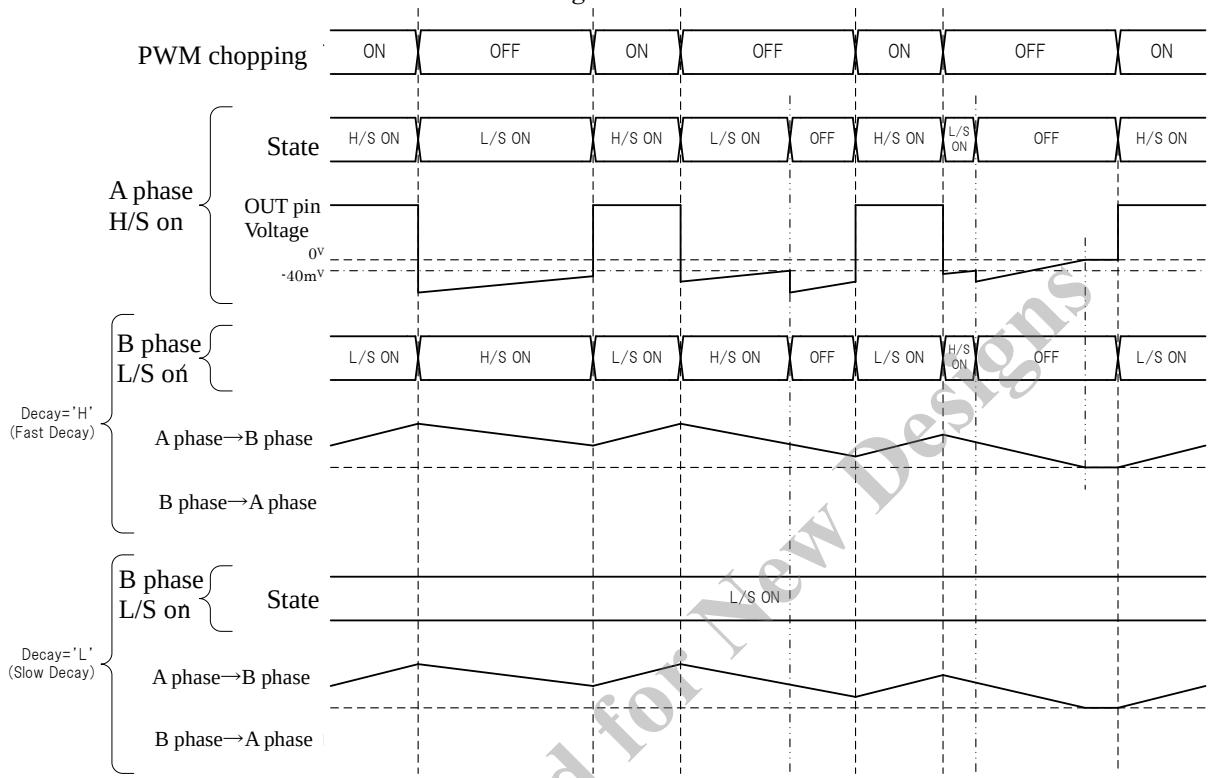
・ This diagram only shows the relation between PWM pin and output. However, the forced off time in "10.6 external PWM control" make the outputs be OFF.

・ Please tie to "L" when not using this function.

PWM and Synchronous rectification (Decay pin and SRMD pin)

SRMD='L' (passive mode)

Timing chart

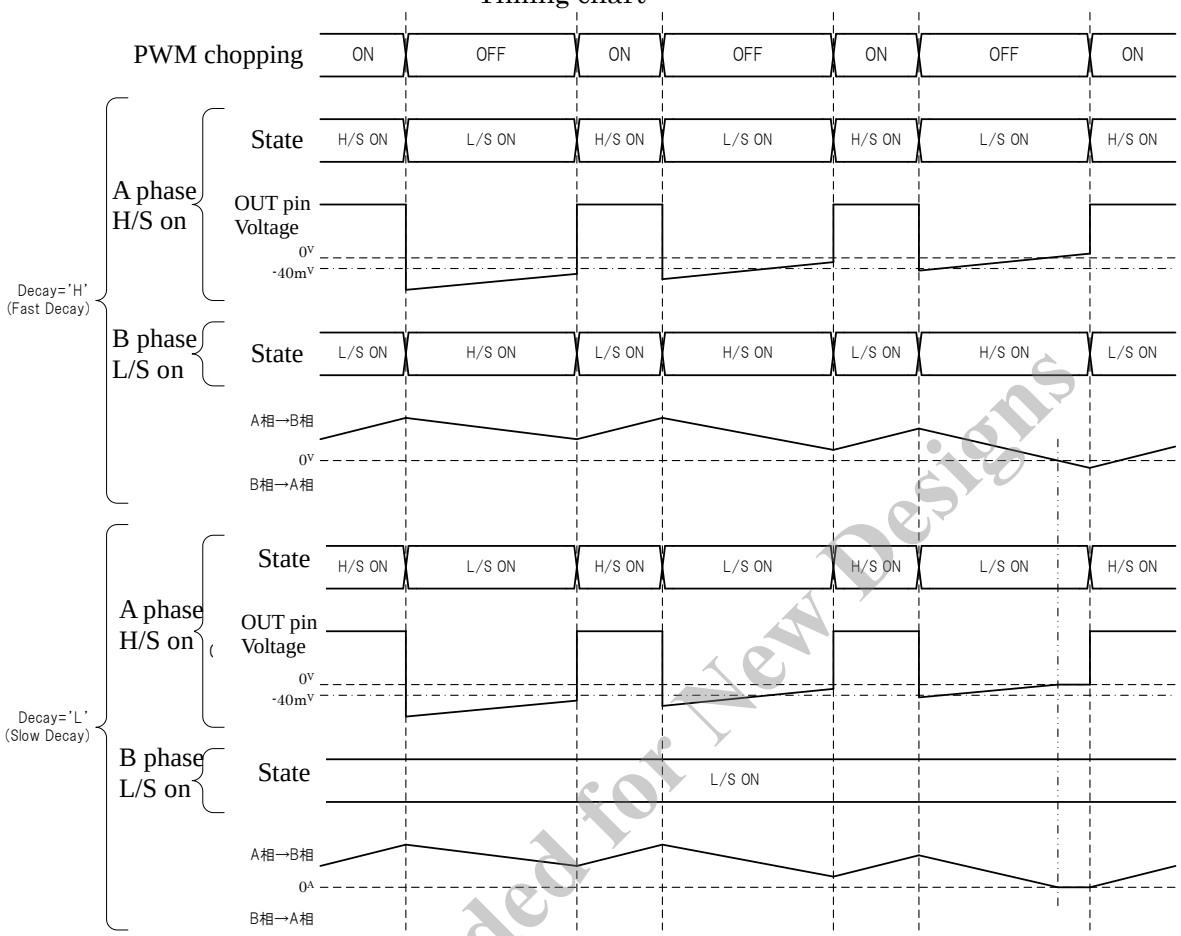


(※The value is typical in the timing chart)

・ The device stop the synchronous rectification in PWM off time if the voltage on OUT pin, where low side is ON, is over -40mV (typ, room temp).

SRMD='H'(Active mode)

Timing chart



(※The value is typical in the timing chart)

・ Synchronous rectification is active in PWM OFF (current recirculation) without monitor on OUT pin.

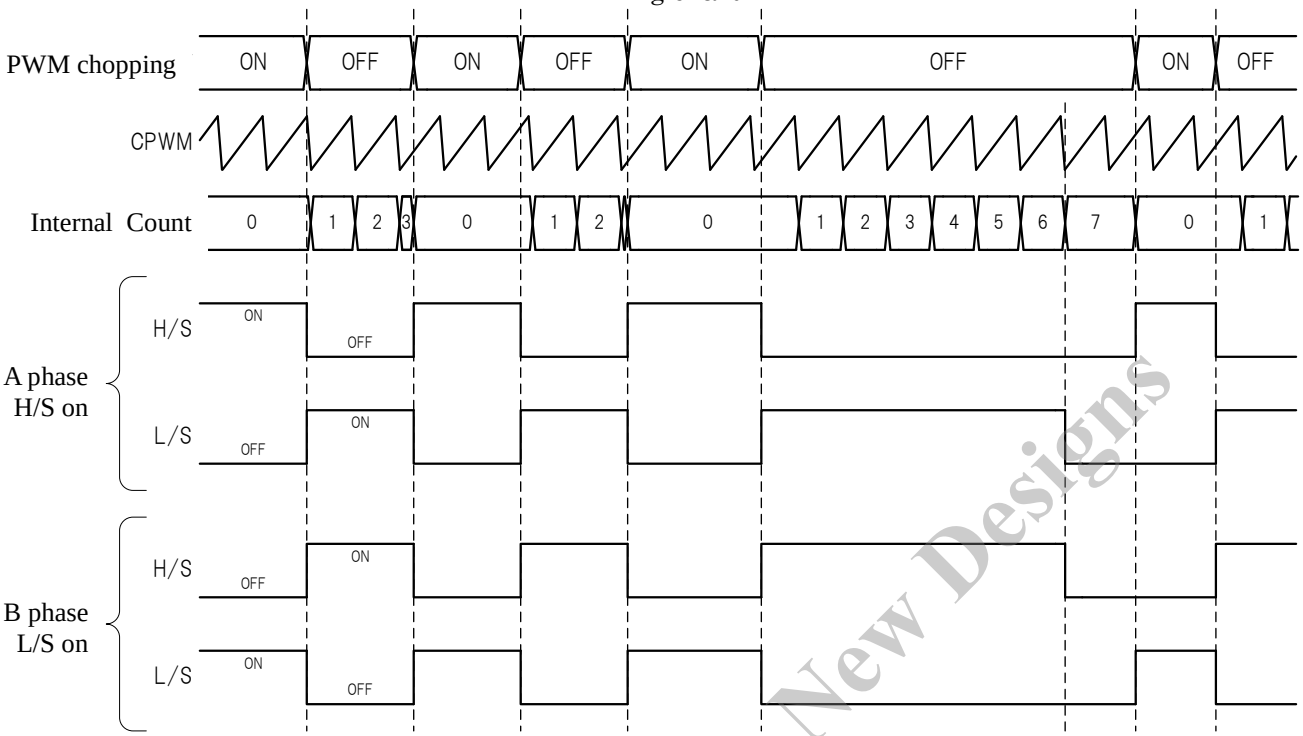
・ In this mode, since the excitation mode is not changed even if current recirculation is finished, the condition of the device is below.

- Slow Decay: Same as short brake
- Fast Decay: Reverse current starts to flow.

・ In the application where not using internal PWM with fast decay, the device gets OCP protection with long term of synchronous rectification due to the reverse current get large.

Disable function for synchronous rectification (Fast decay only)

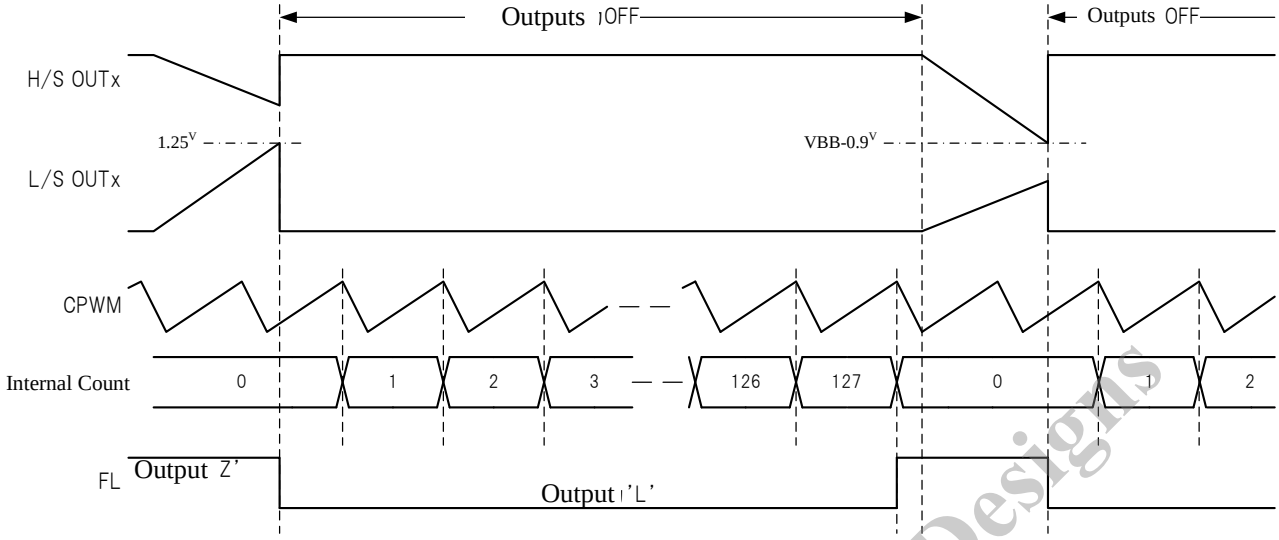
Timing chart



- The device stops synchronous rectification when PWM OFF keeps for 7 cycles of CPWM.
- Synchronous rectification is not activated when in brake mode.

Over current protection

Timing chart

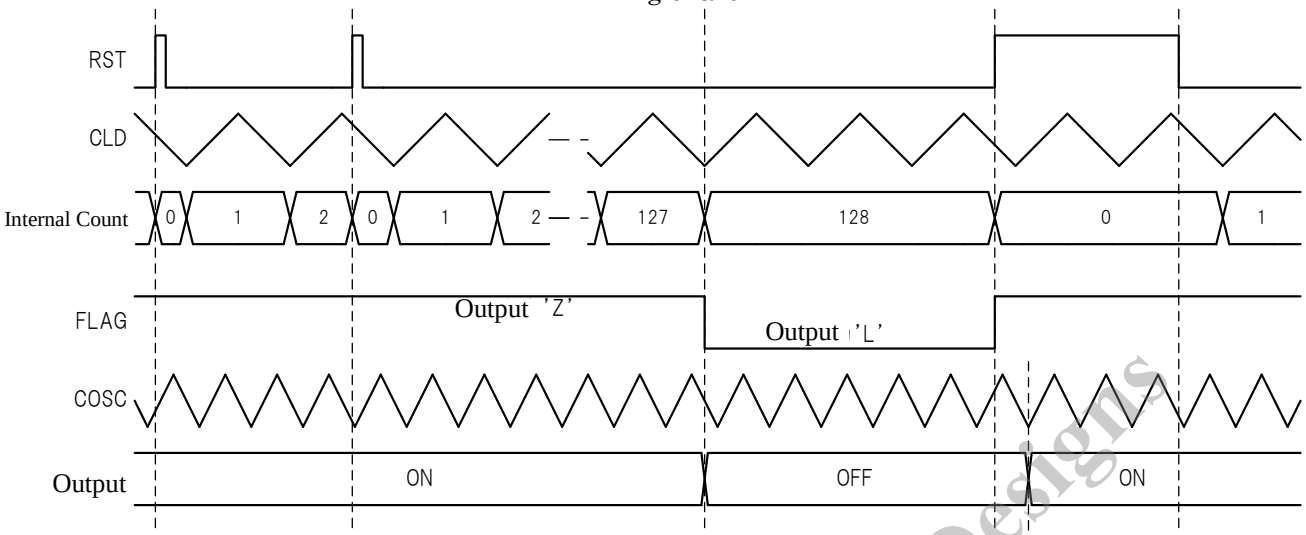


(※The value is typical in the timing chart)

- After OCP function is detected, outputs are disabled for 128 cycles of CPWM. After the disable time (128cycles of CPWM) is finished, the device automatically operates again
- The trigger for off timer count and release of FL output is at the top of CPWM oscillation waveform.
- The trigger for release of off timer count is at the bottom of CPWM oscillation.
- There is time difference between release for FL and actual output on.

Motor lock

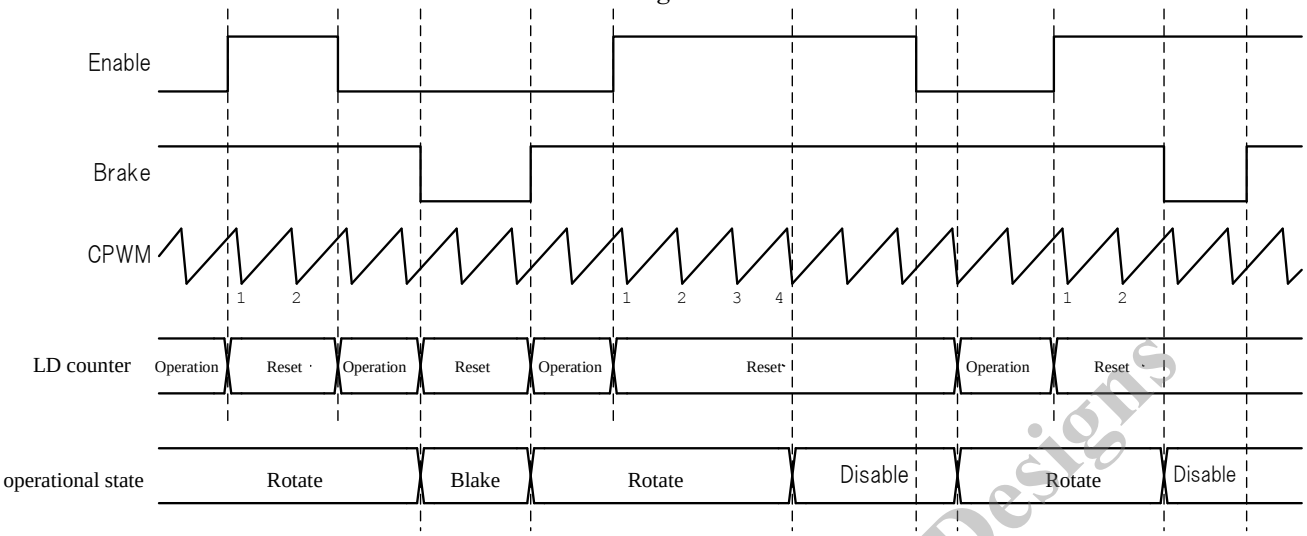
Timing chart



- Lock detection is active in operation only (Enable=L and Brake=H)
- The device recognizes lock condition if RST signal (H) is not for about 128 cycles of CLD.
- RST means internal signal showing release lock condition as in hall input changing. Please refer to timing chart in 10.12 Enable and Brake, or refer to 11.9 Lock detect.

Enable and Brake

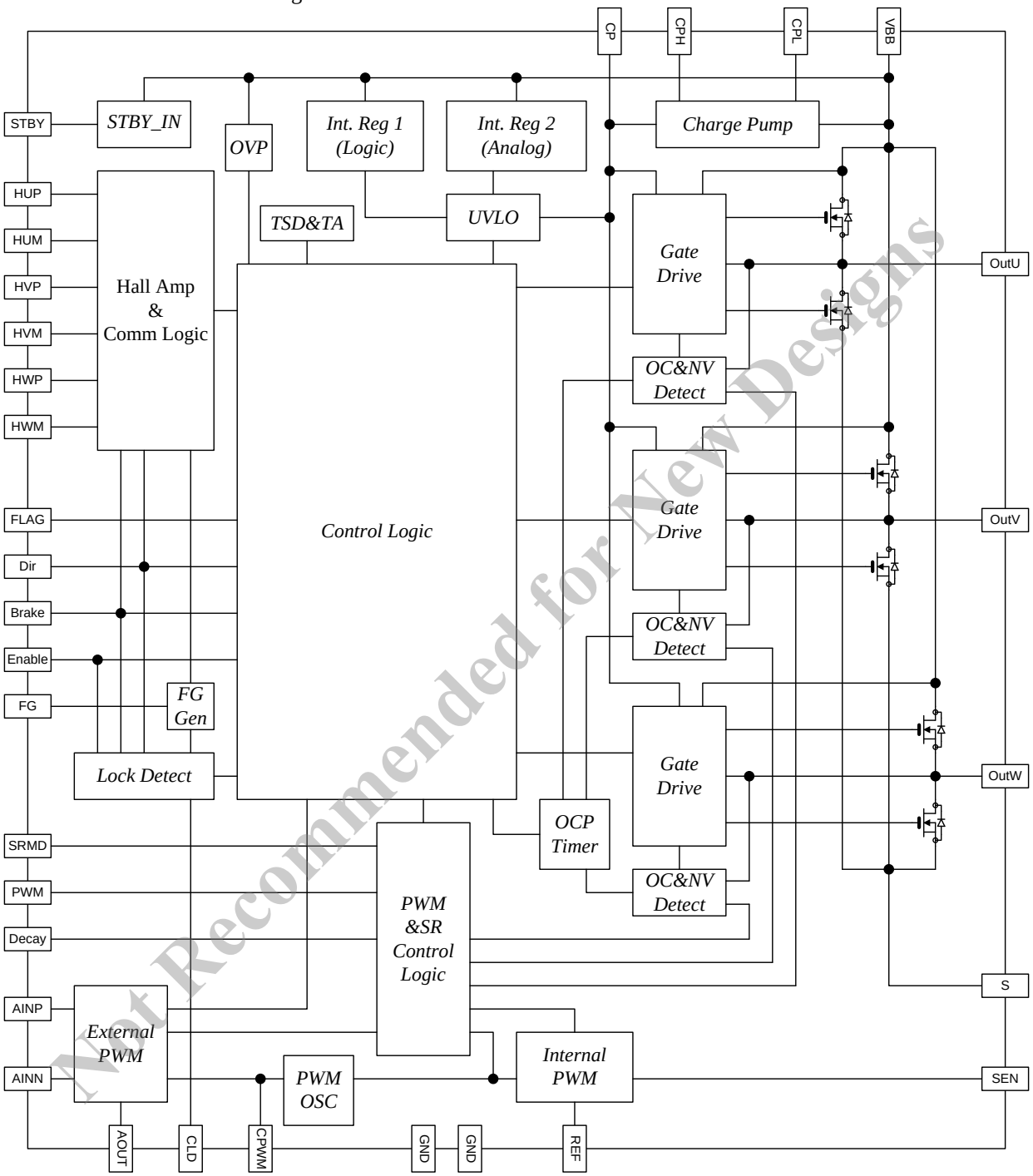
Timing chart



- Enable pin has two functions with priority below.
  - ① Reset for lock counter
    - ➢ Lock counter is reset for Enable being high.
  - ② Enable/Disable operation for output
    - ➢ The device makes output disable at 4th bottom on CPWM oscillation waveform after down-edge of Enable signal.
    - ➢ The device makes output enable at the first on trigger (the bottom of CPWM wave from) after Enable pin changing from "H" to "L".
- Brake signal is neglected for Enable being high.

5 Block diagram (Connection diagram)

Internal functional block diagram

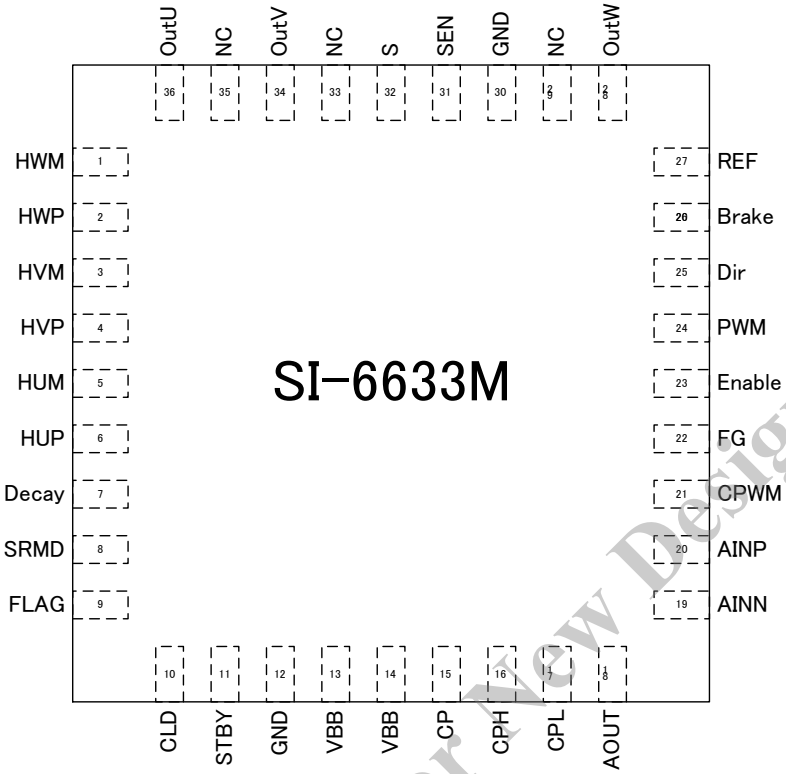


Pin Assignment (Terminal Functions)

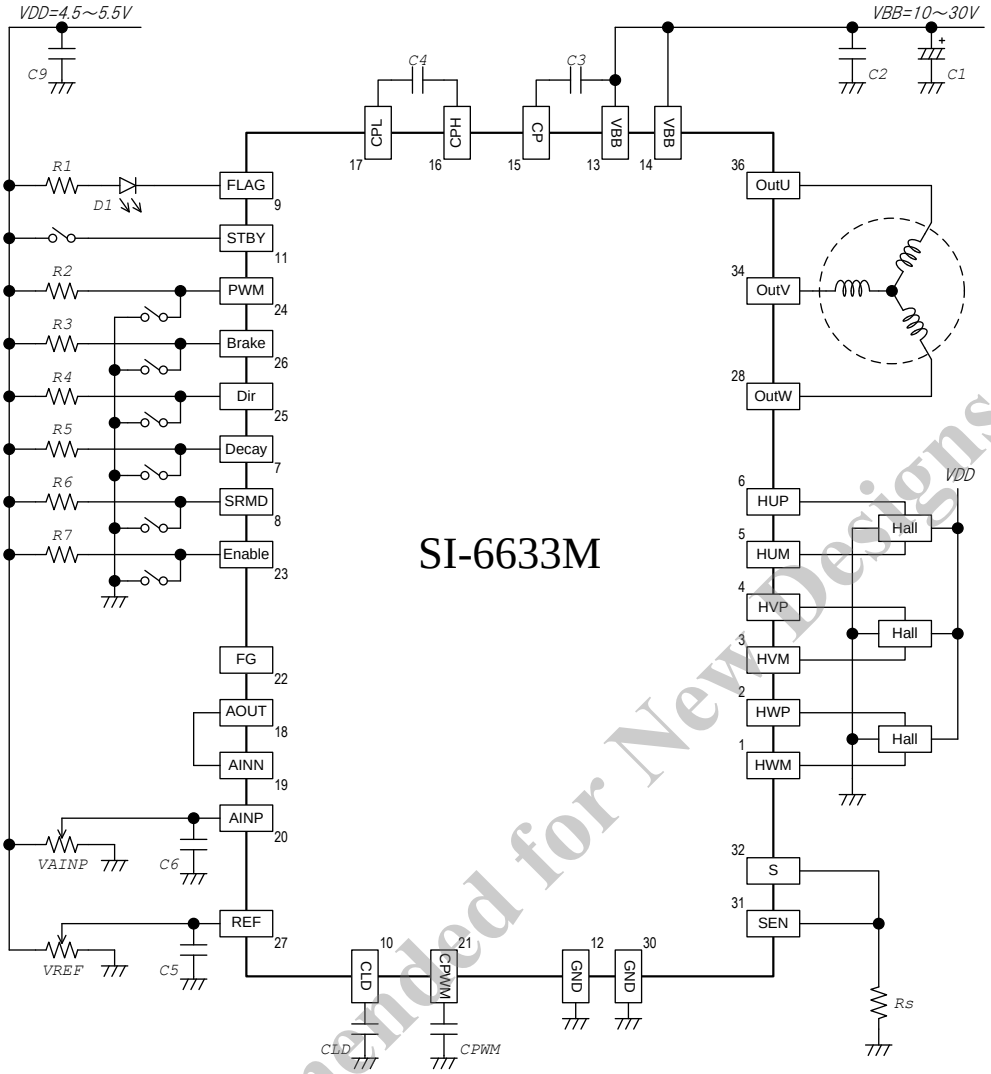
№	Pin name	Function
1	HWM	Hall input W-
2	HWP	Hall input W+
3	HVM	Hall input V-
4	HVP	Hall input V+
5	HUM	Hall input U-
6	HUP	Hall input U+
7	Decay	Select for decay mode
8	SRMD	Select for synchronous rectification
9	FLAG	Output for protection detected
10	CLD	Setting for lock detection timer
11	STBY	Stand-by input
12	GND	Ground
13	VBB	Motor power supply
14	VBB	Motor power supply
15	CP	Reservoir pin for charge pump
16	CPH	Pumping for charge pump - High
17	CPL	Pumping for charge pump - Low
18	AOUT	Amplifier output and 100% ON input
19	AINN	Minus pin for amplifier input
20	AINP	Plus pin for amplifier input
21	CPWM	Setting pin for PWM frequency
22	FG	Output for FG signal
23	Enable	Reset for lock counter and Enable input
24	PWM	External PWM control input
25	Dir	Direction input
26	Brake	Brake input
27	REF	Analog input for internal PWM current control
28	OutW	Output for W phase
29	N.C.	No Connection
30	GND	Ground
31	SEN	Current sensing input
32	S	Source pin
33	N.C.	No Connection
34	OutV	Output for V phase
35	N.C.	No Connection
36	OutU	Output for U phase

※Two GND pins should be connected together to ground line on PCB, two VBB pins should be connected together to VBB line.

Pin Assignment Diagram



6 Example application circuit(Evaluation Board Circuit)



Component value for reference

C1	: 100μF/50V	R1	: 1kΩ	CLD※1	: 0.1μF
C2※1	: 0.1μF/50V	R2	: 10kΩ	CPWM※1	: 1000pF
C3	: 0.1μF/16V	R3	: 10kΩ	Rs※1※2	: 0.1Ω
C4	: 0.1μF/50V	R4	: 10kΩ		
C5	: (option)	R5	: 10kΩ		
C6	: (option)	R6	: 10kΩ		
		R7	: 10kΩ		

※1:These components should be mounted as close to the device as possible.

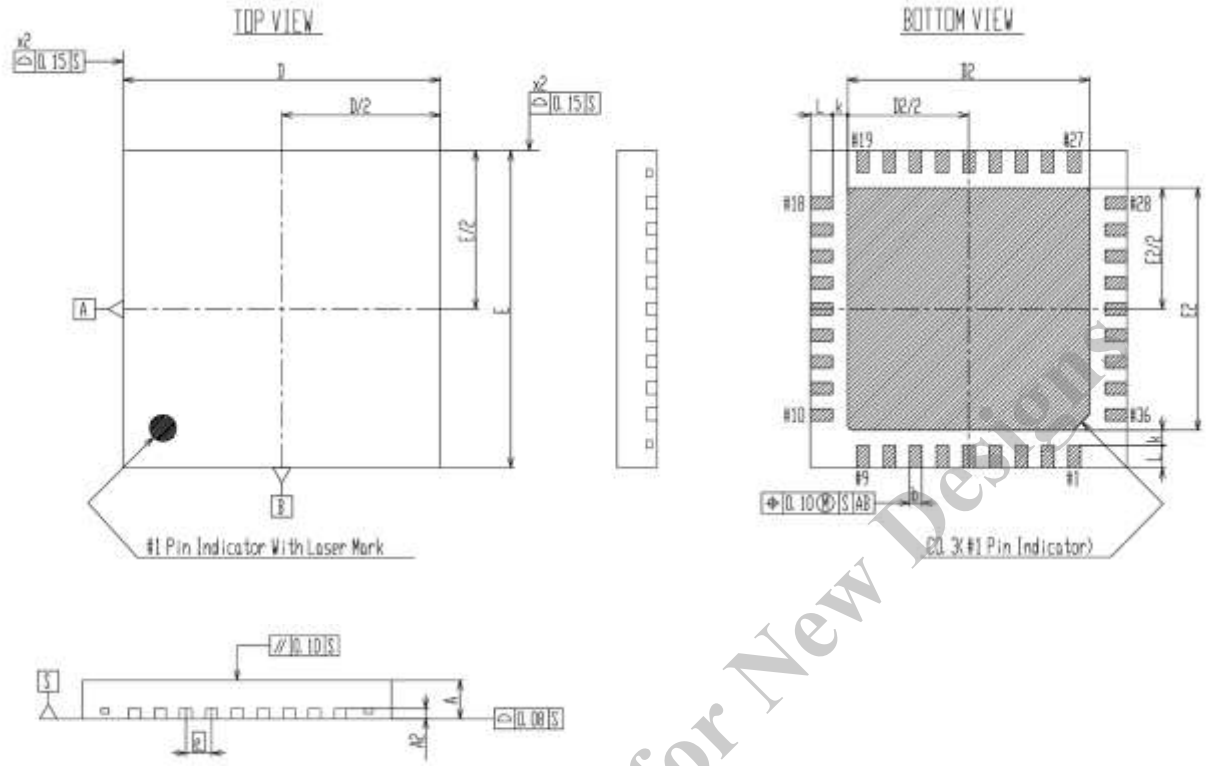
※2:Care should be taken with power dissipation.

☆Precaution to avoid the noise on V_{DD} line.

Switching noise from PCB traces, where high current flows, to the V_{DD} line should be minimized because the noise level more than 0.5V on the V_{DD} line may cause malfunctioning operation.
The tip for avoiding such problem is to separate the logic GND (S-GND) and the power GND (P-GND) on a PCB, and then connect them together at IC GND pin.

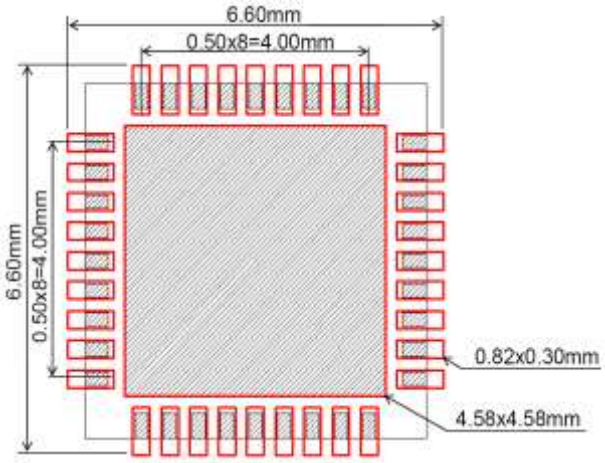
7 Package information

- 7-1 Package type, physical dimensions and recommendation foot print



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.18	0.23	0.28
D	5.90	6.00	6.10
D2	4.43	4.58	4.73
E	5.90	6.00	6.10
E2	4.43	4.58	4.73
e		0.50 BSC.	
k	0.25	—	—
L	0.32	0.42	0.52

Recommended foot print (red line)



Dimensions in millimeters
Material of terminal: Cu
Treatment of terminal : Ni + Pd +Au (Pb Free)

- 7-2 Appearance

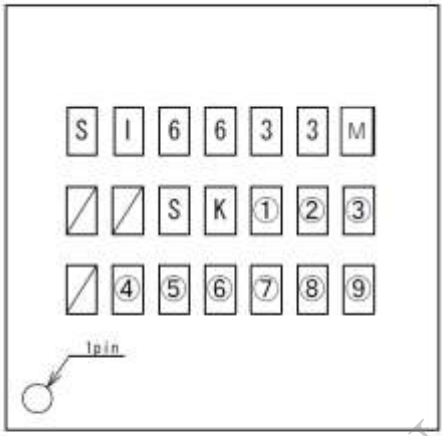
  The body shall be clean and shall not bear any stain, rust or flaw.

- 7-3 Marking

  The type number and lot number shall be clearly marked by laser so that cannot be erased easily.

- 7-4 Blanding

SI-6633M Marking Specification



Division	Mark No.	Contents
Year	①	The last digit of year
Month	②	Month by number or alphabet when assembly is started
		[1-9] in case from January to September
		[10] in case October
		[11] in case November
		[12] in case December
Week	③	[1] in case from first to tenth
		[2] in case from eleventh to twentieth
		[3] in case from twenty to thirty first
Control code	④～⑨	

8 Packing specifications

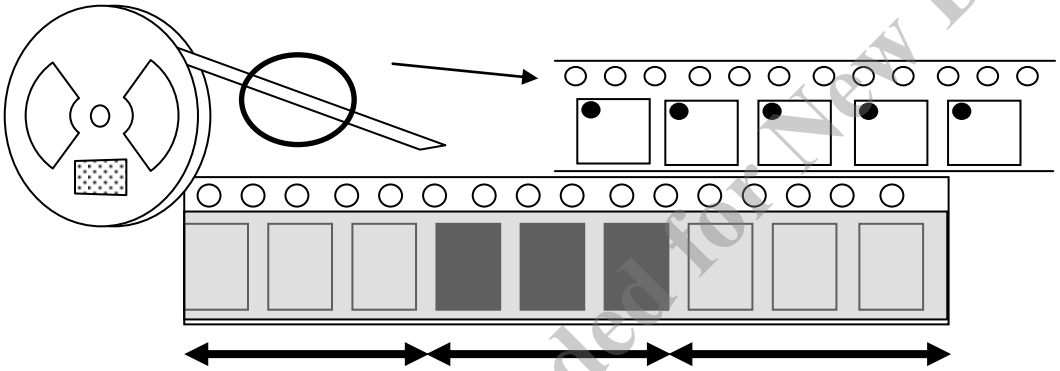
8－1. Container/Material/The number of parts per reel

Container is taping. the number of parts is 2500pcs per reel.
Remainder is packed with combination with next lot.

8－2. The material of taping

Material	
Emboss tape	The width of tape : 16mm
Reel	φ330 [mm]
laminate bag	Size : 0.075×380× 450 [mm]
Inner packing figure	Size : 340×360× 55 [mm]
Outer packing figure	Size : 350×370×230 [mm] 4 reels(max) per 1 outer box

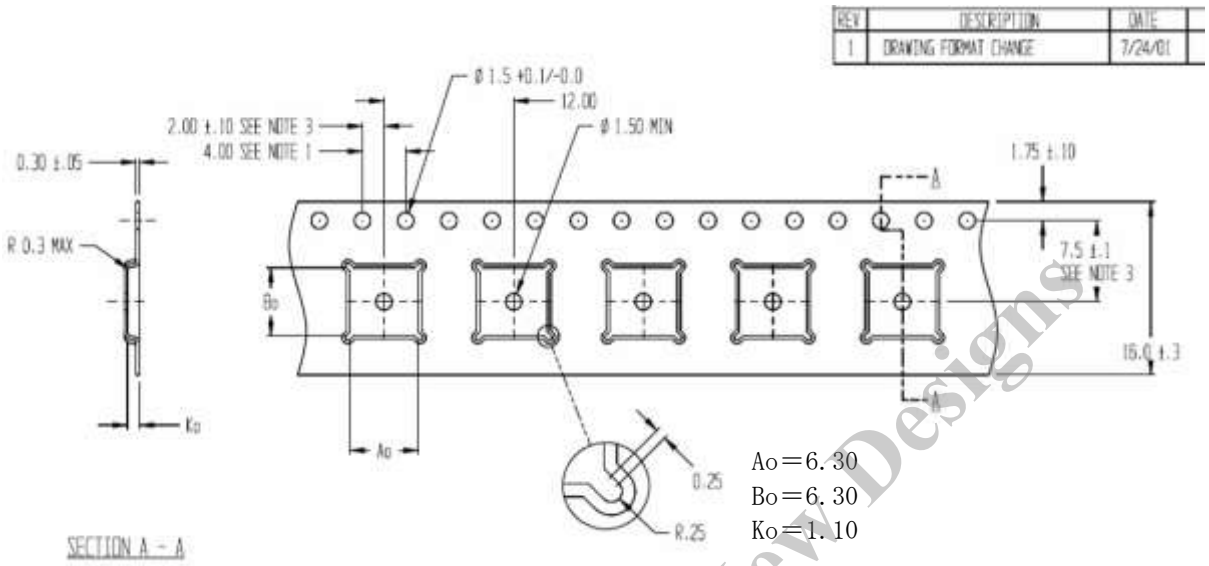
8－3. Emboss tape diagram



※It is heat-sealed with cover tape in reader and trailer.

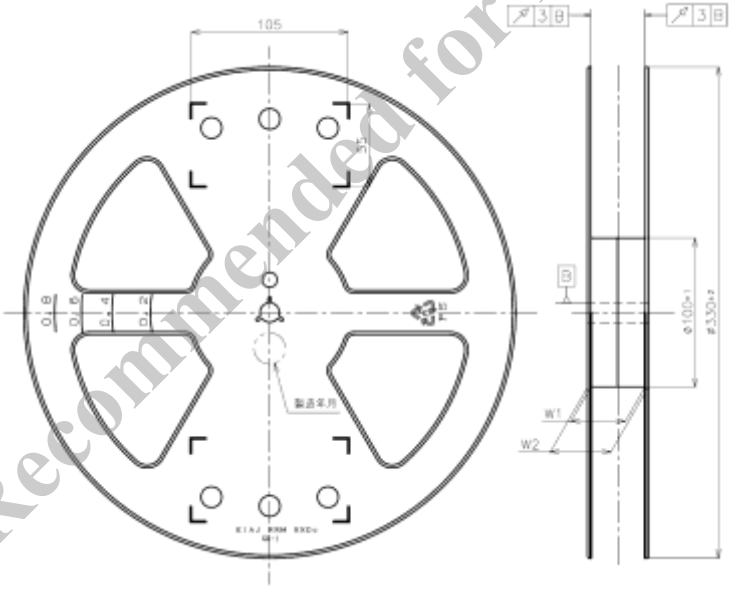
8－4．Dimension, material and diagram

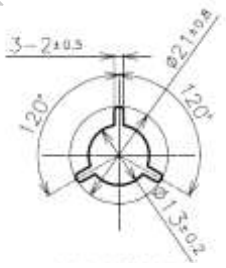
8－4－1．Emboss tape



Ao＝6.30
Bo＝6.30
Ko＝1.10

8－4－2．Reel





Detail of shaft hole

Tape width：16.0mmm
W1 ：17.5±1.0 mm
W2 ：21.5±1.0mm

Dimension in millimeter

・8－5 Storage condition

1． Storage environment is below.
Temperature: 5 degrees-30 degrees
Humidity: 90% or below
Storage limitation is within 12month from packing date

2． If the above storage condition (8-5.1) is expired, the device is needed to have baking with 125 dgerees for 20 hours. Also, Tape and reel are not guaranteed with the temperature and time condition.
If the device should be baked, it is needed to use container with “heatproof” or temperture to cover baking condition. And the container is needed to have static electricity control.

9 Cautions and warnings

Logic inputs/output (PWM, Dir, Decay, SRMD, FG, FL, Break, Enable, STBY)

・Be sure to prevent the logic inputs(PWM, Dir, Decay, SRMD, Break, Enable, STBY) from being "OPEN". If some of the logic inputs are not used, be sure to connect them to VDD or GND.
※In case some of the logic inputs stay "OPEN", a malfunction may occur due to external noises.

・When the logic output(FG, FL) is not used, be sure to keep it "OPEN" or Gnd.
※In case it is connected to VDD, it may cause the device's deterioration or/and breakdown.

About the protection circuit operation

This product has Two protection circuits (motor coil short-circuit and overheating).
These protection circuits work with detecting the thing that excessive energy joins the driver.
Therefore, it is not possible to protect it when the energy caused by the motor coil short-circuit is outside the tolerance of the driver.

Notice

This driver has MOS inputs. Please notice as following contents.

・When static electricity is a problem, care should be taken to properly control the room humidity. This is particularly true in the winter when static electricity is most troublesome.

・Care should be taken with device leads and with assembly sequencing to avoid applying static charges to IC leads. PC board pins should be shorted together to keep them at the same potential to avoid this kind of trouble.

10. other

- Application and operation examples described in this document are quoted for the sole purpose of reference for the use of the products herein and Sanken can assume no responsibility for any infringement of industrial property rights, intellectual property rights or any other rights of Sanken or any third party which may result from its use.

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  In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature (Tj) affects the reliability significantly.

- When using the products specified herein by either (i) combining other products or materials therewith or (ii) physically, chemically or otherwise processing or treating the products, please duly consider all possible risks that may result from all such uses in advance and proceed therewith at your own responsibility.

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