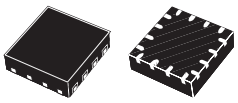
STMEC001

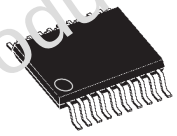
Power interface switch for ExpressCard™

Features

- Compliant with PC Card™ standard for ExpressCard
- 3-channel power interface switch
- Built-in under-voltage lockout (UVLO) circuit
- Ultra-low standby-mode current
- Additional 5 V or 12 V power supply not required
- High reliability ensured with integrated over-current, thermal and undervoltage protection circuitries applied to each voltage rail
- Soft start function for non-rush current
- Ultra-low standby-mode current for power saving
- Ultra-low ON resistance for fast switching



QFN16



TSSOP20

Description

The STMEC001 is an ExpressCard power interface switch which provides the complete power management solution required by the ExpressCard specification.

The STMEC001 consists of 3 internal switches distributing 3.3 V, 3.3 V_{AUX}, and 1.5 V to the ExpressCard socket without the need of additional charge pump or external switches.

The STMEC001 ExpressCard power switch is ideal for notebook computers, desktop computers, personal digital assistants (PDA), or other handheld devices implementing the ExpressCard schematic.

Table 1. Device summary

Order code	Package	Packing
STMEC001QTR	QFN16	Tape and reel
STMEC001ATTR	TSSOP20	Tape and reel

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1 Pin description

Figure 1. STMEC001 pin configuration (top view)

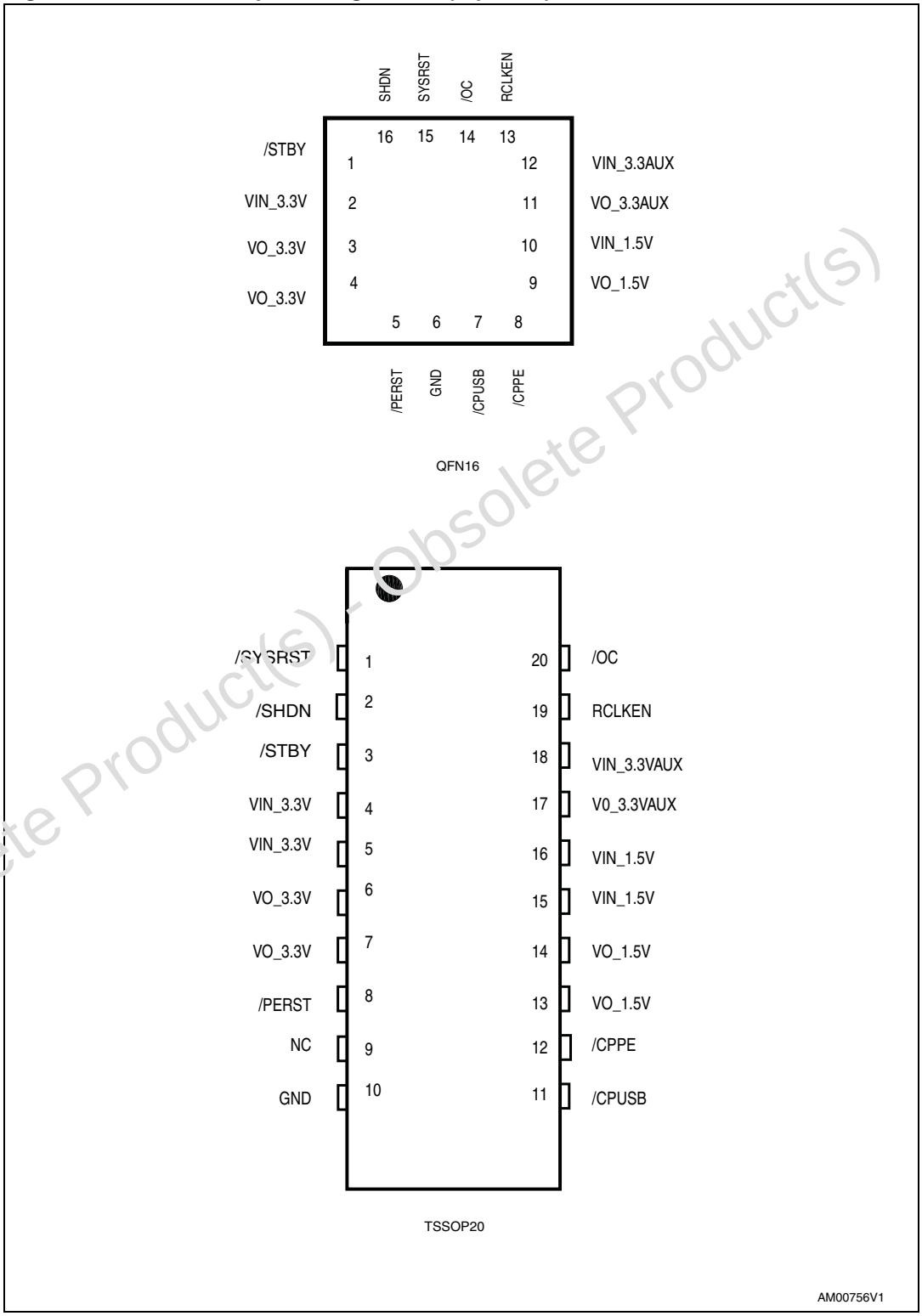


Table 2. Pin assignments

Pin		Name	Type	Description
QFN16	TSSOP20			
15	1	/SYSRST	I	System Reset input - active low, logic level signal, internal 150 KΩ pull-up
16	2	/SHDN	I	Shutdown input - active low, logic level signal, internal 150 KΩ pull-down
1	3	/STBY	I	Standby input - active low, logic level signal, internal 150 KΩ pull-down
2	4	VIN_3.3V	I	3.3 V input for VO_3.3V
-	5	VIN_3.3V	I	3.3 V input for VO_3.3V
3	6	VO_3.3V	O	Switched output that delivers 0 V, 3.3 V or high impedance to card
4	7	VO_3.3V	O	Switched output that delivers 0 V, 3.3 V or high impedance to card
5	8	/PERST	O	A logic level power good to slot (delayed)
-	9	NC	-	No connection
6	10	GND	-	Ground
7	11	/CPUSB	I	Card present input for USB cards, internal 150 KΩ pull-up
8	12	/CPPE	I	Card present input for PCI ExpressCard, internal 150 KΩ pull-up
9	13	VO_1.5V	O	Switched output that delivers 0 V, 1.5 V or high impedance to card
-	14	VO_1.5V	O	Switched output that delivers 0 V, 1.5 V or high impedance to card
10	15	VIN_1.5V	I	1.5 V input for 1.5Vout
-	16	VIN_1.5V	I	1.5 V input for $1.5V_{OUT}$
11	17	$VO\_3.3V_{AUX}$	O	Switched output that delivers 0 V, 3.3 V or high impedance to card
12	18	$VIN\_3.3V_{AUX}$	I	3.3 V input for $VO\_3.3V_{AUX}$ and chip power
13	19	RCLKEN	I/O	Reference clock enable signal. As an output, a logic level power good to host for slot (open drain). As an input, if kept inactive by the host, prevents /PERST from being de-asserted, internal 150 KΩ pull-up
14	20	/OC	O	Over-current status output for slot (open drain)

1.1 Pin functional description

Table 3. Pin detailed descriptions

Symbol	Description
CPPE	A logic low level on this input indicates that the card present supports PCI Express functions. This input pin connects to the 3.3 V_{AUX} input through a 150 kΩ internal pull up. When inserted, the card physically connects this input to ground if the card supports PCI Express functions.
CPUSB	A logic low level on this input indicates that the card present supports USB functions. The input pin CPUSB connects to the 3.3 V_{AUX} input through a 150 kΩ internal pull up. When inserted, the card physically connects CPUSB to ground if the card supports USB functions.
SHDN	When asserted (logic low), this input instructs the STMEC001 to turn off all voltage outputs and the discharge FETs at the 3 outputs are activated.
STBY	When asserted (logic low), this input places the power switch in Standby Mode by turning off the 3.3 V and 1.5 V power switches and keeping the 3.3 V_{AUX} switch on.
RCLKEN	This pin serves as both an input and an output. On power up, the power switch keeps this signal at a low state as long as any of the output power rails are out of their tolerance range. Once all output power rails are within tolerance, the power switch releases RCLKEN allowing it to transition to a high state (internally pulled up to 3.3 V_{AUX}). The transition of RCLKEN from a low to a high state starts an internal timer for the purpose of de-asserting /PERST. As an input, RCLKEN can be kept low to delay the start of the /PERST internal timer. RCLKEN can be used by the host system to enable a clock driver.
PERST	On power up, this output remains asserted. Once all power rails are within tolerance, RCLKEN is asserted and /PERST is de-asserted after a time delay. On power down, this output is asserted whenever any of the power rails drop below their voltage tolerance.
SYSRST	This input is driven by the host system and directly affects /PERST. Asserting /SYSRST (logic level low) forces /PERST to assert.
OC	The OC pin is an open drain output for over-current indication. Output does not turn off during over-current condition. The output voltage decreases as the output current exceeds over-current limit. Only if the temperature increases above the limit the output is turned off completely. Over-current in one output does not affect the other outputs.

2 Logic diagram

Figure 2. STMEC001 block diagram

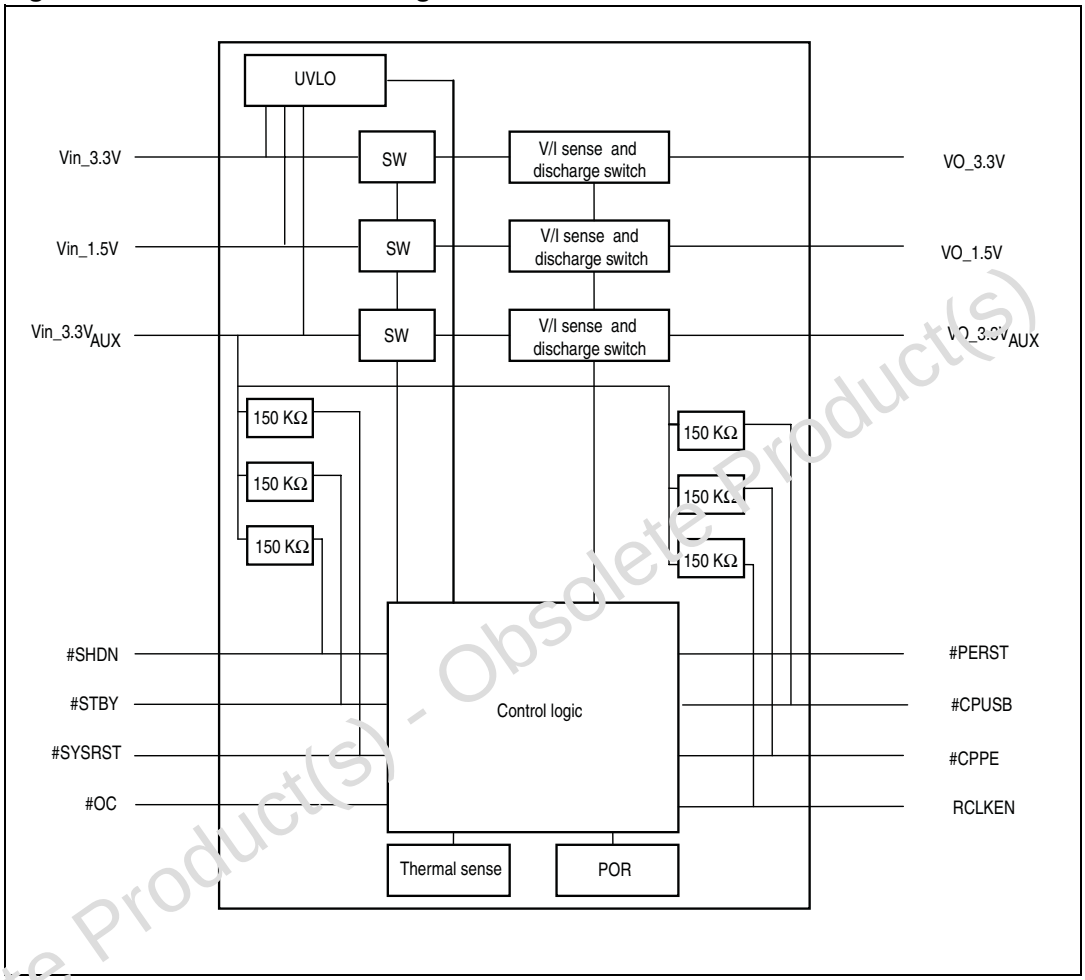
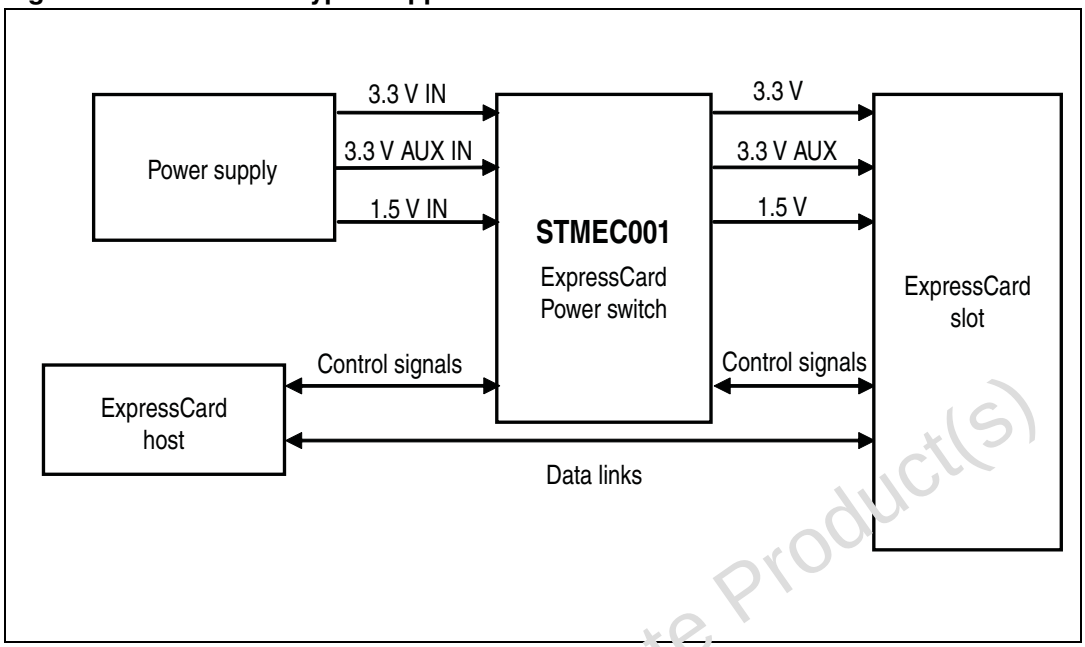


Figure 3. STMEC001 typical application



3 Maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings(1)

Symbol	Parameter	Value	Unit
V_I	Input voltage	$V_I(3.3V_{IN})$ – 0.3 to 4.6	V
		$V_I(1.5V_{IN})$ – 0.3 to 4.6	V
		$V_I(3.3V_{AUX})$ – 0.3 to 4.6	V
I_O	Output current	$V_I(3.3V_{IN})$ internally limited	
		$V_I(1.5V_{IN})$ internally limited	
		$V_I(3.3V_{AUX})$ internally limited	
T_{OP}	Operating junction temperature, T_J (max to be calc. at worst case PD at 85° C ambient)	–40 to 120	°C
T_{STG}	Storage temperature range	–55 to 150	°C

1. Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

4 Power states

The STMEC001 operates in a number of states, as described in the following table:

Table 5. Power states

Voltage inputs			Logic states				Outputs			Mode
$3.3V_{AUX}$	3.3 V	1.5 V	/SHDN	/CPUSB	/CPPE	/STBY	$3.3V_{AUX}$	3.3 V	1.5 V	
ON	X	X	1	1	1	X	GND	GND	GND	No card
ON	X	X	0	X	X	X	GND	GND	GND	Shutdown
ON	ON	ON	1	0	X	1	ON	ON	ON	USB enable
ON	ON	ON	1	X	0	1	ON	ON	ON	PE enable
ON	ON	ON	1	X	X	0	ON	OFF	OFF	Standby
OFF	X	X	X	X	X	X	OFF	OFF	OFF	OFF

4.1 Power states description

- **No card mode**: when no card is inserted, and at least 3.3 V_{AUX} is available, all outputs are grounded
- **Shutdown mode**: when /SHDN is asserted, and at least 3.3 V_{AUX} is available all outputs are grounded
- **USB/PW enable mode**: when all 3 inputs are available, detection of cartd insertion turns on all 3 outputs
  - VIN_3.3 V, VIN_3.3V_{AUX} and VIN_1.5 V are present at the USB/PW enable input of the power switch prior to a card being inserted. Power to the card is based on the state of /CPUSB and /CPPE (see table).
  - The card is present and VIN_1.5 V or/and VIN_3.3 V is removed from the input of the power switch; VIN_3.3V_{AUX} will still be provided to the card, VIN_1.5 and VIN_3.3 V will be disabled (see table). If power to VIN_1.5 V and VIN_3.3 V is restored, output to the card will be restored.
  - Prior to the insertion of a card, VIN_3.3 V_{AUX} is available, VIN_3.3 V and VIN_1.5 V are not available; no power is made available to the card. If VIN_1.5 V and VIN_3.3 V are made available at the input of the power switch after the card is inserted, both VO_3.3 V and VO_1.5 V are made available to the card.
  - **Standby mode**: when all 3 supplies are available and /STBY is asserted. Only 3.3 V_{AUX} output is on.
  - **OFF mode**: if V_{AUX} is off, all outputs are off. When VIN_3.3V_{AUX} is not present, VIN_1.5 V or/and VIN_3.3 V must not be present.

5 Electrical characteristics

Table 6. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_I	Input voltage: $V_I(3.3V_{IN})$ is required for its respective functions	3.0 to 3.6	V
	Input voltage: $V_I(1.5V_{IN})$ is required for its respective functions	1.35 to 1.65	V
	Input voltage: $V_I(3.3V_{AUX})$ is required for all circuit operations	3.0 to 3.6	V
I_O	Output current: $I_O(3.3V)$ at T_J = 100 °C	1.3 (max.)	A
	Output current: $I_O(1.5V)$ at T_J = 100 °C	650 (max.)	mA
	Output current: I_O(AuxV) at T_J = 100 °C	275 (max.)	mA
T_{OP}	Operating junction temperature, T_J (max to be calc. at worst case PD at 85° C ambient)	100	°C

Table 7. Electrical characteristics
T_J = 25° C, $V_I(V_{IN}$ 3.3 V) = $V_I(V_{IN}$ 3.3V_{AUX})= 3.3 V, $V_I(V_{IN}$ 1.5 V) = 1.5 V

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_{SW}(1) TSSOP20	VIN_3.3 V to VO_3.3 V	I = 1300 mA, T_J = 25 °C		53	64	mΩ
		I = 1300 mA, T_J = 100 °C			80	
	VIN_1.5 V to VO_1.5 V	I = 650 mA, T_J = 25 °C		70	88	
		I = 650 mA, T_J = 100 °C			105	
	VIN_3.3V_{AUX} to VO_V_{AUX}	I = 275 mA, T_J = 25 °C		140	170	
		I = 275 mA, T_J = 100 °C			210	
R_{SW}(1) QFN16	VIN_3.3 V to VO_3.3 V	I = 1300 mA, T_J = 25 °C		53	64	mΩ
		I = 1300 mA, T_J = 100 °C			80	
	VIN_1.5 V to VO_1.5 V	I = 650 mA, T_J = 25 °C		80	92	
		I = 650 mA, T_J = 100 °C			115	
	VIN_3.3V_{AUX} to VO_V_{AUX}	I = 275 mA, T_J = 25 °C		170	192	
		I = 275 mA, T_J = 100 °C			230	
R_O	R_O(3.3 V) discharge resistance	I discharge = 1 mA	0.1		0.5	kΩ
	R_O(1.5 V) discharge resistance	I discharge = 1 mA	0.1		0.5	
	R_O(1.5 V) discharge resistance	I discharge = 1 mA	0.1		0.5	

Table 7. Electrical characteristics (continued)
T_J = 25° C, V_I(V_{IN} 3.3 V) = V_I(V_{IN} 3.3V_{AUX})= 3.3 V, V_I(V_{IN} 1.5 V) = 1.5 V

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{OS}	I_O(3.3 V) limit (limit is the steady state value)	T_J -40° C to100° C Output powered into a short	1.3		2.5	A
	I_O(1.5 V) limit	T_J -40° C to100° C Output powered into a short	650		1300	mA
	I_O(V_{AUX}) limit	T_J -40° C to 100° C Output powered into a short	275		660	

1. Switch resistance (in production - probe testing at 1.3 A. Final test at 1.0 A and apply guard band)

Table 8. Power switching

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
Tsh	Thermal shutdown, trip point, T_J.		Over-current condition	155		165	° C
	Hysteresis				10		° C
I_{OL}	Current limit response time. From short to first threshold within 1.1 times of the final current limit		V_O (3.3V_{OUT}) with100 mΩ short		5	20	µs
			V_O (1.5V_{OUT}) with100 mΩ short		5	20	
			V_O (V_{AUX}) with100 mΩ short		5	20	
I_Q	Input quiescent current: normal operation	$V_{IN\_3.3}V_{AUX}$	V_O(V_{AUX}) = V_I(3.3V_{AUX}) = V_I(3.3V_{IN}) V_O(1.5V) = VI(1.5VIN) T_J -40° C,100° C Outputs are ON and unloaded			120	µA
		$V_{IN\_3.3V}$				40	
		$V_{IN\_1.5V}$				10	
	Input quiescent current: normal operation with pull-up	$V_{IN\_3.3}V_{AUX}$	V_O(V_{AUX}) = V_I(3.3V_{AUX}) = V_I(3.3V_{IN}) V_O(1.5 V) = V_I(1.5V_{IN}) T_J -40° C,100° C] Outputs are ON and unloaded		150	180	
		$V_{IN\_3.3V}$			25	40	
		$V_{IN\_1.5V}$			10	25	
	Input quiescent current: /SHDN asserted with pull-up	$V_{IN\_3.3}V_{AUX}$	T_J -40° C,100° C discharge FETs are ON		150	270	
		$V_{IN\_3.3V}$			10	15	
		$V_{IN\_1.5V}$			10	15	
SHDN	Forward leakage current (current measured at input pins/no card present) /SHDN inactive		$V_{IN\_3.3}V_{AUX}$		50	100	µA
			$V_{IN_}$3.3V		15	20	
			$V_{IN_}$1.5V		5	10	
I_{LEAK}(1)	Reverse leakage current (current measured from output pins / input grounded)	$V_{IN\_3.3}V_{AUX}$	T_J = 25 ° C		5	10	µA
			T_J = 100 ° C		20	50	
		$V_{IN\_1.5V}$	T_J = 25 ° C		10	15	
			T_J = 100 ° C		30	50	
		$V_{IN\_3.3V}$	T_J = 25 ° C		10	15	
			T_J = 100 ° C		30	50	

1. All high side switches are in Hi-Z state, V_O (AUX) = V_O (3.3 V) = 3.3 V, Vo (1.5 V) = 1.5 V, T_J -40 ° C,100 ° C

Table 9. Undervoltage lockout (UVLO)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
UVLO	VIN_3.3 UVLO	VIN_3.3 level, below which VIN_3.3 and VIN_1.5 switches are off	2.6		2.9	V
	VIN_1.5 UVLO	VIN_1.5 level, below which VIN_3.3 and VIN_1.5 switches are off	1		1.25	V
	VIN_3.3 VAUX UVLO	VIN_3.3VAUX level, below which sets the device into OFF state	2.6		2.9	V
	UVLO hysteresis			100		mV

6 Logic characteristics

Table 10. Logic states

Logic transition	Condition	Min	Typ	Max	Unit
Logic input voltage	High level	2.0			V
	Low level			0.8	
PERST# assertion threshold of output voltage	3.3 V output falling	2.7		3.0	V
	AUX output falling	2.7		3.0	
	1.5 V output falling	1.2		1.35	
PERST# assertion delay from output voltage invalid	Output falling below threshold			500	ns
PERST# de-assertion from output voltage valid	Output rising above threshold	4	10	20	ms
PERST# assertion delay from SYSRST#	STSRST asserted or de-asserted			500	ns
RCLKEN assertion delay from output voltage valid	Output rising above threshold			100	µs
OC# output low voltage	I_{OC} = 2 mA			0.4	V
OC# leakage current	V_{OC} = 3.6 V			1	µA
OC# deglitch	Falling into or out of an over-current condition	6		20	µs

Table 11. ESD protections

Pin	Condition	ESD tolerance	Unit
V_{OUT} (3.3 V, 1.5 V, AUX)	Versus GND & supply	6	kV
All other pins (except RCLKEN)	Versus GND & supply	2	
RCLKEN	Versus GND	2	
RCLKEN	Versus supply	1	

7 Switching times

Table 12. Switching characteristics

Symbol	Parameter		Condition	Min	Typ	Max	Unit
t_R	Output rise time	VIN_3.3V to VO_3.3V	$C_{L(3.3V)}$ = 0.1 µF $I_{o(3.3V)}$ = 0 A	0.1		3	ms
		VIN_3.3V$_{AUX}$ to VO_V$_{AUX}$	$C_{L(AUX)}$ = 0.1 µF $I_{o(AUX)}$ = 0A	0.1		3	
		VIN_1.5V to VO_1.5V	$C_{L(1.5V)}$ = 0.1 µF $I_{o(1.5V)}$ = 0 A	0.1		3	
		VIN_3.3V to VO_3.3V	$C_{L(3.3V)}$ = 100 µF R_L = VO_3.3V / 1.0 A	0.1		6	
		VIN_3.3V$_{AUX}$ to VO_V$_{AUX}$	$C_{L(3.3V)}$ = 100 µF R_L = VO_V$_{AUX}$/ 0.25 A	0.1		6	
		VIN_1.5V to VO_1.5V	$C_{L(3.3V)}$ = 100 µF R_L = VO_1.5 V / 0.5 A	0.1		6	
t_F	Output fall time (/CPUSB and /CPPE inactive)	VIN_3.3V to VO_3.3V	$C_{L(3.3V)}$ = 0.1 µF $I_{o(3.3V)}$ = 0 A	10		150	µs
		VIN_3.3V$_{AUX}$ to VO_V$_{AUX}$	$C_{L(AUX)}$ = 0.1 µF $I_{o(AUX)}$ = 0 A	10		150	
		VIN_1.5V to VO_1.5V	$C_{L(1.5V)}$ = 0.1 µF $I_{o(1.5V)}$ = 0 A	10		150	
		VIN_3.3V to VO_3.3V	$C_{L(3.3V)}$ = 20 µF, no load	2.0		30.0	ms
		VIN_3.3V$_{AUX}$ to VO_V$_{AUX}$	$C_{L(AUX)}$ = 20 µF, no load	2.0		30.0	
		VIN_1.5V to VO_1.5V	$C_{L(1.5V)}$ = 20 µF, no load	2.0		30.0	
t_{SHDN}	Output fall time (/SHDN active)	VIN_3.3V to VO_3.3V	$C_{L(3.3V)}$ = 0.1 µF $I_{o(3.3V)}$ = 0 A	10		80	µs
		VIN_3.3V$_{AUX}$ to VO_V$_{AUX}$	$C_{L(AUX)}$ = 0.1 µF $I_{o(AUX)}$ = 0 A	10		80	
		VIN_1.5V to VO_1.5V	$C_{L(1.5V)}$ = 0.1 µF $I_{o(1.5V)}$ = 0 A	10		80	
		VIN_3.3V to VO_3.3V	$C_{L(3.3V)}$ = 100 µF R_L = VO_3.3V/1.0 A	0.1		5.0	ms
		VIN_3.3V$_{AUX}$ to VO_V$_{AUX}$	$C_{L(3.3V)}$ = 100 µF R_L = VO_V$_{AUX}$/0.25 A	0.1		5.0	
		VIN_1.5V to VO_1.5V	$C_{L(3.3V)}$ = 100 µF R_L = VO_1.5V/0.5 A	0.1		5.0	

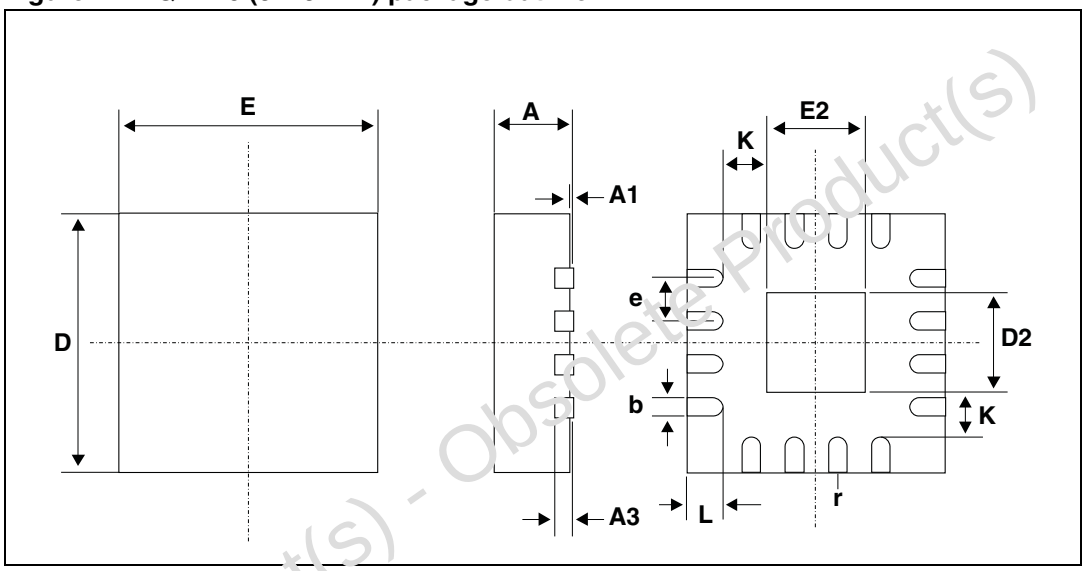
Table 12. Switching characteristics (continued)

Symbol	Parameter		Condition	Min	Typ	Max	Unit
t_{PD}	Propagation delay	VIN_3.3V to VO_3.3V	$C_{L(3.3V)}$ = 0.1 µF $I_{o(3.3V)}$ = 0 A	0.02		1.0	ms
		VIN_3.3V$_{AUX}$ to VO_V$_{AUX}$	$C_{L(AUX)}$ = 0.1 µF, $I_{o(AUX)}$ = 0 A	0.02		1.0	
		VIN_1.5V to VO_1.5V	$C_{L(1.5V)}$ = 0.1 µF $I_{o(1.5V)}$ = 0 A	0.02		1.0	
		VIN_3.3V to VO_3.3V	$C_{L(3.3V)}$=100µF R_L = VO_3.3V/1.0 A	0.05		1.0	
		VIN_3.3V$_{AUX}$ to VO_V$_{AUX}$	$C_{L(3.3V)}$ = 100 µF R_L = VO_V$_{AUX}$/0.25 A	0.05		1.0	
		VIN_1.5V to VO_1.5V	$C_{L(3.3V)}$ = 100µF R_L = VO_1.5V/0.5 A	0.05		1.0	

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 4. QFN16 (3 x 3 mm) package outline

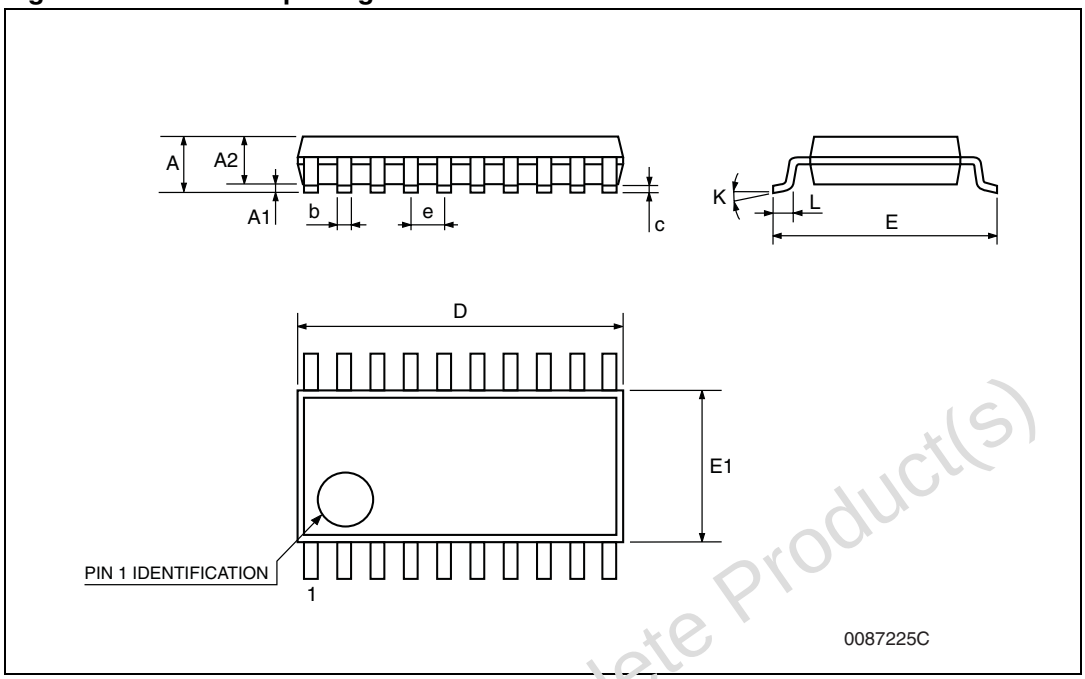


1. Drawing not to scale.

Table 13. QFN16 (3 x 3 mm) mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1		0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D		3.00	
D2	1.55	1.70	1.80
E		3.00	
E2	1.55	1.70	1.80
e		0.50	
K		0.20	
L	0.30	0.40	0.50
r		0.09	

Figure 5. TSSOP20 package outline



1. Drawing not to scale.

Table 14. TSSOP20 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			1.2
A1	0.05		0.15
A2	0.8	1	1.05
b	0.19		0.30
c	0.09		0.20
D	6.4	6.5	6.6
E	6.2	6.4	6.6
E1	4.3	4.4	4.48
e		0.65 BSC	
K	0°		8°
L	0.45	0.60	0.75

9 Revision history

Table 15. Document revision history

Date	Revision	Change
02-Aug-2006	1	First release
08-Feb-2007	2	Replaced TSSOP24 package information with QFN16
18-Oct-2007	3	Modified title, added R_{SW} values for QFN16 in *Table 7 on page 10*, small text changes, layout restructure, content reworked to improve readability in *Section 4.1: Power states description on page 9*, modified *Figure 2: STMEC001 block diagram on page 6*
17-Apr-2008	4	Modified: *Figure 2* and *Table 2: Pin assignments on page 4* and *Table 5: Power states on page 9*, minor text changes.
14-Nov-2008	5	Modified: *Figure 1: STMEC001 pin configuration (top view) on page 3*, *Table 2: Pin assignments on page 4*, removed "inches" colums from *Table 13: QFN16 (3 x 3 mm) mechanical data on page 16* and *Table 14: TSSOP20 mechanical data on page 17*.

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