



## Wireless Components

2 Band TV Tuner Mixer-Oscillator-PLL  
with unbalanced IF-Amplifier

KTS6027-2, KTS6029-2 Version 2.0

Specification July 2001

| Revision History: Current Version: Preliminary Datasheet V 1.1, July 2000 |                                 |                                                                                                                                   |
|---------------------------------------------------------------------------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Previous Version:Target Data Sheet                                        |                                 |                                                                                                                                   |
| Page<br>(in previous<br>Version)                                          | Page<br>(in current<br>Version) | Subjects (major changes since last revision)                                                                                      |
| all                                                                       | all                             | version to 1.1, status to preliminary                                                                                             |
| 4 - 2                                                                     | 4 - 2                           | circuit diagram modified                                                                                                          |
| 4 - 3                                                                     | 4 - 3                           | circuit diagram modified                                                                                                          |
| 5 - 2                                                                     | 5 - 2                           | Bus input/output SDA max changed to 6V,<br>Bus input SCL max changed to 6V,<br>ADC input added                                    |
| 5 - 3                                                                     | 5 - 3                           | new reference for ESD protection                                                                                                  |
| 5 - 5                                                                     | 5 - 5                           | Current consumption for LOW/MID band and HIGH band added,<br>tbf's replaced by data<br>Charge Pump output voltage VCP = 1.3 V min |
| 5 - 8                                                                     | 5 - 8                           | Oscillator phsase noise -85 dBc/Hz min, -89 dBc/Hz typ                                                                            |
| 5 - 9                                                                     | 5 - 9                           | Oscillator phsase noise -85 dBc/Hz min, -89 dBc/Hz typ                                                                            |

| Revision History: Current Version: Datasheet, V 2.0, July 2001 |                                 |                                              |
|----------------------------------------------------------------|---------------------------------|----------------------------------------------|
| Previous Version:Preliminary Datasheet V 1.1, July 2000        |                                 |                                              |
| Page<br>(in previous<br>Version)                               | Page<br>(in current<br>Version) | Subjects (major changes since last revision) |
| all                                                            | all                             | version to 2.0, preliminary deleted          |
| 5 - 2                                                          | 5- 2                            | definition of thermal properties changed     |
| 5 - 5                                                          | 5 - 5                           | current consumption changed                  |

ABM®, AOP®, ARCOFI®, ARCOFI®-BA, ARCOFI®-SP, DigiTape®, EPIC®-1, EPIC®-S, ELIC®, FALC®54, FALC®56, FALC®-E1, FALC®-LH, IDEC®, IOM®, IOM®-1, IOM®-2, IPAT®-2, ISAC®-P, ISAC®-S, ISAC®-S TE, ISAC®-P TE, ITAC®, IWE®, MUSAC®-A, OCTAT®-P, QUAT®-S, SICAT®, SICOFI®, SICOFI®-2, SICOFI®-4, SICOFI®-4µC, SLICOFI® are registered trademarks of Infineon Technologies AG.

ACE™, ASM™, ASP™, POTSWIRE™, QuadFALC™, SCOUT™ are trademarks of Infineon Technologies AG.

#### Edition 03.99

Published by Infineon Technologies AG

Balanstraße 73,  
81541 München

© Infineon Technologies AG 30.08.01.

All Rights Reserved.

#### Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies AG is an approved CECC manufacturer.

#### Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

#### Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components<sup>1</sup> of the Infineon Technologies AG, may only be used in life-support devices or systems<sup>2</sup> with the express written approval of the Infineon Technologies AG.

- 1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.
- 2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

## Product Info

### General Description

The **KTS6027-2/KTS6029-2** is a 5 V mixer/oscillator and synthesizer for analog and digital TV and VCR tuners.

### Features

#### General

- Suitable for analog and digital terrestrial TV tuner
- Compatible with KTS6027-S or KTS6029-S in normal mode
- New features in extended mode
- Full ESD protection

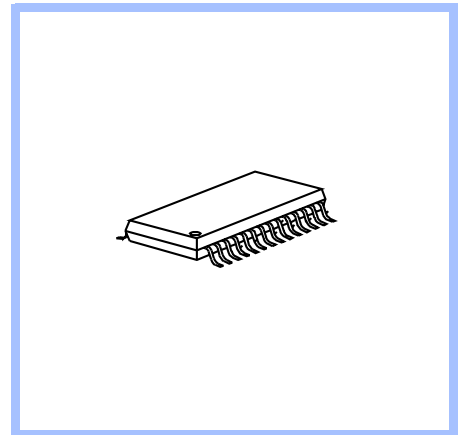
#### Mixer/Oscillator

- High impedance mixer input for LOW/MID band
- Low impedance mixer input for HIGH band
- 4 pin oscillator for LOW/MID band
- 4 pin oscillator for HIGH band

#### IF-Amplifier

- single ended IF preamplifier
- 75  $\Omega$  output impedance

### Package



### PLL

- PLL with short lock-in time
- High voltage VCO tuning output
- Fast I<sup>2</sup>C bus
- 4 NPN bandswitch buffers
- Internal LOW-MID/HIGH switch
- Lock-in flag
- Power-down reset
- 4 programmable reference divider ratios: 24, 64, 80, 128
- 4 programmable charge pump currents

### Application

- The IC is suitable for NTSC tuners in TV- and VCR-sets or CATV set-top receivers for analog and digital (ATSC) TV.

### Ordering Information

| Type      | Ordering Code                 | Package      |
|-----------|-------------------------------|--------------|
| KTS6027-2 | Q67037-A1162 ( tape and reel) | P-TSSOP-28-1 |
| KTS6029-2 | Q67037-A1163 ( tape and reel) | P-TSSOP-28-1 |

# 1 Table of Contents

|          |                                                        |            |
|----------|--------------------------------------------------------|------------|
| <b>1</b> | <b>Table of Contents</b>                               | <b>1-1</b> |
| <b>2</b> | <b>Product Description</b>                             | <b>2-1</b> |
| 2.1      | General Description                                    | 2-2        |
| 2.2      | Features                                               | 2-2        |
| 2.3      | Application                                            | 2-3        |
| 2.4      | Package Outlines                                       | 2-3        |
| <b>3</b> | <b>Functional Description</b>                          | <b>3-1</b> |
| 3.1      | Pin Configuration                                      | 3-2        |
| 3.2      | Internal Pin Configuration                             | 3-3        |
| 3.3      | Block Diagram                                          | 3-8        |
| 3.4      | Circuit Description                                    | 3-9        |
| <b>4</b> | <b>Applications</b>                                    | <b>4-1</b> |
| 4.1      | KTS6027-2 Evaluation Board                             | 4-2        |
| 4.2      | KTS6029-2 Evaluation Board                             | 4-3        |
| <b>5</b> | <b>Reference</b>                                       | <b>5-1</b> |
| 5.1      | Electrical Data                                        | 5-2        |
| 5.1.1    | Absolute Maximum Ratings                               | 5-2        |
| 5.1.2    | Operating Range                                        | 5-4        |
| 5.1.3    | AC/DC Characteristics                                  | 5-5        |
| 5.2      | Programming                                            | 5-10       |
| 5.3      | I2C Bus Timing Diagram                                 | 5-14       |
| 5.4      | Test Circuits                                          | 5-15       |
| 5.4.1    | Gain (GV) test Set-up in LOW/MID                       | 5-15       |
| 5.4.2    | Gain (GV) test Set-up in HIGH                          | 5-15       |
| 5.4.3    | Matching circuit for optimum noise figure in LOW/MID   | 5-16       |
| 5.4.4    | Noise Figure Test Set-up in LOW/MID                    | 5-16       |
| 5.4.5    | Noise Figure Test Set-up in HIGH                       | 5-17       |
| 5.4.6    | Cross modulation Test Set-up in LOW/MID band           | 5-17       |
| 5.4.7    | Cross modulation Test Set-up in HIGH band              | 5-18       |
| 5.4.8    | Measurement of $f_{ref}$ and $f_{div}$                 | 5-18       |
| 5.5      | Electrical Diagrams                                    | 5-19       |
| 5.5.1    | Input admittance (S11) of the LOW/MID band mixer input | 5-19       |
| 5.5.2    | Input impedance (S11) of the HIGH band mixer input     | 5-19       |
| 5.5.3    | Output admittance (S22) of the Mixer output            | 5-20       |
| 5.5.4    | Output impedance (S22) of the IF output                | 5-20       |

# 2

## Product Description

### Contents of this Chapter

|     |                               |     |
|-----|-------------------------------|-----|
| 2.1 | General Description . . . . . | 2-6 |
| 2.2 | Features . . . . .            | 2-6 |
| 2.3 | Application . . . . .         | 2-7 |
| 2.4 | Package Outlines . . . . .    | 2-7 |

## 2.1 General Description

The **KTS6027-2, KTS6029-2** device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in TV and VCR tuners.

The PLL block with four selectable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I<sup>2</sup>C bus. The device has four output ports. A flag is set when the loop is locked. It can be read by the processor via the I<sup>2</sup>C bus.

The mixer-oscillator block includes two balanced mixers (one mixer with high-impedance input and one mixer with a balanced low-impedance input), two frequency and amplitude-stable balanced oscillators for LOW/MID and HIGH, an IF amplifier, a low-noise reference voltage source, and a band switch.

## 2.2 Features

### General

- Suitable for analog and ATSC TV tuners
- Compatible with KTS6027-S or KTS6029-S in normal mode
- New features in extended mode
- Full ESD protection

### Mixer/Oscillator

- High impedance mixer input for LOW/MID band
- Low impedance mixer input for HIGH band
- 4 pin oscillator for LOW/MID band
- 4 pin oscillator for HIGH band

### IF-Amplifier

- single ended IF preamplifier
- 75  $\Omega$  output impedance

### PLL

- PLL with short lock-in time
- High voltage VCO tuning output
- Fast I<sup>2</sup>C bus
- 4 NPN bandswitch buffers
- Internal LOW-MID/HIGH switch

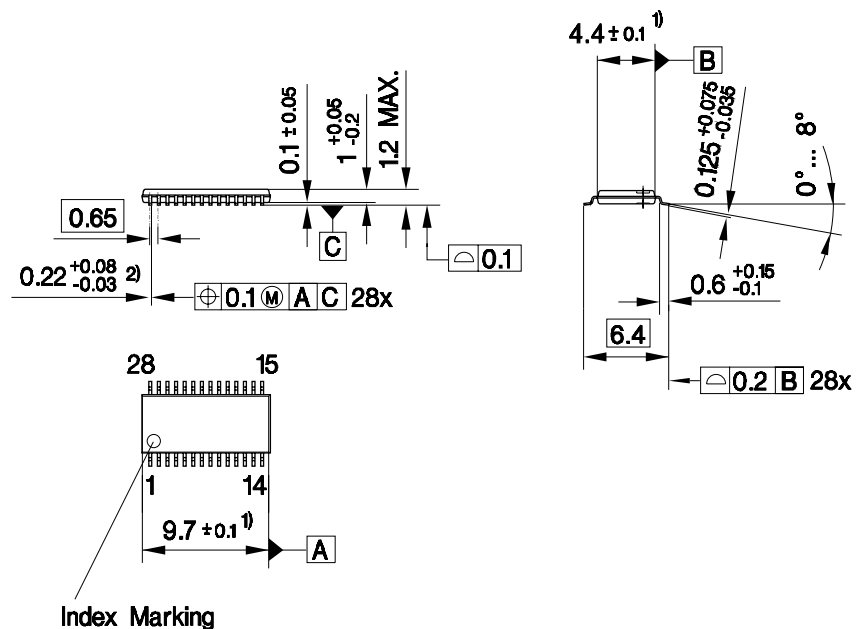
- Lock-in flag
- Power-down reset
- 4 programmable reference divider ratios: 24, 64, 80, 128
- 4 programmable charge pump currents

## 2.3 Application

- The IC is suitable for NTSC tuners in TV- and VCR-sets or CATV set-top receivers for analog and digital (ATSC) TV.

## 2.4 Package Outlines

P-TSSOP-28-1



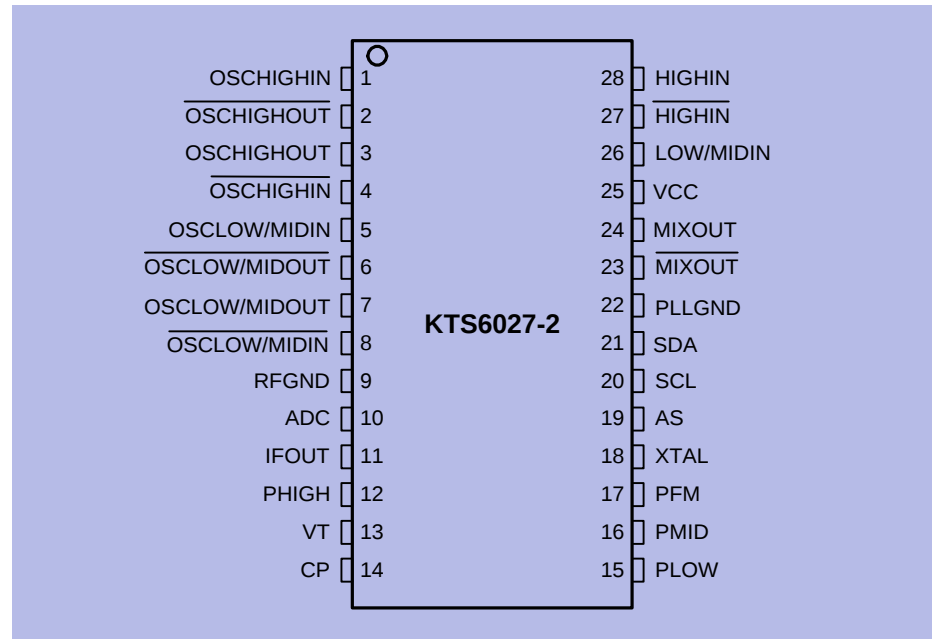
- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

# 3 Functional Description

## Contents of this Chapter

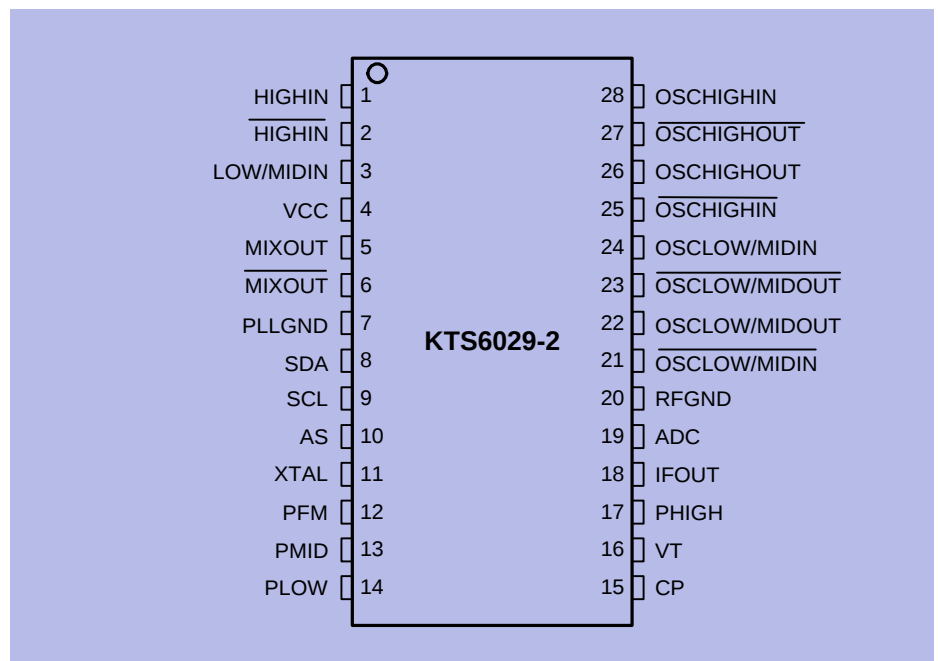
|       |                                      |      |
|-------|--------------------------------------|------|
| 3.1   | Pin Configuration . . . . .          | 3-9  |
| 3.2   | Internal Pin Configuration . . . . . | 3-10 |
| 3.3   | Block Diagram . . . . .              | 3-15 |
| 3.4   | Circuit Description. . . . .         | 3-16 |
| 3.4.1 | General . . . . .                    | 3-16 |
| 3.4.2 | Mixer-Oscillator block . . . . .     | 3-16 |
| 3.4.3 | PLL block . . . . .                  | 3-16 |
| 3.4.4 | I2C-Bus Interface . . . . .          | 3-17 |

### 3.1 Pin Configuration



KTS6027-2\_Pin\_config

Figure 3-1 KTS6027-2 Pin Configuration



KTS6029-2\_Pin\_config

Figure 3-2 KTS6029-2 Pin Configuration

## 3.2 Internal Pin Configuration

Note: Pin designation refers to KTS6027-2. KTS6029-2 has reversed pinning

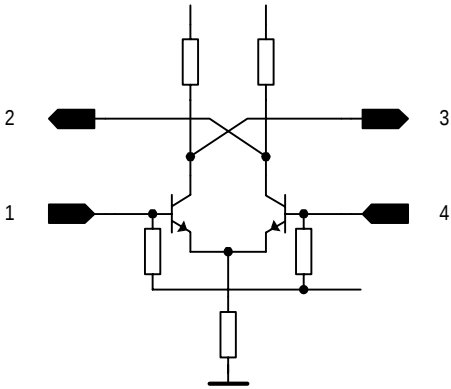
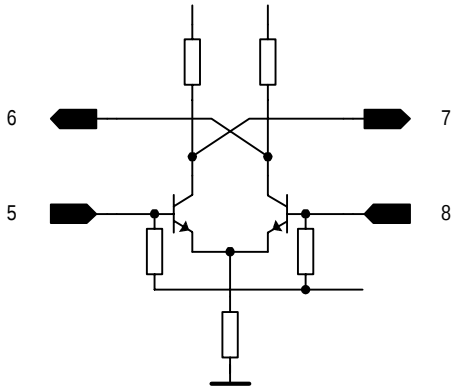
| Table 3-1 Pin Definition and Function |                                                     |                                                                                      |                    |       |
|---------------------------------------|-----------------------------------------------------|--------------------------------------------------------------------------------------|--------------------|-------|
| Pin No.                               | Symbol                                              | Equivalent I/O-Schematic                                                             | Average DC voltage |       |
|                                       |                                                     |                                                                                      | LOW/MID            | HIGH  |
| 1                                     | OSCHIGHIN                                           |   | 0.0 V              | 1.6 V |
| 2                                     | $\overline{\text{OSC-HIGHOUT}}$                     |                                                                                      | 0.0 V              | 2.8 V |
| 3                                     | OSC-HIGHOUT                                         |                                                                                      | 0.0 V              | 2.8 V |
| 4                                     | $\overline{\text{OSCHIGHIN}}$                       |                                                                                      | 0.0 V              | 1.6 V |
| 5                                     | OSCLOW/<br>MIDIN                                    |  | 1.6 V              | 0.0 V |
| 6                                     | $\overline{\text{OSCLOW/}}\overline{\text{MIDOUT}}$ |                                                                                      | 2.3 V              | 0.0 V |
| 7                                     | OSCLOW/<br>MIDOUT                                   |                                                                                      | 2.3 V              | 0.0 V |
| 8                                     | $\overline{\text{OSCLOW/}}\overline{\text{MIDIN}}$  |                                                                                      | 1.6 V              | 0.0 V |
| 9                                     | RFGND                                               | analog ground                                                                        | 0.0 V              | 0.0 V |

Table 3-1 Pin Definition and Function (continued)

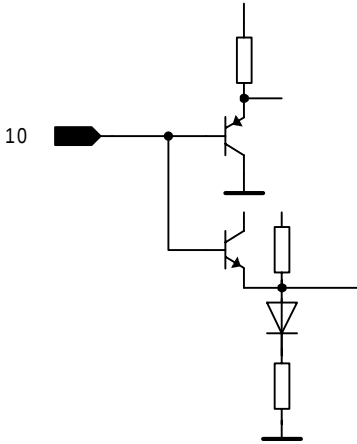
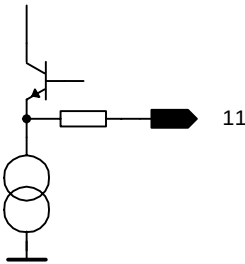
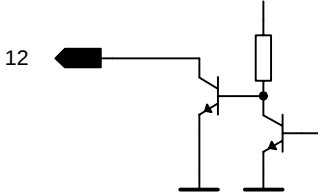
| Pin No. | Symbol | Equivalent I/O-Schematic                                                            | Average DC voltage |           |
|---------|--------|-------------------------------------------------------------------------------------|--------------------|-----------|
|         |        |                                                                                     | LOW/MID            | HIGH      |
| 10      | ADC    |   | $V_{ADC}$          | $V_{ADC}$ |
| 11      | IFOUT  |  | 2.3 V              | 2.3 V     |
| 12      | PHIGH  |  | 5.0 V              | $V_{CE}$  |

Table 3-1 Pin Definition and Function (continued)

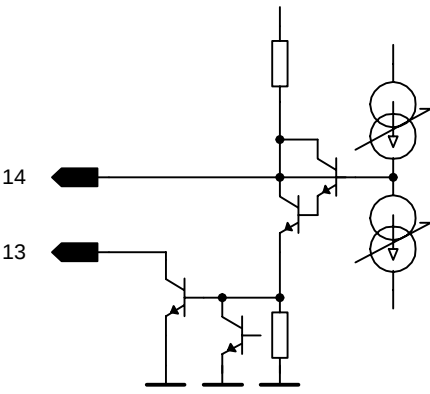
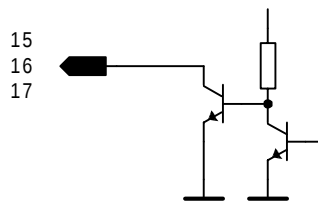
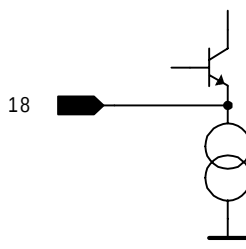
| Pin No. | Symbol | Equivalent I/O-Schematic                                                            | Average DC voltage |                 |
|---------|--------|-------------------------------------------------------------------------------------|--------------------|-----------------|
|         |        |                                                                                     | LOW/MID            | HIGH            |
| 13      | VT     |   | $V_T$              | $V_T$           |
| 14      | CP     |                                                                                     | 2.1 V              | 2.1 V           |
| 15      | PLOW   |  | 5 V or $V_{CE}$    | 5 V             |
| 16      | PMID   |                                                                                     | 5 V or $V_{CE}$    | 5 V             |
| 17      | PFM    |                                                                                     | 5 V or $V_{CE}$    | 5 V or $V_{CE}$ |
| 18      | XTAL   |  | 3.0 V              | 3.0 V           |

Table 3-1 Pin Definition and Function (continued)

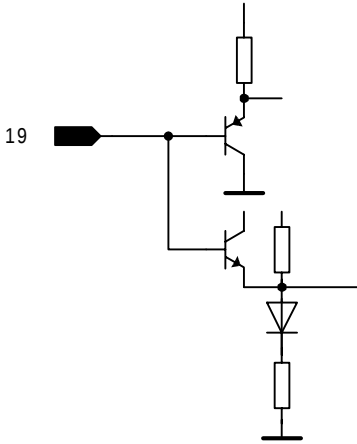
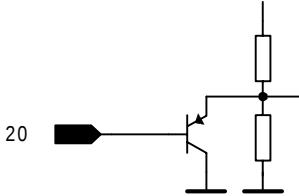
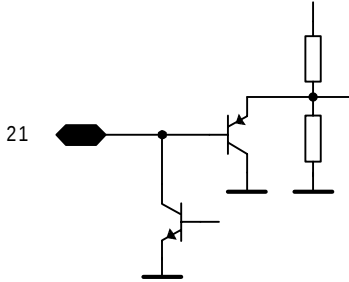
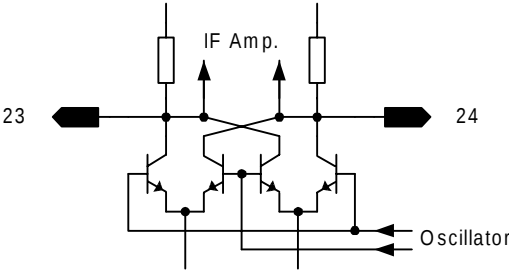
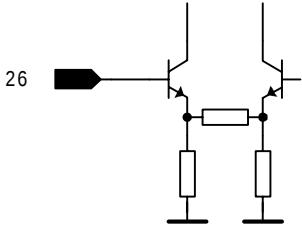
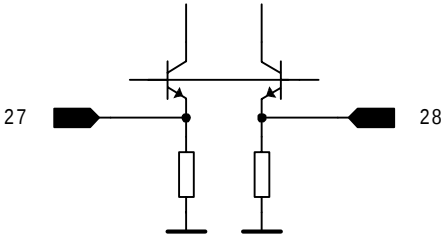
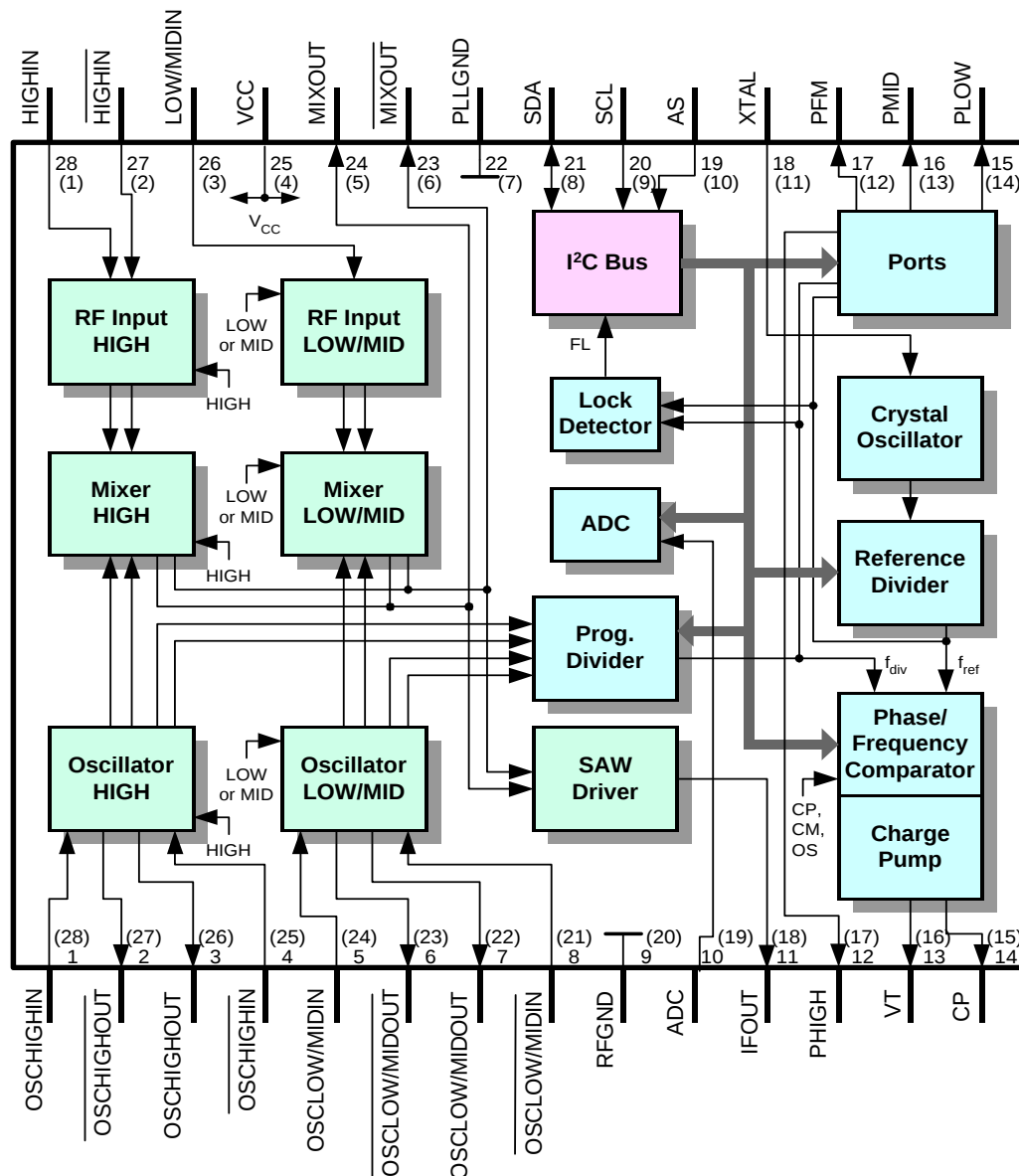
| Pin No. | Symbol | Equivalent I/O-Schematic                                                            | Average DC voltage |          |
|---------|--------|-------------------------------------------------------------------------------------|--------------------|----------|
|         |        |                                                                                     | LOW/MID            | HIGH     |
| 19      | AS     |   | $V_{AS}$           | $V_{AS}$ |
| 20      | SCL    |  | n.a.               | n.a.     |
| 21      | SDA    |  | n.a.               | n.a.     |
| 22      | PLLGND | digital ground                                                                      | 0.0 V              | 0.0 V    |

Table 3-1 Pin Definition and Function (continued)

| Pin No. | Symbol                     | Equivalent I/O-Schematic                                                             | Average DC voltage |       |
|---------|----------------------------|--------------------------------------------------------------------------------------|--------------------|-------|
|         |                            |                                                                                      | LOW/MID            | HIGH  |
| 23      | $\overline{\text{MIXOUT}}$ |    | 3.8 V              | 3.8 V |
| 24      | MIXOUT                     |                                                                                      | 3.8 V              | 3.8 V |
| 25      | VCC                        | supply voltage                                                                       | 5.0 V              | 5.0 V |
| 26      | LOW/MIDIN                  |    | 1.8 V              | 0.0 V |
| 27      | $\overline{\text{HIGHIN}}$ |                                                                                      | 0.0 V              | 0.9 V |
| 28      | HIGHIN                     |  | 0.0 V              | 0.9 V |

### 3.3 Block Diagram



KTS602729\_block\_diag

Note: Pin designations in parenthesis refer to KTS6029-2

Figure 3-3 Block Diagram

## 3.4 Circuit Description

### 3.4.1 General

In the **normal** mode (see Table 5-7 Test modes on page 32) the IC is compatible with KTS6027-S / KTS6029-S. An **extended** mode makes a reference divider ratio of 24 (see Table 5-8 Reference divider ratio on page 32) and two additional charge pump currents (see Table 5-9 Charge pump current on page 33) available.

### 3.4.2 Mixer-Oscillator block

The mixer oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for LOW and / or MID band and HIGH band, an IF amplifier, a reference voltage source and a band switch.

Filters between tuner input and IC separate the TV frequency signals into two bands. The band switching in the tuner front-end is done by using two or three port outputs. In the selected band the signal passes a tuner input stage with MOSFET amplifier, a double-tuned bandpass filter and is then fed to the balanced mixer input of the IC which has in case of LOW / MID a high-impedance input and in case of HIGH a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency which is filtered out at the balanced high-impedance output pair by means of a parallel tuned circuit. The following SAW preamplifier has a low output impedance to drive the SAW filter directly.

### 3.4.3 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio  $N = 256$  through 32767 and is then compared in a digital frequency / phase detector to a reference frequency  $f_{ref} = 31.25, 50, 62.5$  or 166.7 kHz.

This frequency is derived from an unbalanced, low-impedance 4 MHz crystal oscillator (pin XTAL) divided by  $R = 128, 80, 64$  or 24.

The phase detector has two outputs that drive two current sources of opposite polarity as charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the negative current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO

(internal amplifier, external pull-up resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits T0 = 1 and T1 = 0. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuitry. TUNE may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33 V .

By means of the control bits CP, CM, T0 and T1 the pump current can be switched between four values by software. This programmability permits alteration of the control response time of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software-switched ports PLOW, PMID, PHIGH and PFM are general-purpose open-collector outputs. The test bits T0 = 0 and T1 = 1 switches the test signals  $f_{ref}$  (i.e.  $f_{XTAL} / 64$ ) and  $f_{div}$  (divided input signal) to PLOW and PMID respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is wider than the period of the crystal oscillator (i.e. 250 ns). Hence, if FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P (K_{VCO} / f_{XTAL}) (C1+C2) / (C1C2)$$

where  $I_P$  is the charge pump current,  $K_{VCO}$  the VCO gain,  $f_{XTAL}$  the crystal oscillator frequency and C1, C2 the capacitances in the loop filter (see Figure 4-1 KTS6027-2 Evaluation Board on page 20). As the charge pump pulses at i.e. 62.5 kHz (=  $f_{ref}$ ), it takes a maximum of 16  $\mu$ s for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive  $f_{ref}$  periods. Therefore it takes between 128 and 144  $\mu$ s for FL to be set after the loop regains lock.

### 3.4.4 I<sup>2</sup>C-Bus Interface

Data is exchanged between the processor and the PLL via the I<sup>2</sup>C bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I<sup>2</sup>C bus.

The data from the processor pass through an I<sup>2</sup>C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH

while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The table "Bit Allocation" ([see Table 5-4 Bit Allocation Read / Write on page 31](#)) should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte.

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists the lock flag and the power-on flag.

Four different chip addresses can be set by appropriate DC level at pin AS ([see Table 5-6 Address selection on page 32](#)).

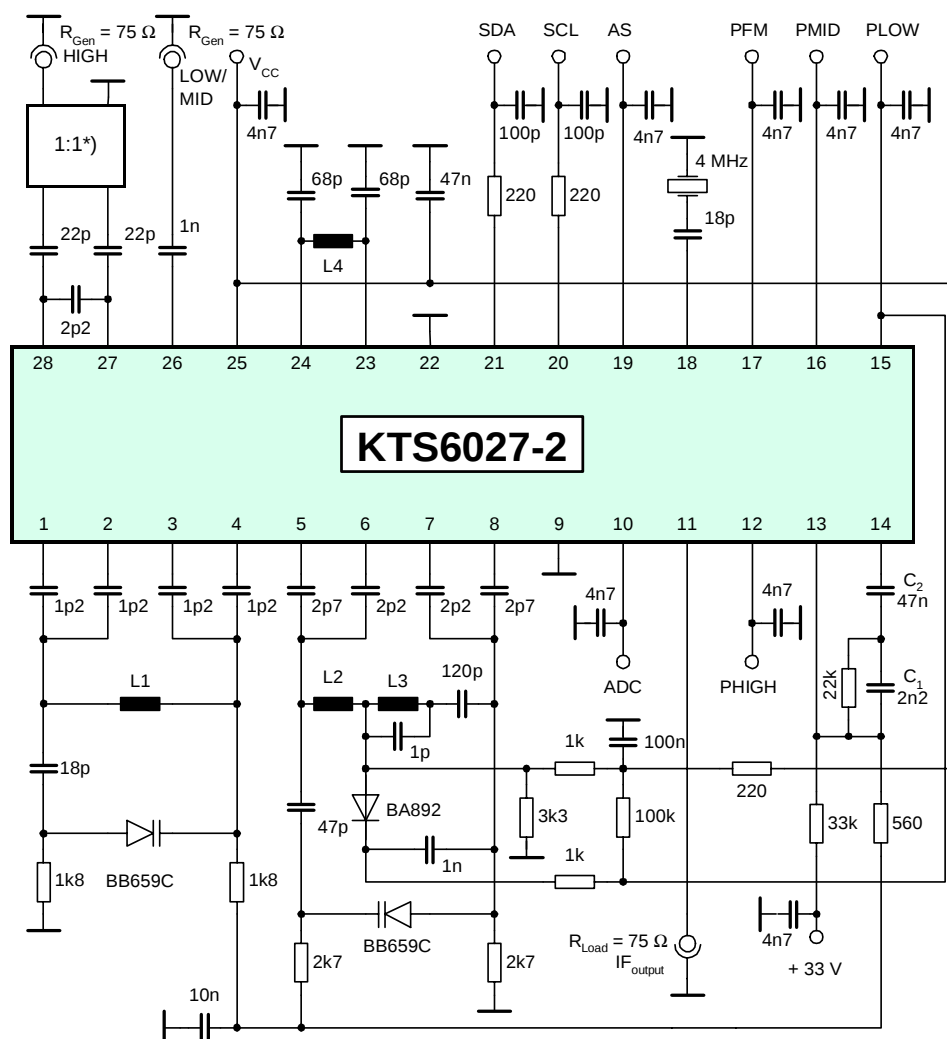
While applying the supply voltage, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and when  $V_{CC}$  falls below 3.2 V. It will be reset at the end of a READ operation.

# 4 Applications

## Contents of this Chapter

|     |                                      |     |
|-----|--------------------------------------|-----|
| 4.1 | KTS6027-2 Evaluation Board . . . . . | 4-2 |
| 4.2 | KTS6029-2 Evaluation Board . . . . . | 4-3 |

## 4.1 KTS6027-2 Evaluation Board



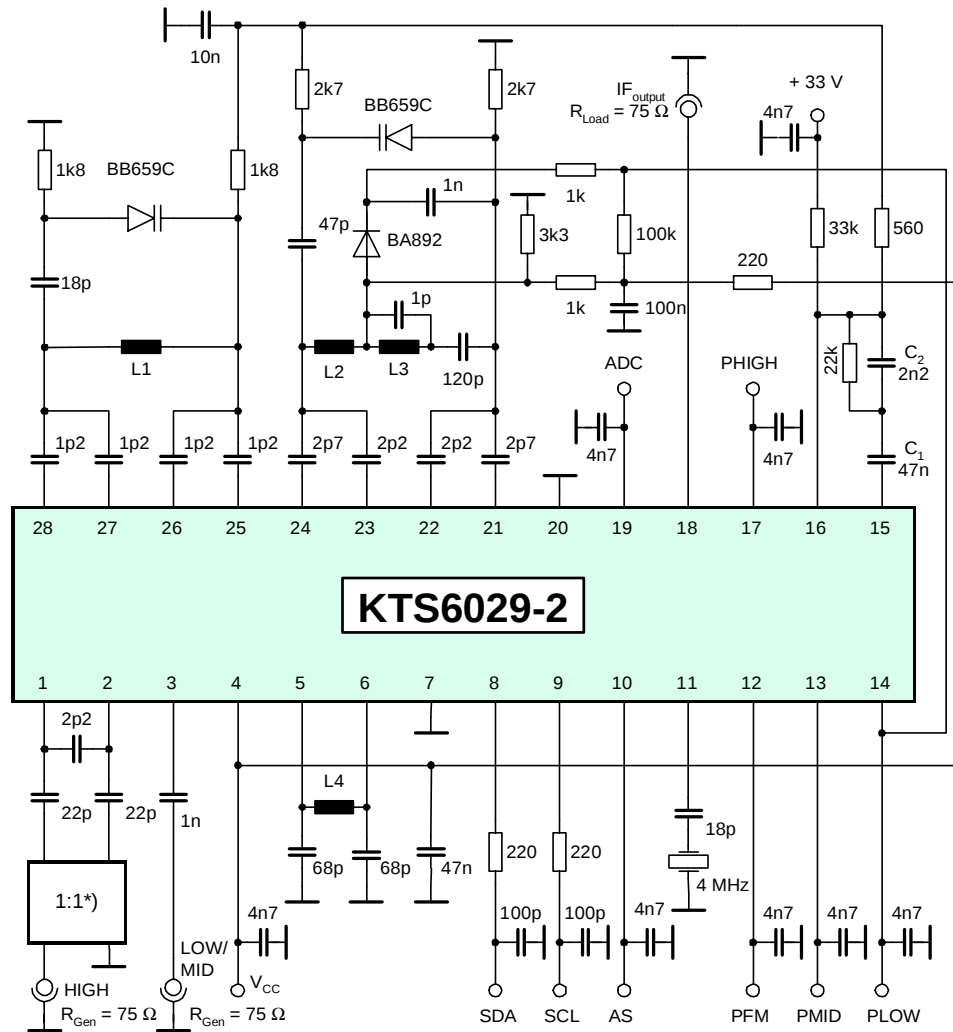
KTS6027-2 Application Circuit

Figure 4-1 KTS6027-2 Evaluation Board (NTSC)

| Table 4-1 Recommended band limits in MHz |          |        |            |     |
|------------------------------------------|----------|--------|------------|-----|
|                                          | RF input |        | Oscillator |     |
|                                          | min      | max    | min        | max |
| LOW                                      | 55.25    | 127.25 | 101        | 173 |
| MID                                      | 133.25   | 361.25 | 179        | 407 |
| HIGH                                     | 367.25   | 803.25 | 413        | 849 |

| Table 4-1 Coils |                          |        |        |
|-----------------|--------------------------|--------|--------|
|                 | turns                    | E      | wire E |
| L1              | 1.5                      | 2 mm   | 0.4 mm |
| L2              | 3.5                      | 2.5 mm | 0.5 mm |
| L3              | 9.5                      | 2.5 mm | 0.4 mm |
| L4              | 12.5                     | 3.5 mm | 0.3 mm |
| *)              | TOKO B4F Type 617DB-1023 |        |        |

## 4.2 KTS6029-2 Evaluation Board



KTS6029-2 Application Circuit

Figure 4-2 KTS6029-2 Evaluation Board (NTSC)

| Table 4-1 Recommended band limits in MHz |          |        |            |     |
|------------------------------------------|----------|--------|------------|-----|
|                                          | RF input |        | Oscillator |     |
|                                          | min      | max    | min        | max |
| LOW                                      | 55.25    | 127.25 | 101        | 173 |
| MID                                      | 133.25   | 361.25 | 179        | 407 |
| HIGH                                     | 367.25   | 803.25 | 413        | 849 |

| Table 4-1 Coils |                          |        |        |
|-----------------|--------------------------|--------|--------|
|                 | turns                    | E      | wire E |
| L1              | 1.5                      | 2 mm   | 0.4 mm |
| L2              | 3.5                      | 2.5 mm | 0.5 mm |
| L3              | 9.5                      | 2.5 mm | 0.4 mm |
| L4              | 12.5                     | 3.5 mm | 0.3 mm |
| *)              | TOKO B4F Type 617DB-1023 |        |        |

# 5

## Reference

### Contents of this Chapter

|            |                                                              |             |
|------------|--------------------------------------------------------------|-------------|
| <b>5.1</b> | <b>Electrical Data</b> .....                                 | <b>5-2</b>  |
| 5.1.1      | Absolute Maximum Ratings .....                               | 5-2         |
| 5.1.2      | Operating Range .....                                        | 5-4         |
| 5.1.3      | AC/DC Characteristics .....                                  | 5-5         |
| <b>5.2</b> | <b>Programming</b> .....                                     | <b>5-10</b> |
| Table 5-4  | Bit Allocation Read / Write .....                            | 5-10        |
| Table 5-5  | Description of symbols .....                                 | 5-10        |
| Table 5-6  | Address selection .....                                      | 5-11        |
| Table 5-7  | Test modes .....                                             | 5-11        |
| Table 5-8  | Reference divider ratio .....                                | 5-11        |
| Table 5-9  | Charge pump current .....                                    | 5-12        |
| Table 5-10 | Bandswitching .....                                          | 5-12        |
| Table 5-11 | A/D converter levels .....                                   | 5-13        |
| <b>5.3</b> | <b>I2C Bus Timing Diagram</b> .....                          | <b>5-14</b> |
| <b>5.4</b> | <b>Test Circuits</b> .....                                   | <b>5-15</b> |
| 5.4.1      | Gain (GV) test Set-up in LOW/MID .....                       | 5-15        |
| 5.4.2      | Gain (GV) test Set-up in HIGH .....                          | 5-15        |
| 5.4.3      | Matching circuit for optimum noise figure in LOW/MID .....   | 5-16        |
| 5.4.4      | Noise Figure Test Set-up in LOW/MID .....                    | 5-16        |
| 5.4.5      | Noise Figure Test Set-up in HIGH .....                       | 5-17        |
| 5.4.6      | Cross modulation Test Set-up in LOW/MID band .....           | 5-17        |
| 5.4.7      | Cross modulation Test Set-up in HIGH band .....              | 5-18        |
| 5.4.8      | Measurement of fref and fddiv .....                          | 5-18        |
| <b>5.5</b> | <b>Electrical Diagrams</b> .....                             | <b>5-19</b> |
| 5.5.1      | Input admittance (S11) of the LOW/MID band mixer input ..... | 5-19        |
| 5.5.2      | Input impedance (S11) of the HIGH band mixer input .....     | 5-19        |
| 5.5.3      | Output admittance (S22) of the Mixer output .....            | 5-20        |
| 5.5.4      | Output impedance (S22) of the IF output .....                | 5-20        |

## 5.1 Electrical Data

### 5.1.1 Absolute Maximum Ratings



#### WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

**Table 5-1 Absolute Maximum Ratings**

| Parameter <sup>1).</sup>                               | Symbol              | Limit Values |                          | Unit | Remarks                                 |
|--------------------------------------------------------|---------------------|--------------|--------------------------|------|-----------------------------------------|
|                                                        |                     | min          | max                      |      |                                         |
| Supply voltage                                         | V <sub>CC</sub>     | -0.3         | 6                        | V    |                                         |
| Ambient temperature                                    | T <sub>A</sub>      | -40          | T <sub>Amax</sub><br>2). | °C   |                                         |
| Junction temperature                                   | T <sub>J</sub>      |              | +125                     | °C   |                                         |
| Storage temperature                                    | T <sub>Stg</sub>    | -40          | +125                     | °C   |                                         |
| Temperature difference junction to case <sup>3).</sup> | T <sub>JC</sub>     |              | 2                        | K    |                                         |
| <b>PLL</b>                                             |                     |              |                          |      |                                         |
| CP                                                     | V <sub>CHGPMP</sub> | -0.3         | 3                        | V    |                                         |
|                                                        | I <sub>CHGPMP</sub> |              | 1                        | mA   |                                         |
| Crystal oscillator pin XTAL                            | V <sub>XTAL</sub>   |              | V <sub>CC</sub>          | V    |                                         |
|                                                        | I <sub>XTAL</sub>   | -5           |                          | mA   |                                         |
| Bus input/output SDA                                   | V <sub>SDA</sub>    | -0.3         | 6                        | V    |                                         |
| Bus output current SDA                                 | I <sub>SDA(L)</sub> |              | 5                        | mA   | open collector                          |
| Bus input SCL                                          | V <sub>SCL</sub>    | -0.3         | 6                        | V    |                                         |
| Chip address switch AS                                 | V <sub>AS</sub>     | -0.3         | V <sub>CC</sub>          | V    |                                         |
| VCO tuning output (loop filter)                        | V <sub>T</sub>      | -0.3         | 35                       | V    |                                         |
| ADC input                                              | V <sub>ADC</sub>    | -0.3         | V <sub>CC</sub>          | V    |                                         |
| Port outputs PLOW, PMID, PHIGH, PFM                    | V <sub>P</sub>      | -0.3         | V <sub>CC</sub>          | V    |                                         |
|                                                        | I <sub>P(L)</sub>   | -1           | 25                       | mA   | t <sub>max</sub> = 0.1 sec.<br>at 5.5 V |
| Total port output current                              | ΣI <sub>P(L)</sub>  |              | 40                       | mA   | t <sub>max</sub> = 0.1 sec.<br>at 5.5 V |

Table 5-1 Absolute Maximum Ratings

| Parameter <sup>1)</sup>        | Symbol           | Limit Values |     | Unit            | Remarks |  |
|--------------------------------|------------------|--------------|-----|-----------------|---------|--|
|                                |                  | min          | max |                 |         |  |
| Mixer-Oscillator               |                  |              |     |                 |         |  |
| Mix input LOW/MID              | V <sub>i</sub>   | -0.3         |     | 3               | V       |  |
| Mix inputs HIGH                | V <sub>i</sub>   |              |     | 2               | V       |  |
|                                | I <sub>i</sub>   | -5           |     | 6               | mA      |  |
| VCO base voltage               | V <sub>B</sub>   | -0.3         |     | 3               | V       |  |
| VCO collector voltage          | V <sub>C</sub>   |              |     | V <sub>CC</sub> | V       |  |
| ESD-Protection <sup>4)</sup> . |                  |              |     |                 |         |  |
| all pins                       | V <sub>ESD</sub> |              |     | 2               | kV      |  |

1). All values are referred to ground (pin), unless stated otherwise.

Currents with a positive sign flow into the pin and currents with a negative sign flow out of pin.

2).The maximum ambient temperature depends on the mounting conditions of the package. Any application mounting must guarantee not to exceed the maximum junction temperature of 125 °C. As reference the temperature difference junction to case is given.

3).Referred to top center of package

4). According to EIA/JESD22-A114-B (HBM incircuit test), as a single device incircuit contact discharge test.

### 5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

**Table 5-2 Operating Range**

| Parameter                           | Symbol   | Limit Values |                   | Unit | Test Conditions | L | Item |
|-------------------------------------|----------|--------------|-------------------|------|-----------------|---|------|
|                                     |          | min          | max               |      |                 |   |      |
| Supply voltage                      | $V_{CC}$ | +4.5         | +5.5              | V    |                 |   |      |
| Programmable divider factor         | N        | 256          | 32767             |      |                 |   |      |
| LOW/MID Mixer input frequency range | $f_i$    | 40           | 500               | MHz  |                 |   |      |
| HIGH Mixer input frequency range    | $f_i$    | 350          | 900               | MHz  |                 |   |      |
| LOW/MID Oscillator frequency range  | $f_O$    | 75           | 560               | MHz  |                 |   |      |
| HIGH Oscillator frequency range     | $f_O$    | 380          | 950               | MHz  |                 |   |      |
| Ambient temperature                 | $T_A$    | -20          | $T_{Amax}$<br>1). | °C   |                 |   |      |

1).see 5.1.1 Absolute Maximum Ratings on page 2

### 5.1.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

**Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ °C}$ ,  $V_{CC}$**

|                                                                    | Symbol            | Limit Values |       |         | Unit | Test Conditions                           | L | Item |
|--------------------------------------------------------------------|-------------------|--------------|-------|---------|------|-------------------------------------------|---|------|
|                                                                    |                   | min          | typ   | max     |      |                                           |   |      |
| Supply                                                             |                   |              |       |         |      |                                           |   |      |
| Supply voltage                                                     | V <sub>CC</sub>   | 4.5          | 5     | 5.5     | V    |                                           |   |      |
| Current consumption                                                | I <sub>CC</sub>   | 48           | 61    | 74      | mA   | LOW/MID band                              |   |      |
|                                                                    |                   | 51           | 65    | 79      | mA   | HIGH band                                 |   |      |
| Digital Unit                                                       |                   |              |       |         |      |                                           |   |      |
| PLL                                                                |                   |              |       |         |      |                                           |   |      |
| Crystal oscillator connections XTAL                                |                   |              |       |         |      |                                           |   |      |
| Crystal frequency                                                  | f <sub>XTAL</sub> | 3.2          | 4.0   | 4.8     | MHz  | series resonance                          |   |      |
| Crystal resistance                                                 | R <sub>XTAL</sub> | 10           |       | 100     | Ω    | series resonance                          |   |      |
| Oscillation frequency                                              | f <sub>XTAL</sub> | 3,99975      | 4,000 | 4,00025 | MHz  | f <sub>XTAL</sub> = 4 MHz                 |   |      |
| Input impedance                                                    | Z <sub>XTAL</sub> | -700         | -900  | -1100   | Ω    | f <sub>XTAL</sub> = 4 MHz                 |   |      |
| Charge pump output CP                                              |                   |              |       |         |      |                                           |   |      |
| Output current,<br>see Table 5-9 Charge<br>pump current on page 12 | ICPDH             | ± 430        | ± 650 | ± 860   | μA   | VCP = 1.8 V                               |   |      |
|                                                                    | ICPH              | ± 180        | ± 250 | ± 360   | μA   | VCP = 1.8 V                               |   |      |
|                                                                    | ICPDL             | ± 90         | ± 125 | ± 180   | μA   | VCP = 1.8 V                               |   |      |
|                                                                    | ICPL              | ± 35         | ± 50  | ± 70    | μA   | VCP = 1.8 V                               |   |      |
| Tristate current                                                   | ICPZ              |              | ± 1   |         | nA   | T0=1, T1=0                                |   |      |
| Output voltage                                                     | VCP               | 1.3          |       | 2.5     | V    | PLL locked                                |   |      |
| Drive output VT (open collector)                                   |                   |              |       |         |      |                                           |   |      |
| HIGH output current                                                | I <sub>TH</sub>   |              |       | 10      | μA   | V <sub>TH</sub> = 33 V, T0 = 1,<br>T1 = 0 |   |      |
| LOW output voltage                                                 | V <sub>TL</sub>   |              |       | 0.5     | V    | I <sub>TL</sub> = 1.0 mA                  |   |      |
| I <sup>2</sup> C-Bus                                               |                   |              |       |         |      |                                           |   |      |
| Bus inputs SCL, SDA                                                |                   |              |       |         |      |                                           |   |      |
| HIGH input voltage                                                 | V <sub>IH</sub>   | 3            |       | 5.5     | V    |                                           |   |      |
| LOW input voltage                                                  | V <sub>IL</sub>   | 0            |       | 1.5     | V    |                                           |   |      |
| HIGH input current                                                 | I <sub>IH</sub>   |              |       | 10      | μA   | V <sub>IH</sub> = V <sub>CC</sub>         |   |      |
| LOW input current                                                  | I <sub>IL</sub>   | -10          |       |         | μA   | V <sub>IL</sub> = 0 V                     |   |      |

Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC}$  (continued)

|                                                      | Symbol             | Limit Values |     |     | Unit | Test Conditions          | L | Item |
|------------------------------------------------------|--------------------|--------------|-----|-----|------|--------------------------|---|------|
|                                                      |                    | min          | typ | max |      |                          |   |      |
| Bus output SDA (open collector)                      |                    |              |     |     |      |                          |   |      |
| HIGH output current                                  | I <sub>OH</sub>    |              |     | 10  | μA   | V <sub>OH</sub> = 5.5 V  |   |      |
| LOW output voltage                                   | V <sub>OL</sub>    |              |     | 0.4 | V    | I <sub>OL</sub> = 3 mA   |   |      |
| Edge speed SCL,SDA                                   |                    |              |     |     |      |                          |   |      |
| Rise time                                            | t <sub>r</sub>     |              |     | 300 | ns   |                          |   |      |
| Fall time                                            | t <sub>f</sub>     |              |     | 300 | ns   |                          |   |      |
| Clock timing SCL                                     |                    |              |     |     |      |                          |   |      |
| Frequency                                            | f <sub>SCL</sub>   | 0            |     | 400 | kHz  |                          |   |      |
| HIGH pulse width                                     | t <sub>H</sub>     | 0.6          |     |     | μs   |                          |   |      |
| LOW pulse width                                      | t <sub>L</sub>     | 1.3          |     |     | μs   |                          |   |      |
| Start condition                                      |                    |              |     |     |      |                          |   |      |
| Set-up time                                          | t <sub>susta</sub> | 0.6          |     |     | μs   |                          |   |      |
| Hold time                                            | t <sub>hsta</sub>  | 0.6          |     |     | μs   |                          |   |      |
| Stop condition                                       |                    |              |     |     |      |                          |   |      |
| Set up time                                          | t <sub>susto</sub> | 0.6          |     |     | μs   |                          |   |      |
| Bus free                                             | t <sub>buf</sub>   | 1.3          |     |     | μs   |                          |   |      |
| Data transfer                                        |                    |              |     |     |      |                          |   |      |
| Set-up time                                          | t <sub>sudat</sub> | 0.1          |     |     | μs   |                          |   |      |
| Hold time                                            | t <sub>hdat</sub>  | 0            |     |     | μs   |                          |   |      |
| Input hysteresis SCL, SDA                            | V <sub>hys</sub>   |              | 200 |     | mV   |                          |   |      |
| Pulse width of spikes which are suppressed           | t <sub>sp</sub>    | 0            |     | 50  | ns   |                          |   |      |
| Capacitive load for each bus line                    | C <sub>L</sub>     |              |     | 400 | pF   |                          |   |      |
| Port outputs PLOW, PMID, PHIGH, PFM (open collector) |                    |              |     |     |      |                          |   |      |
| HIGH output current                                  | I <sub>POH</sub>   |              |     | 1   | μA   | V <sub>POH</sub> = 5 V   |   |      |
| LOW output voltage                                   | V <sub>POL</sub>   |              |     | 0.5 | V    | I <sub>POL</sub> = 25 mA |   |      |
| ADC port input                                       |                    |              |     |     |      |                          |   |      |
| HIGH input current                                   | I <sub>ADCH</sub>  |              |     | 10  | μA   |                          |   |      |
| LOW input current                                    | I <sub>ADCL</sub>  | -10          |     |     | μA   |                          |   |      |
| Address selection input AS                           |                    |              |     |     |      |                          |   |      |
| HIGH input current                                   | I <sub>ASH</sub>   |              |     | 50  | μA   | V <sub>ASH</sub> = 5 V   |   |      |
| LOW input current                                    | I <sub>ASL</sub>   | -50          |     |     | μA   | V <sub>ASL</sub> = 0 V   |   |      |

Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ °C}$ ,  $V_{CC}$  (continued)

|                                                                                                     | Symbol               | Limit Values |     |     | Unit | Test Conditions                                                                                                                                             | L | Item |
|-----------------------------------------------------------------------------------------------------|----------------------|--------------|-----|-----|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|---|------|
|                                                                                                     |                      | min          | typ | max |      |                                                                                                                                                             |   |      |
| Analog Unit                                                                                         |                      |              |     |     |      |                                                                                                                                                             |   |      |
| LOW/MID Band Section (including IF amplifier)                                                       |                      |              |     |     |      |                                                                                                                                                             |   |      |
| Voltage gain                                                                                        | G <sub>V</sub>       | 15           | 18  | 21  | dB   | f <sub>RF</sub> = 55.25 to 361.25 MHz, f <sub>IF</sub> = 41,25 to 58.75 MHz                                                                                 |   |      |
| Mixer noise figure                                                                                  | NF                   |              | 9   | 11  | dB   | f <sub>RF</sub> = 55.25 to 361.25 MHz                                                                                                                       |   |      |
| Output voltage causing 0.8 % of crossmodulation in channel,<br><a href="#">see 5.4.6 on page 17</a> | V <sub>o</sub>       |              | 109 |     | dBμV | f <sub>RFw</sub> = 55.25 MHz                                                                                                                                |   |      |
|                                                                                                     | V <sub>o</sub>       |              | 109 |     | dBμV | f <sub>RFw</sub> = 361.25 MHz                                                                                                                               |   |      |
| Input IP2                                                                                           | IP2                  |              | 140 |     | dBμV | f <sub>RF1</sub> = 55.25 MHz<br>f <sub>RF2</sub> = 111.00 MHz,<br>P <sub>RF1</sub> = P <sub>RF2</sub>                                                       |   |      |
|                                                                                                     | IP2                  |              | 135 |     | dBμV | f <sub>RF1</sub> = 361.25 MHz<br>f <sub>RF2</sub> = 723.00 MHz,<br>P <sub>RF1</sub> = P <sub>RF2</sub>                                                      |   |      |
| Input IP3                                                                                           | IP3                  |              | 110 |     | dBμV | f <sub>RF1</sub> = 55.25 MHz<br>f <sub>RF2</sub> = 60.75 MHz,<br>f <sub>RF2</sub> = 61.75 MHz,<br>P <sub>RF1</sub> = P <sub>RF2</sub> = P <sub>RF3</sub>    |   |      |
|                                                                                                     | IP3                  |              | 110 |     | dBμV | f <sub>RF1</sub> = 253.25 MHz<br>f <sub>RF2</sub> = 258.75 MHz,<br>f <sub>RF2</sub> = 259.75 MHz,<br>P <sub>RF1</sub> = P <sub>RF2</sub> = P <sub>RF3</sub> |   |      |
| Output voltage caus-<br>ing 1 dB compression                                                        | Vo                   |              | 115 |     | dBμV | f <sub>RF</sub> = 55.25 MHz                                                                                                                                 |   |      |
|                                                                                                     | Vo                   |              | 115 |     | dBμV | f <sub>RF</sub> = 361.25 MHz                                                                                                                                |   |      |
| Mixer input impedance                                                                               | R <sub>i</sub>       | 0.5          | 1   | 1.5 | kΩ   | parallel equivalent circuit, f <sub>RF</sub> = 100 MHz                                                                                                      |   |      |
|                                                                                                     | C <sub>i</sub>       |              | 2   | 3   | pF   | parallel equivalent circuit, f <sub>RF</sub> = 100 MHz                                                                                                      |   |      |
| Oscillator frequency shift, PLL unlocked                                                            | Δf <sub>Osc(V)</sub> |              |     | 400 | kHz  | V <sub>CC</sub> = 5 V ± 10 %                                                                                                                                |   |      |
| Oscillator frequency drift, PLL unlocked                                                            | Δf <sub>Osc(T)</sub> |              |     | 500 | kHz  | ΔT = 25 °C                                                                                                                                                  |   |      |
| Oscillator frequency drift, PLL unlocked                                                            | Δf <sub>Osc(t)</sub> |              |     | 100 | kHz  | t = 5 s up to 15 min after switching on                                                                                                                     |   |      |

Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC}$  (continued)

|                                                                                  | Symbol              | Limit Values |     |     | Unit       | Test Conditions                                                                                                                      | L | Item |
|----------------------------------------------------------------------------------|---------------------|--------------|-----|-----|------------|--------------------------------------------------------------------------------------------------------------------------------------|---|------|
|                                                                                  |                     | min          | typ | max |            |                                                                                                                                      |   |      |
| Oscillator pulling, PLL unlocked                                                 | $V_i$               | 100          | 108 |     | dB $\mu$ V | $\Delta f = 10\text{ kHz}$<br>$f_{RF} = 55.25\text{ MHz}$                                                                            |   |      |
|                                                                                  | $V_i$               | 100          | 108 |     | dB $\mu$ V | $\Delta f = 10\text{ kHz}$<br>$f_{RF} = 361.25\text{ MHz}$                                                                           |   |      |
| Oscillator phase noise <sup>1)</sup>                                             | $\Phi_{OSC}$        | -86          | -89 |     | dBc/Hz     | $f_m = 10\text{ kHz}$                                                                                                                |   |      |
| IF suppression                                                                   | $a_{IF}$            | 15           | 20  |     | dB         | $V_i = 80\text{ dB}\mu\text{V}$                                                                                                      |   |      |
| <b>HIGH Band Section (including IF amplifier)</b>                                |                     |              |     |     |            |                                                                                                                                      |   |      |
| Voltage gain                                                                     | $G_V$               | 26           | 29  | 32  | dB         | $f_{RF} = 367.25\text{ MHz}$ to $801.25\text{ MHz}$ ,<br>$f_{IF} = 41.25$ to $58.75\text{ MHz}$                                      |   |      |
| Mixer noise figure                                                               | NF                  |              | 6   | 9   | dB         | $f_{RF} = 367.25$ to $613.25\text{ MHz}$                                                                                             |   |      |
|                                                                                  |                     |              | 7   | 10  | dB         | $f_{RF} = 619.25$ to $801.25\text{ MHz}$                                                                                             |   |      |
| Output voltage causing 0.8 % of crossmodulation in channel, see 5.4.7 on page 18 | $V_o$               |              | 109 |     | dB $\mu$ V | $f_{RFW} = 403.25\text{ MHz}$                                                                                                        |   |      |
|                                                                                  | $V_o$               |              | 109 |     | dB $\mu$ V | $f_{RFW} = 775.25\text{ MHz}$                                                                                                        |   |      |
| Input IP2                                                                        | IP2                 |              | 130 |     | dB $\mu$ V | $f_{RF1} = 373.25\text{ MHz}$<br>$f_{RF2} = 747.00\text{ MHz}$ ,<br>$P_{RF1} = P_{RF2}$                                              |   |      |
| Input IP3                                                                        | IP3                 |              | 99  |     | dB $\mu$ V | $f_{RF1} = 503.25\text{ MHz}$<br>$f_{RF2} = 510.25\text{ MHz}$ ,<br>$f_{RF2} = 512.25\text{ MHz}$ ,<br>$P_{RF1} = P_{RF2} = P_{RF3}$ |   |      |
|                                                                                  | IP3                 |              | 99  |     | dB $\mu$ V | $f_{RF1} = 775.25\text{ MHz}$<br>$f_{RF2} = 780.75\text{ MHz}$ ,<br>$f_{RF2} = 781.75\text{ MHz}$ ,<br>$P_{RF1} = P_{RF2} = P_{RF3}$ |   |      |
| Output voltage causing 1 dB compression                                          | $V_o$               |              | 115 |     | dB $\mu$ V | $f_{RF} = 503.25\text{ MHz}$                                                                                                         |   |      |
|                                                                                  | $V_o$               |              | 115 |     | dB $\mu$ V | $f_{RF} = 799.25\text{ MHz}$                                                                                                         |   |      |
| Mixer input impedance                                                            | $R_i$               | 14           | 20  | 26  | $\Omega$   | serial equivalent circuit, $f_{RF} = 600\text{ MHz}$                                                                                 |   |      |
|                                                                                  | $L_i$               | 6            | 10  | 14  | nH         | serial equivalent circuit, $f_{RF} = 600\text{ MHz}$                                                                                 |   |      |
| Oscillator frequency shift, PLL unlocked                                         | $\Delta f_{OSC(V)}$ |              |     | 400 | kHz        | $V_{CC} = 5\text{ V} \pm 10\%$                                                                                                       |   |      |
| Oscillator frequency drift, PLL unlocked                                         | $\Delta f_{OSC(T)}$ |              |     | 800 | kHz        | $\Delta T = 25\text{ }^{\circ}\text{C}$                                                                                              |   |      |

Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC}$  (continued)

|                                                | Symbol                     | Limit Values |     |     | Unit       | Test Conditions                                                          | L | Item |
|------------------------------------------------|----------------------------|--------------|-----|-----|------------|--------------------------------------------------------------------------|---|------|
|                                                |                            | min          | typ | max |            |                                                                          |   |      |
| Oscillator frequency drift, PLL unlocked       | $\Delta f_{\text{Osc}(t)}$ |              |     | 100 | kHz        | t = 5 s up to 15 min after switching on                                  |   |      |
| Oscillator pulling, PLL unlocked               | $V_i$                      | 100          | 108 |     | dB $\mu$ V | $\Delta f$ = 10 kHz<br>$f_{\text{RF}}$ = 367.25 MHz                      |   |      |
|                                                |                            | 100          | 108 |     | dB $\mu$ V | $\Delta f$ = 10 kHz<br>$f_{\text{RF}}$ = 801.25 MHz                      |   |      |
| Oscillator phase noise <sup>1)</sup>           |                            | -86          | -89 |     | dBc/Hz     | fm = 10kHz                                                               |   |      |
| IF suppression                                 | $a_{\text{IF}}$            | 15           | 20  |     | dB         | $V_i$ = 80 dB $\mu$ V                                                    |   |      |
| SAW preamplifier                               |                            |              |     |     |            |                                                                          |   |      |
| IF output impedance                            | $R_{\text{IF}}$            |              |     | 80  | $\Omega$   | serial equivalent circuit,<br>$f_{\text{IF}}$ = 45.75 MHz                |   |      |
|                                                | $L_{\text{IF}}$            |              | 7   |     | nH         |                                                                          |   |      |
| Rejection at the IF outputs                    |                            |              |     |     |            |                                                                          |   |      |
| Divider interference rejection <sup>2)</sup> . | $V_o$                      |              |     | 30  | dB $\mu$ V |                                                                          |   |      |
| Channel CH6 beat <sup>3)</sup> .               | $\text{INT}_{\text{CH6}}$  | 70           |     |     | dBc        | $V_{\text{RFpix}}$ = 80 dB $\mu$ V<br>$V_{\text{RFSnd}}$ = 80 dB $\mu$ V |   |      |
| Channel A-5 beat rejection <sup>4)</sup> .     | $\text{INT}_{\text{CHA5}}$ | 70           |     |     | dBc        | $V_{\text{RFpix}}$ = 80 dB $\mu$ V                                       |   |      |

■ This value is only guaranteed in lab.

- 1). Measured in the evaluation board. (see Chapter 4)
- 2). This is the level of divider interferences close to the IF frequency. For example channel S3:  $f_{OSC} = 158.15\text{ MHz}$ ,  $1/4 f_{OSC} = 39.5375\text{ MHz}$ . Measured in the evaluation board. (see Chapter 4)
- 3). Channel 6 beat is the interfering product of  $f_{RFpix} + f_{RFSnd} - f_{OSC}$  of channel 6 at 42 MHz. Measured in the evaluation board. (see Chapter 4)
- 4). Channel A-5 beat is the interfering product of  $f_{RFPIX} + f_{RFSND} - f_{OSC}$  of channel A-5,  $f_{beat} = 45.5\text{ MHz}$ . The possible mechanisms are  $f_{OSC} - 2 \times f_{IF}$  or  $2 \times f_{RFpix} - f_{OSC}$ . Measured in the evaluation board. (see Chapter 4)

## 5.2 Programming

**Table 5-4 Bit Allocation Read / Write**

| Byte                           | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB | Ack |
|--------------------------------|-----|------|------|------|------|------|------|-----|-----|
| Write Data                     |     |      |      |      |      |      |      |     |     |
| Address Byte                   | 1   | 1    | 0    | 0    | 0    | MA1  | MA0  | 0   | A   |
| Progr. Divider Byte 1          | 0   | N14  | N13  | N12  | N11  | N10  | N9   | N8  | A   |
| Progr. Divider Byte 2          | N7  | N6   | N5   | N4   | N3   | N2   | N1   | N0  | A   |
| Control Byte                   | 1   | CP   | T1   | T0   | CM   | RSA  | RSB  | OS  | A   |
| Bandswitch Byte <sup>1).</sup> | x   | x    | x    | x    | P3   | P2   | P1   | P0  | A   |
| Read Data                      |     |      |      |      |      |      |      |     |     |
| Address Byte                   | 1   | 1    | 0    | 0    | 0    | MA1  | MA0  | 1   | A   |
| Status Byte                    | POR | FL   | x    | x    | x    | A2   | A1   | A0  | A   |

1). see Table 5-10 Bandswitching on page 12

**Table 5-5 Description of symbols**

| Symbol                                      | Description                                                                                                                            |
|---------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| MA0, MA1                                    | Address selection bits (see Table 5-6 Address selection on page 11)                                                                    |
| N14 to N0                                   | programmable divider bits:<br>$N = 2^{14} \times N14 + 2^{13} \times N13 + \dots + 2^3 \times N3 + 2^2 \times N2 + 2^1 \times N1 + N0$ |
| CP                                          | charge pump current: bit = 0: charge pump current = 50 $\mu$ A<br>bit = 1: charge pump current = 250 $\mu$ A                           |
| T1, T0                                      | test bits (see Table 5-7 Test modes on page 11)                                                                                        |
| CM                                          | charge pump mode bit (see Table 5-9 Charge pump current on page 12)                                                                    |
| RSA, RSB                                    | reference divider bits (see Table 5-8 Reference divider ratio on page 11)                                                              |
| OS                                          | tuning amplifier control bit: bit = 0: enable $V_T$<br>bit = 1: disable $V_T$                                                          |
| PLOW, PMID, PHIGH, PFM, see 5-10 on page 12 | NPN ports control bits: bit = 0: NPN open-collector output is inactive<br>bit = 1: NPN open-collector output is active                 |
| A0, A1, A2                                  | ADC bits (see Table 5-11 A/D converter levels on page 13)                                                                              |
| FL                                          | PLL lock flag bit = 1: loop is locked                                                                                                  |
| POR                                         | Power-on reset flag<br>flag is set at power-on and reset at the end of READ operation                                                  |
| x                                           | don't care                                                                                                                             |

Table 5-6 Address selection

| Voltage at AS                                 | MA1 | MA0 |
|-----------------------------------------------|-----|-----|
| (0...0.1) * V <sub>CC</sub>                   | 0   | 0   |
| (0.2...0.3) * V <sub>CC</sub> or open circuit | 0   | 1   |
| (0.4...0.6) * V <sub>CC</sub>                 | 1   | 0   |
| (0.9...1) * V <sub>CC</sub>                   | 1   | 1   |

Table 5-7 Test modes

| Test mode                                         | Mode                 | T1 | T0 |
|---------------------------------------------------|----------------------|----|----|
| Normal operation                                  | normal <sup>1)</sup> | 0  | 0  |
| Charge pump output, CP is in high-impedance state |                      | 0  | 1  |
| PMID = fdiv output, PLOW = fref output            |                      | 1  | 0  |
| Extended operation                                | extended             | 1  | 1  |

1). In this mode the IC is compatible with KTS6027-S / KTS6029-S

Table 5-8 Reference divider ratio

| Reference divider ratio | Mode <sup>1).</sup> | T1 | T0 | RSA | RSB | fref <sup>2).</sup> |
|-------------------------|---------------------|----|----|-----|-----|---------------------|
| 80                      | normal              | 0  | 0  | x   | 0   | 50 kHz              |
|                         |                     | 0  | 1  |     |     |                     |
|                         |                     | 1  | 0  |     |     |                     |
| 128                     |                     | 0  | 0  | 0   | 1   | 31.25 kHz           |
|                         |                     | 0  | 1  |     |     |                     |
|                         |                     | 1  | 0  |     |     |                     |
| 64                      |                     | 0  | 0  | 1   | 1   | 62.5 kHz            |
|                         |                     | 0  | 1  |     |     |                     |
|                         |                     | 1  | 0  |     |     |                     |
| 80                      | extended            | 1  | 1  | 0   | 0   | 50 kHz              |
| 128                     |                     |    |    | 0   | 1   | 31.25 kHz           |
| 24                      |                     |    |    | 1   | 0   | 166.7 kHz           |
| 64                      |                     |    |    | 1   | 1   | 62.5 kHz            |

1). see Table 5-7 Test modes on page 11

2). With a 4 MHz quartz.

Table 5-9 Charge pump current

| Charge pump current | Mode <sup>1)</sup> | CP | T1 | T0 | CM |
|---------------------|--------------------|----|----|----|----|
| 50 $\mu$ A          | normal             | 0  | 0  | 0  | x  |
| 250 $\mu$ A         |                    | 1  |    |    | x  |
| 50 $\mu$ A          | extended           | 0  | 1  | 1  | 0  |
| 125 $\mu$ A         |                    | 0  |    |    | 1  |
| 250 $\mu$ A         |                    | 1  |    |    | 0  |
| 600 $\mu$ A         |                    | 1  |    |    | 1  |

1). see Table 5-7 Test modes on page 11

Table 5-10 Bandswitching

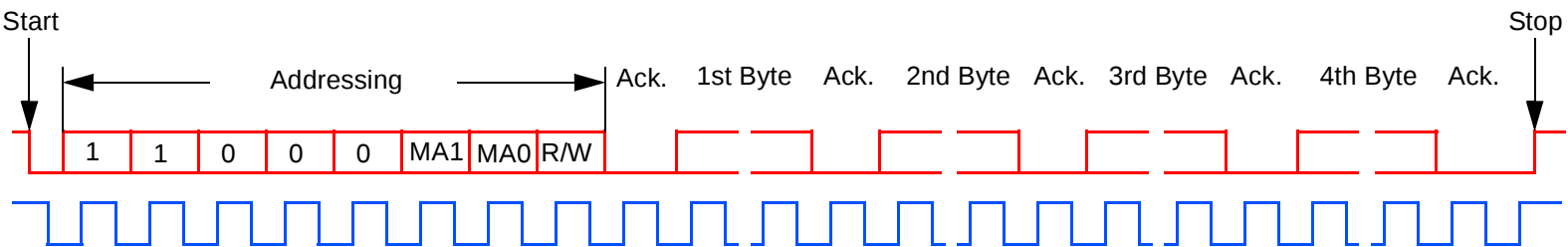
| Bit Designation     |        | P3 | P2 | P1 | P0 |
|---------------------|--------|----|----|----|----|
| Active Port         | Pin    |    |    |    |    |
| PHIGH <sup>1)</sup> | 12     | 0  | 0  | 0  | 0  |
| PLOW                | 15     | 0  | 0  | 0  | 1  |
| PMID                | 16     | 0  | 0  | 1  | 0  |
| not used            |        | 0  | 0  | 1  | 1  |
| PHIGH               | 12     | 0  | 1  | 0  | 0  |
| PLOW, PFM           | 15, 17 | 0  | 1  | 0  | 1  |
| PMID, PFM           | 16, 17 | 0  | 1  | 1  | 0  |
| not used            |        | 0  | 1  | 1  | 1  |
| PHIGH               | 12     | 1  | 0  | 0  | 0  |
| PLOW, PFM           | 15, 17 | 1  | 0  | 0  | 1  |
| PMID, PFM           | 16, 17 | 1  | 0  | 1  | 0  |
| not used            |        | 1  | 0  | 1  | 1  |
| PHIGH, PFM          | 12, 17 | 1  | 1  | 0  | 0  |
| PLOW, PFM           | 15, 17 | 1  | 1  | 0  | 1  |
| PMID, PFM           | 16, 17 | 1  | 1  | 1  | 0  |
| not used            |        | 1  | 1  | 1  | 1  |

1). Default after power-on

Table 5-11 A/D converter levels

| Voltage at ADC              | A2 | A1 | A0 |
|-----------------------------|----|----|----|
| $(0...0.15) \cdot V_{CC}$   | 0  | 0  | 0  |
| $(0.15...0.3) \cdot V_{CC}$ | 0  | 0  | 1  |
| $(0.3...0.45) \cdot V_{CC}$ | 0  | 1  | 0  |
| $(0.45...0.6) \cdot V_{CC}$ | 0  | 1  | 1  |
| $(0.6...1) \cdot V_{CC}$    | 1  | 0  | 0  |

## 5.3 I<sup>2</sup>C Bus Timing Diagram



### Telegram examples:

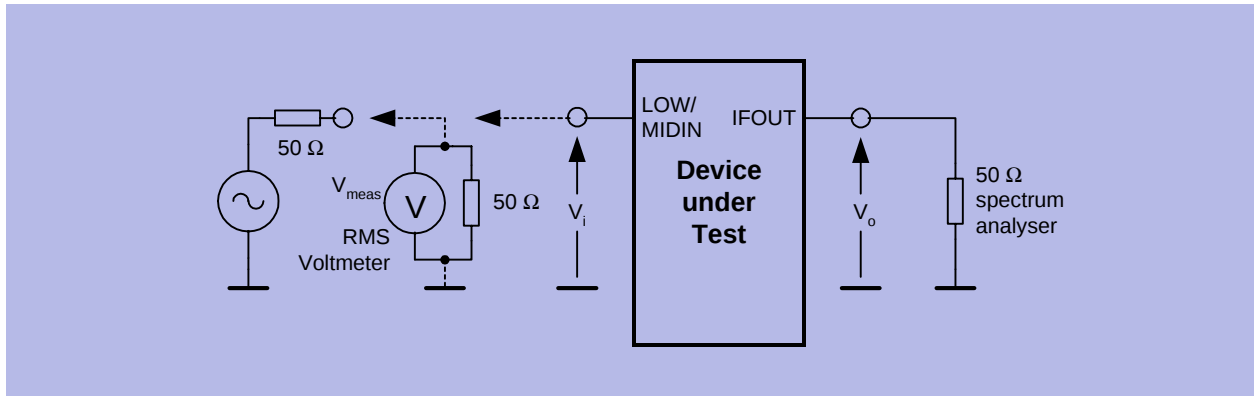
Start-ADB-DB1-DB2-CB-BB-Stop  
 Start-ADB-CB-BB-DB1-DB2-Stop  
 Start-ADB-DB1-DB2-Stop  
 Start-ADB-CB-BB-Stop

### Abbreviations:

Start= start condition  
 ADB= address byte  
 DB1= prog. divider byte 1  
 DB2= prog. divider byte 2  
 CB= Control byte  
 BB= Bandswitch byte  
 Stop= stop condition

## 5.4 Test Circuits

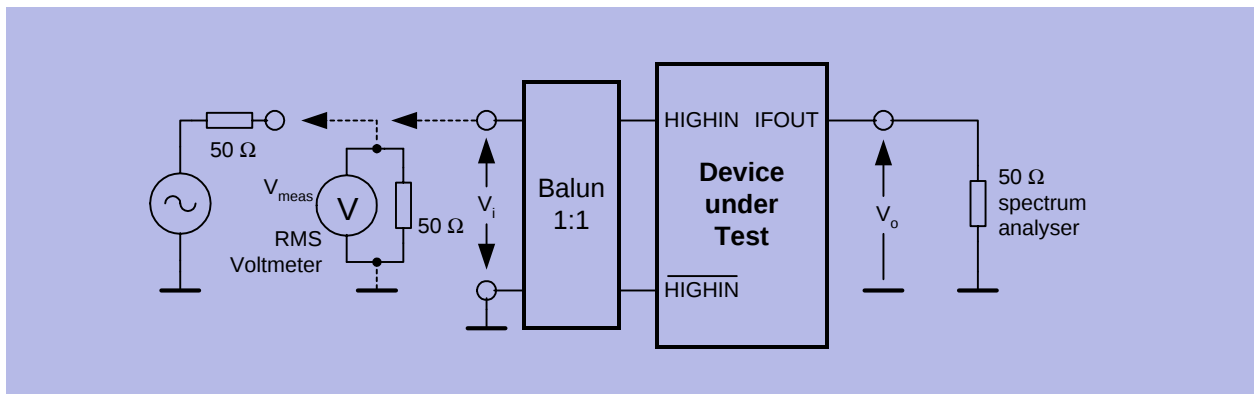
### 5.4.1 Gain ( $G_V$ ) test Set-up in LOW/MID



GVHFM

- $Z_i \gg 50 \Omega \Rightarrow V_i = 2 \times V_{\text{meas}} = 80 \text{ dB}\mu\text{V}$
- $V_i = V_{\text{meas}} + 6\text{dB} = 80 \text{ dB}\mu\text{V}$
- $G_V = 20 \log(V_o / V_i)$

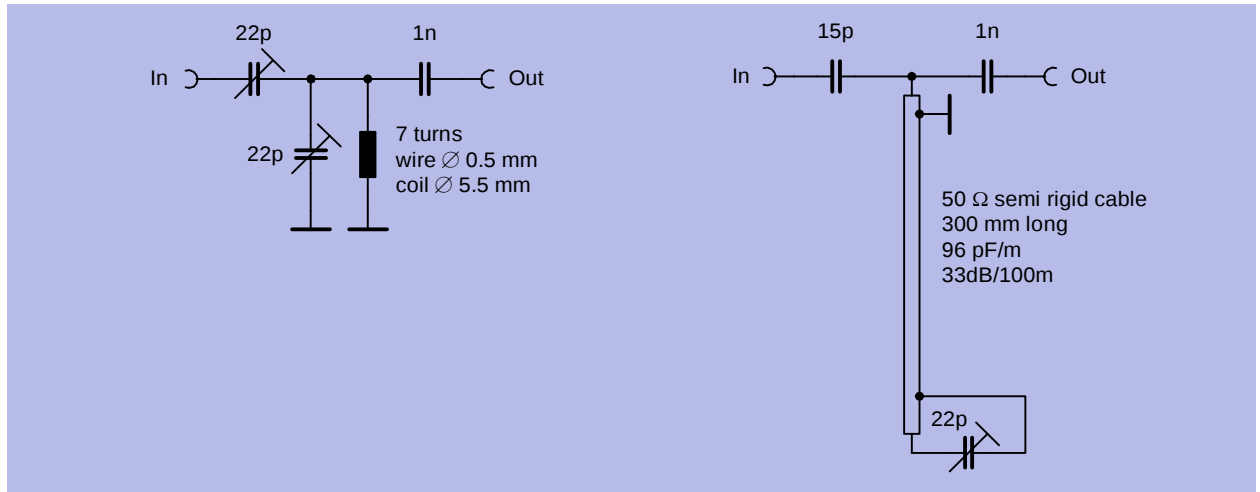
### 5.4.2 Gain ( $G_V$ ) test Set-up in HIGH



GUHFM

- $V_i = V_{\text{meas}} = 70 \text{ dB}\mu\text{V}$
- $G_V = 20 \log(V_o / V_i) + 1 \text{ dB}$  (1 dB = insertion loss of balun)

### 5.4.3 Matching circuit for optimum noise figure in LOW/MID



NFM

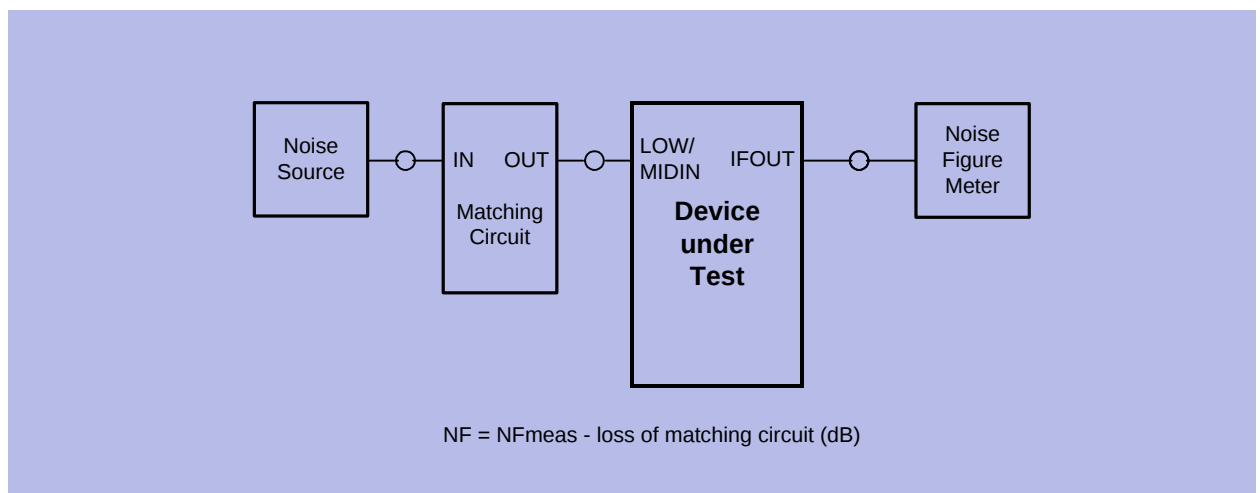
For  $f_{RF} = 50 \text{ MHz}$

- loss = 0 dB
- image suppression = 16 dB

For  $f_{RF} = 150 \text{ MHz}$

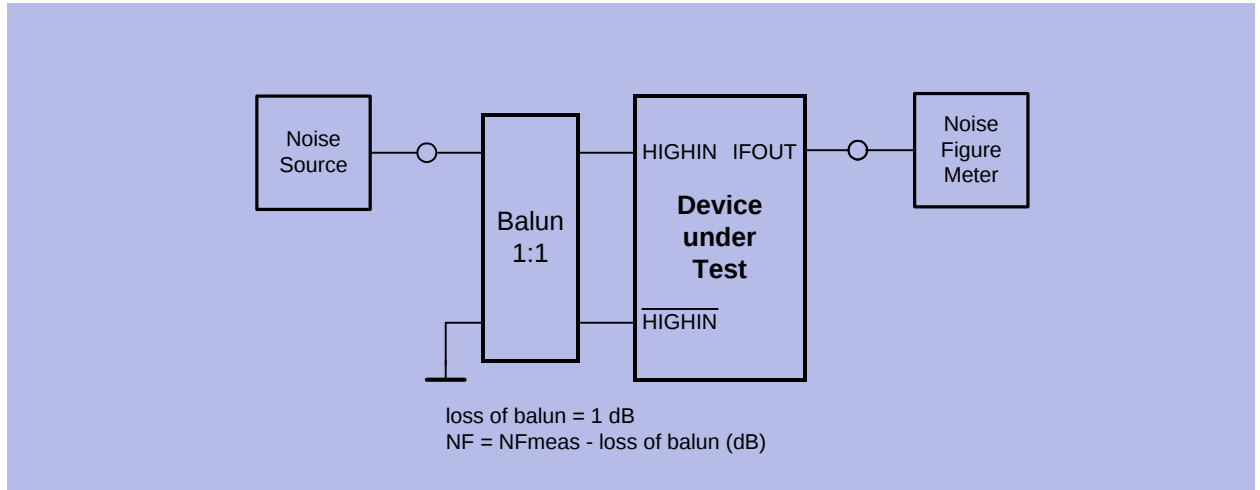
- loss = 1.3 dB
- image suppression = 13 dB

### 5.4.4 Noise Figure Test Set-up in LOW/MID



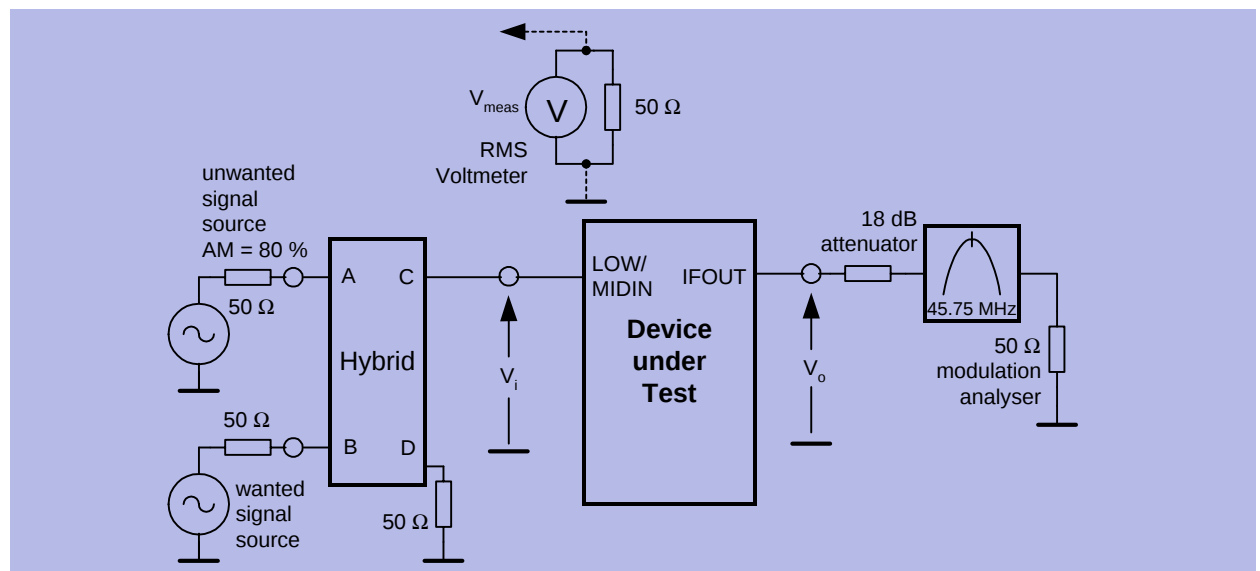
NFVHFM

### 5.4.5 Noise Figure Test Set-up in HIGH



NFUHF

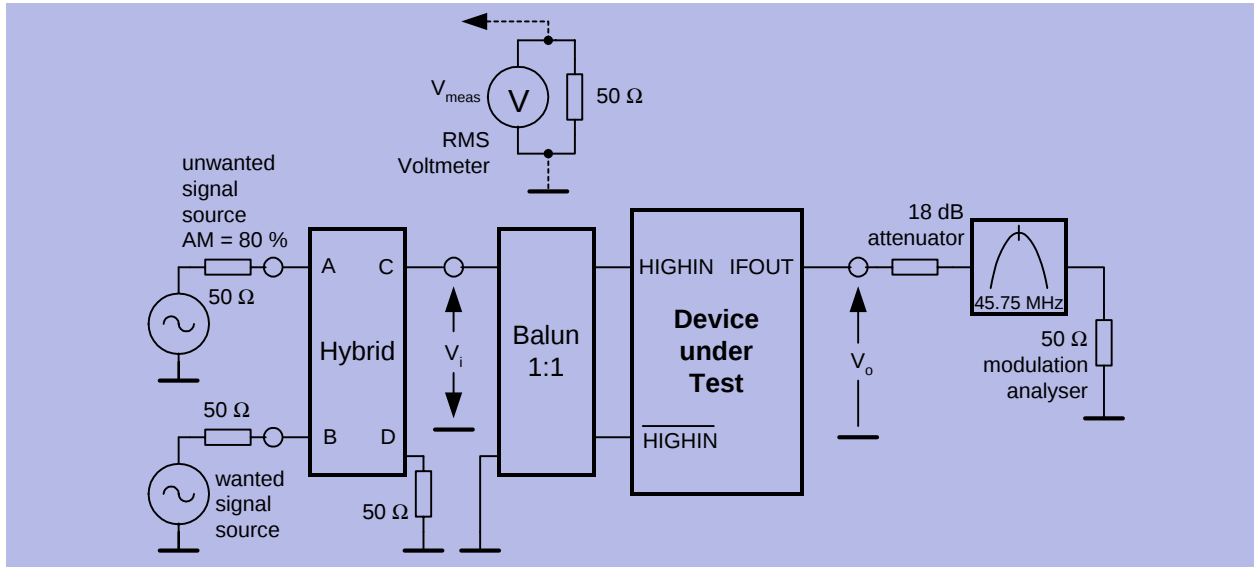
### 5.4.6 Cross modulation Test Set-up in LOW/MID band



XVHFM

- $Z_i \gg 50 \Omega \Rightarrow V_i = 2 \times V_{meas}$
- wanted output signal at  $f_{pix}$ ,  $V_o = 100 \text{ dB}\mu\text{V}$
- unwanted output signal at  $f_{snd}$ , 80 % AM modulated with 1 kHz

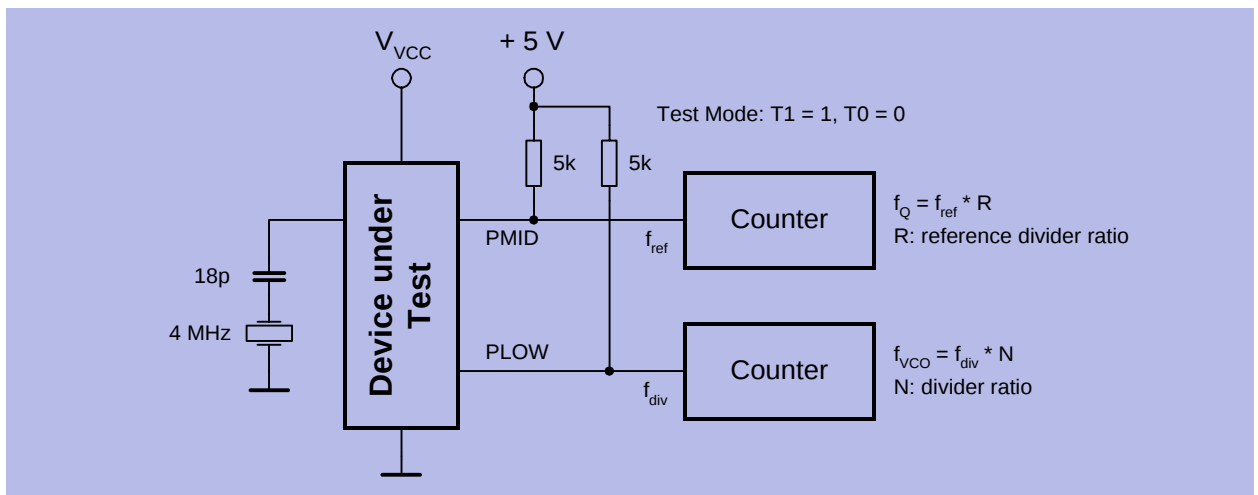
### 5.4.7 Cross modulation Test Set-up in HIGH band



XUHFM

- wanted output signal at  $f_{\text{pix}}$ ,  $V_o = 100 \text{ dB}\mu\text{V}$
- unwanted output signal at  $f_{\text{snd}}$ , 80 % AM modulated with 1 kHz

### 5.4.8 Measurement of $f_{\text{ref}}$ and $f_{\text{div}}$

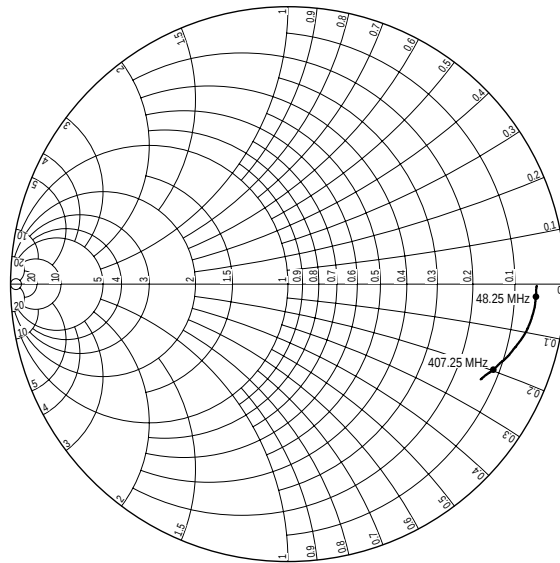


MEAS\_COF

## 5.5 Electrical Diagrams

### 5.5.1 Input admittance (S11) of the LOW/MID band mixer input

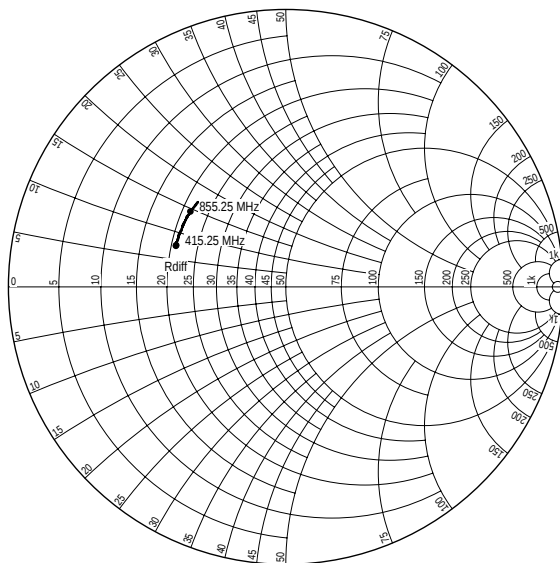
$$Y_0 = 20\text{mS}$$



Y\_VHFMIX

### 5.5.2 Input impedance (S11) of the HIGH band mixer input

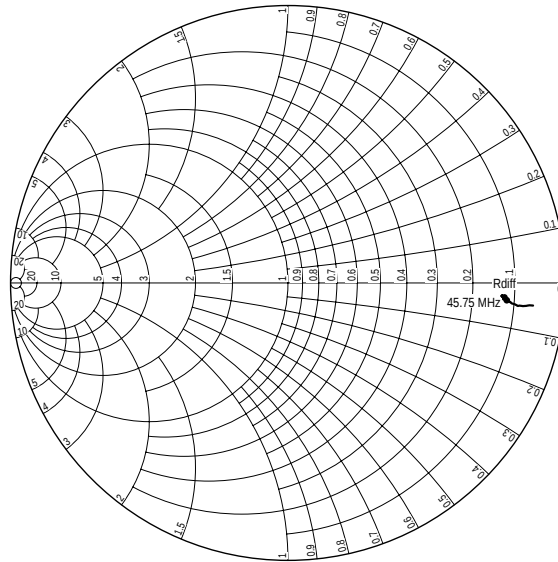
$$Z_0 = 50\ \Omega \text{ (symmetrical)}$$



Zn\_UHFMIX

### 5.5.3 Output admittance (S22) of the Mixer output

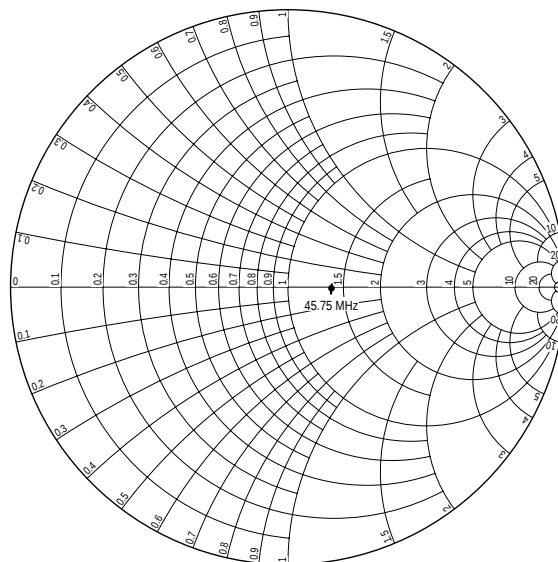
$$Y_0 = 20\text{mS}$$



Y\_MIXOUT

### 5.5.4 Output impedance (S22) of the IF output

$$Z_0 = 50\ \Omega$$



UIFOUT