

DATA SHEET

74ABT651

Octal transceiver/register, inverting
(3-State)

Product data
Supersedes data of 1995 Sep 06

2002 Dec 17

Octal transceiver/register, inverting (3-State)

74ABT651

FEATURES

- Independent registers for A and B buses
- The 74ABT651 is the inverting version of the 74ABT652
- Multiplexed real-time and stored data
- 3-State outputs
- Live insertion/extraction permitted.
- Power-up 3-State
- Power-up reset
- Output capability: +64 mA / –32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT651 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT651 transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH. Output Enable (OEAB, $\overline{\text{OEBA}}$) and Select (SAB, SBA) pins are provided for bus management.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT651.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.

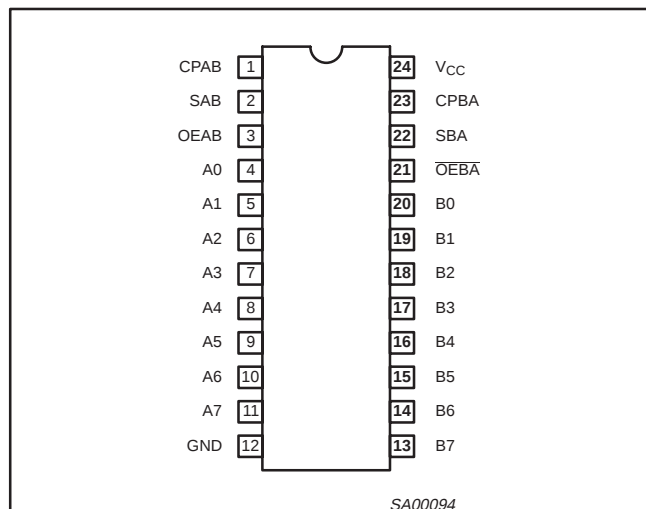
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^\circ\text{C}$; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	$C_L = 50\text{ pF}$; $V_{\text{CC}} = 5\text{ V}$	3.8 4.4	ns
C_{IN}	Input capacitance	$V_{\text{I}} = 0\text{ V}$ or V_{CC}	4	pF
$C_{\text{I/O}}$	I/O capacitance	Outputs disabled; $V_{\text{O}} = 0\text{ V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{ V}$	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
24-Pin Plastic DIP	-40°C to $+85^\circ\text{C}$	74ABT651N	SOT222-1
24-Pin plastic SO	-40°C to $+85^\circ\text{C}$	74ABT651D	SOT137-1
24-Pin Plastic TSSOP Type I	-40°C to $+85^\circ\text{C}$	74ABT651PW	SOT355-1

PIN CONFIGURATION



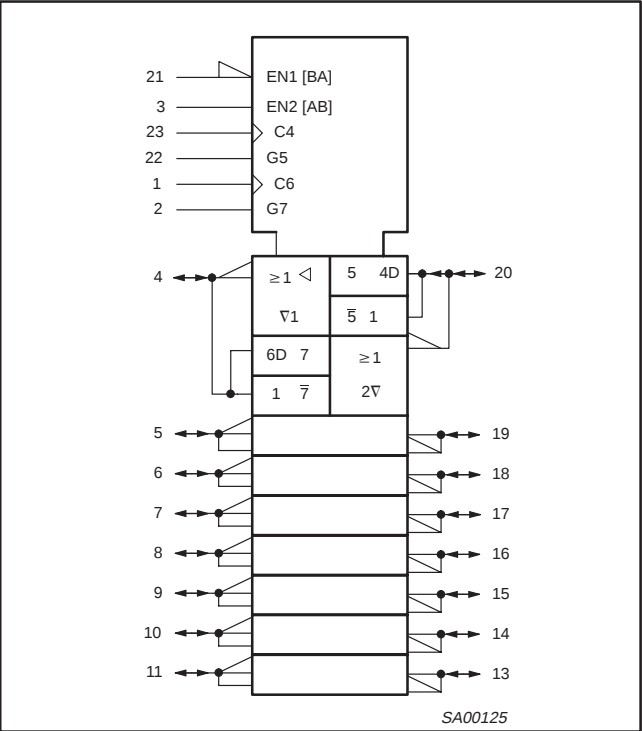
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / $\overline{\text{OEBA}}$	A to B Output Enable input / B to A Output Enable input (active-LOW)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0 V)
24	V_{CC}	Positive supply voltage

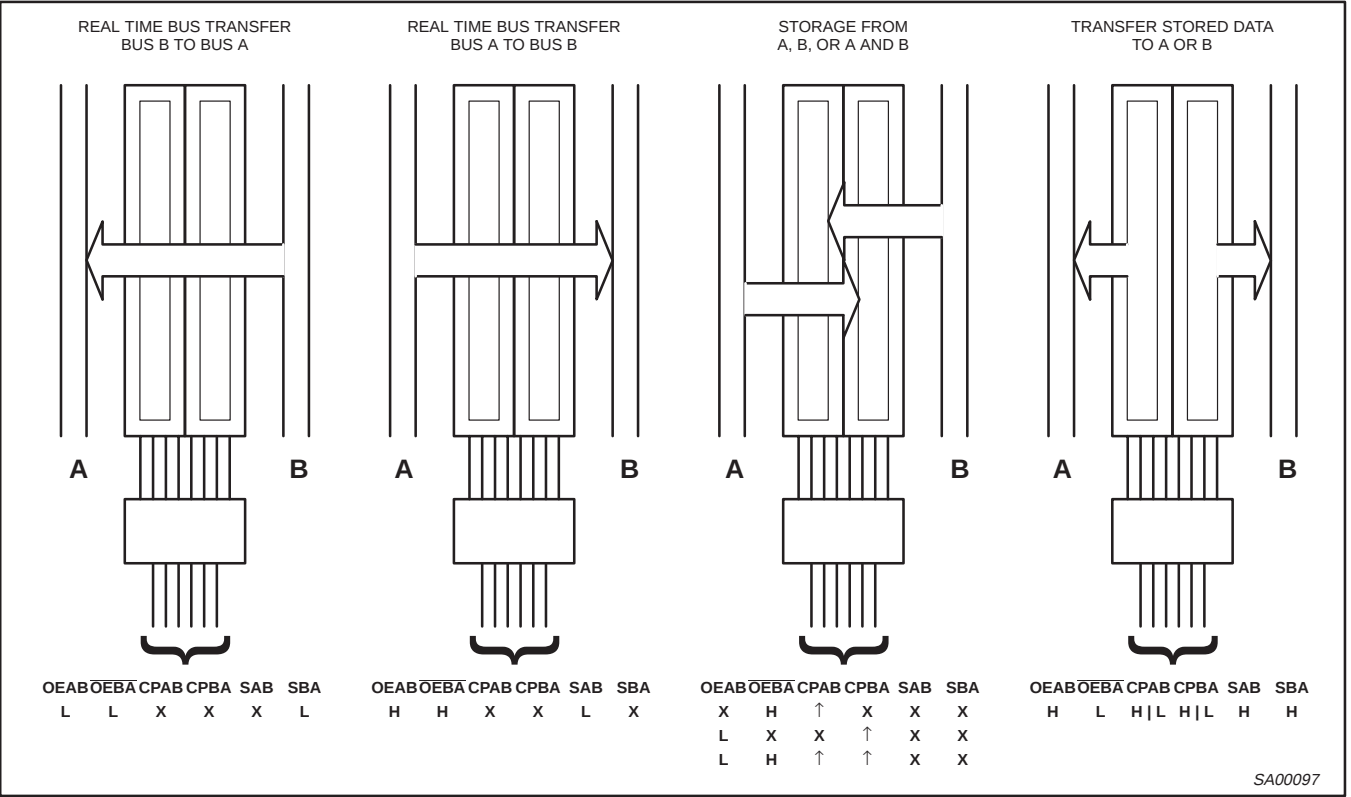
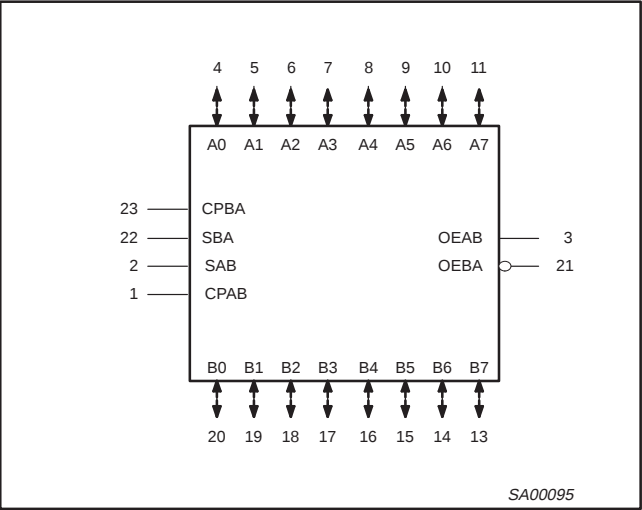
Octal transceiver/register, inverting (3-State)

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LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



Octal transceiver/register, inverting (3-State)

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FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	OEBA	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time $\bar{B}$ data to A bus Stored $\bar{B}$ data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time $\bar{A}$ data to B bus Store $\bar{A}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\bar{A}$ data to B bus Stored $\bar{B}$ data to A bus

H = HIGH voltage level

L = LOW voltage level

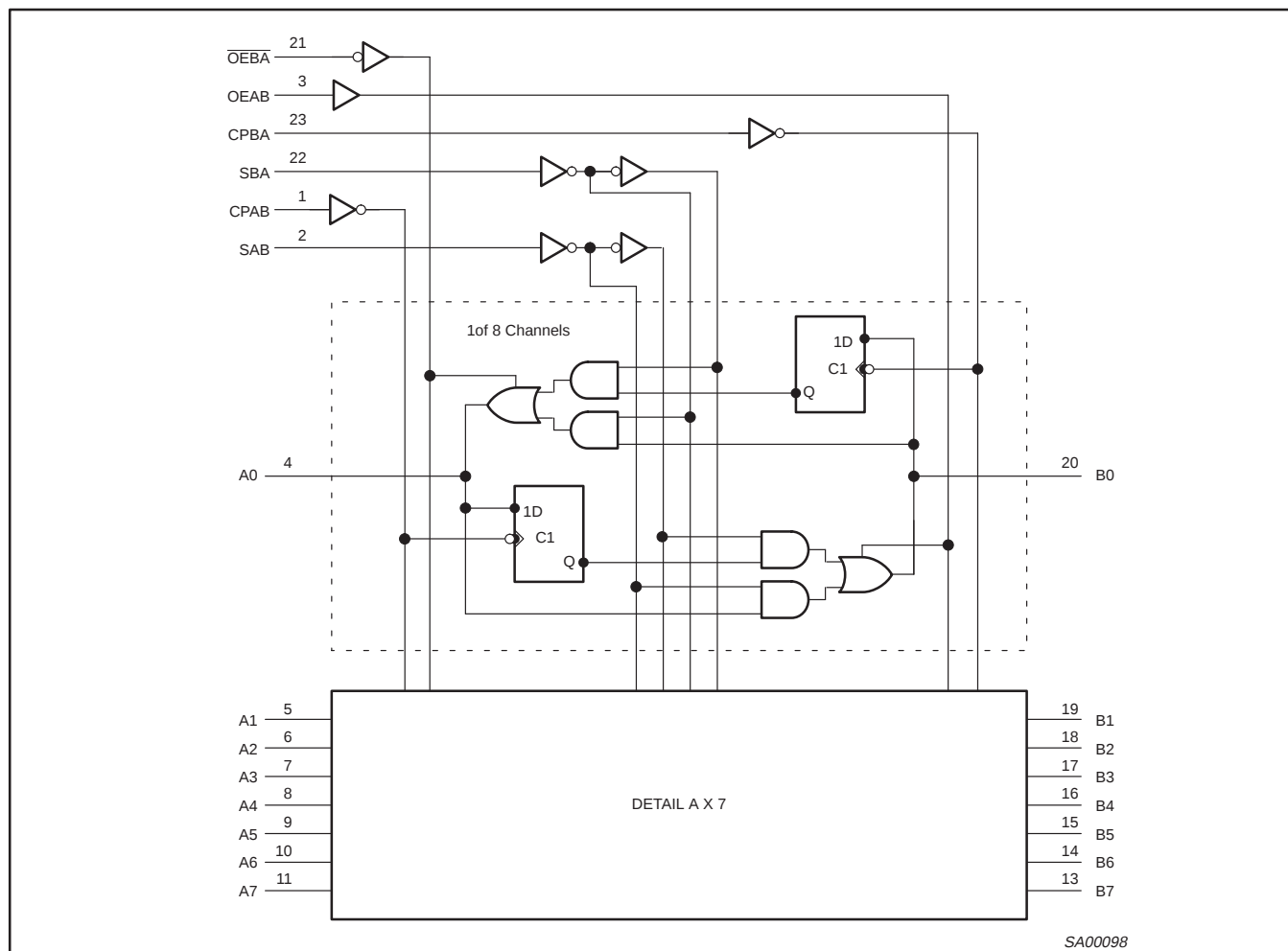
X = Don't care

↑ = LOW-to-HIGH clock transition

* The data output function may be enabled or disabled by various signals at the $\overline{\text{OEBA}}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

** If both Select controls (SAB and SBA) are LOW, then clocks can occur simultaneously. If either Select control is HIGH, the clocks must be staggered in order to load both registers.

LOGIC DIAGRAM



Octal transceiver/register, inverting (3-State)

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	−18	mA
V_I	DC input voltage ³		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	−50	mA
V_{OUT}	DC output voltage ³	output in Off or HIGH state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0		V
V_{IL}	LOW-level input voltage		0.8	V
I_{OH}	HIGH-level output current		−32	mA
I_{OL}	LOW-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T _{amb} = +25 °C			T _{amb} = -40 °C to +85 °C		
				Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage		V _{CC} = 4.5 V; I _{IK} = -18 mA		-0.9	-1.2		-1.2	V
V _{OH}	HIGH-level output voltage		V _{CC} = 4.5 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	2.5	3.2		2.5		V
			V _{CC} = 5.0 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	3.0	3.7		3.0		V
			V _{CC} = 4.5 V; I _{OH} = -32 mA; V _I = V _{IL} or V _{IH}	2.0	2.30		2.0		V
V _{OL}	LOW-level output voltage		V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST} ³	Power-up output low voltage		V _{CC} = 5.5 V; I _O = 1 mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	Control pins	V _{CC} = 5.5 V; V _I = GND or 5.5 V		±0.01	±1.0		±1.0	µA
		Data pins	V _{CC} = 5.5 V; V _I = GND or 5.5 V		±5	±100		±100	µA
I _{OFF}	Power-off leakage current		V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V		±5.0	±100		±100	µA
I _{PU} /I _{PD}	Power-up/down 3-State output current ⁴		V _{CC} = 2.1 V; V _O = 0.5 V; V _O $\overline{\text{OE}}$ = Don't Care; V _I = GND or V _{CC}		±5.0	±50		±50	µA
I _{IH} + I _{OZH}	3-State output HIGH current		V _{CC} = 5.5 V; V _O = 2.7 V; V _I = V _{IL} or V _{IH}		5.0	50		50	µA
I _{IL} + I _{OZL}	3-State output LOW current		V _{CC} = 5.5 V; V _O = 0.5 V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	µA
I _{CEX}	Output High leakage current		V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}		5.0	50		50	µA
I _O	Output current ¹		V _{CC} = 5.5 V; V _O = 2.5 V	-40	-65	-180	-40	-180	mA
I _{CCH}	Quiescent supply current		V _{CC} = 5.5 V; Outputs High, V _I = GND or V _{CC}		110	250		250	µA
I _{CCL}				20	30		30	mA	
I _{CCZ}				110	250		250	µA	
ΔI _{CC}	Additional supply current per input pin ²		V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10%, a transition time of up to 100 µsec is permitted.

AC CHARACTERISTICS

GND = 0 V; t_R = t_F = 2.5 ns; C_L = 50 pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V			T _{amb} = −40 °C to +85 °C V _{CC} = +5.0 V ±0.5 V		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	125	300		125		MHz
t _{PLH} t _{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.2 1.7	3.8 4.4	5.1 5.1	2.2 1.7	5.6 5.6	ns
t _{PLH} t _{PHL}	Propagation delay An to Bn or Bn to An	2	1.5 1.5	3.2 3.7	5.1 4.6	1.5 1.5	6.2 5.4	ns
t _{PLH} t _{PHL}	Propagation delay SAB to Bn or SBA to An	3	1.5 1.5	3.8 4.4	5.1 4.9	1.5 1.5	6.5 5.9	ns
t _{PZH} t _{PZL}	Output enable time OEBA to An	5 6	1.3 2.5	3.7 4.7	4.6 6.8	1.3 2.5	5.8 8.5	ns
t _{PHZ} t _{PLZ}	Output disable time OEBA to An	5 6	1.5 1.5	4.0 3.2	4.5 3.8	1.5 1.5	5.0 4.1	ns
t _{PZH} t _{PZL}	Output enable time OEAB to Bn	5 6	1.8 2.9	3.4 4.5	6.1 6.5	1.8 2.9	6.5 7.4	ns
t _{PHZ} t _{PLZ}	Output disable time OEAB to Bn	5 6	1.5 1.5	3.8 3.1	4.5 4.4	1.5 1.5	5.5 5.1	ns

Octal transceiver/register, inverting (3-State)

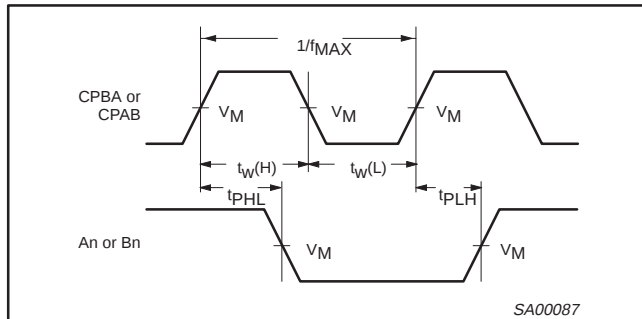
74ABT651

AC SET-UP REQUIREMENTS

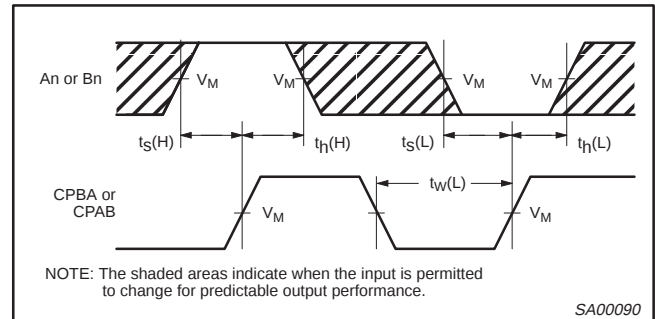
GND = 0 V; $t_R = t_F = 2.5$ ns; $C_L = 50$ pF, $R_L = 500$ Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25$ °C $V_{CC} = +5.0$ V		$T_{amb} = -40$ °C to $+85$ °C $V_{CC} = +5.0$ V ± 0.5 V	
			Min	Typ	Min	
$t_S(H)$ $t_S(L)$	Set-up time An to CPAB, Bn to CPBA	4	3.0 3.0	1.2 0.8	3.0 3.0	ns
$t_H(H)$ $t_H(L)$	Hold time An to CPAB, Bn to CPBA	4	0.0 0.0	-0.8 -0.9	0.0 0.0	ns
$t_W(H)$ $t_W(L)$	Pulse width, HIGH or LOW CPAB or CPBA	1	4.0 4.0	1.2 1.1	4.0 4.0	ns

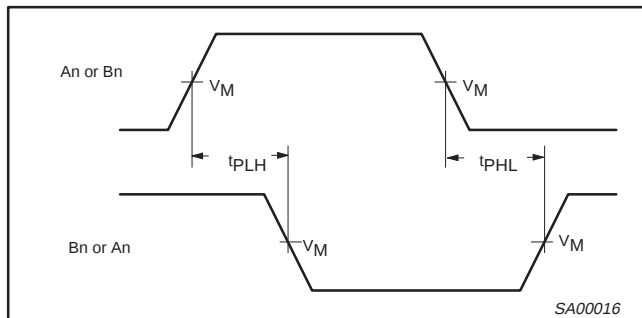
AC WAVEFORMS

 $V_M = 1.5$ V; $V_{IN} =$ GND to 3.0 V

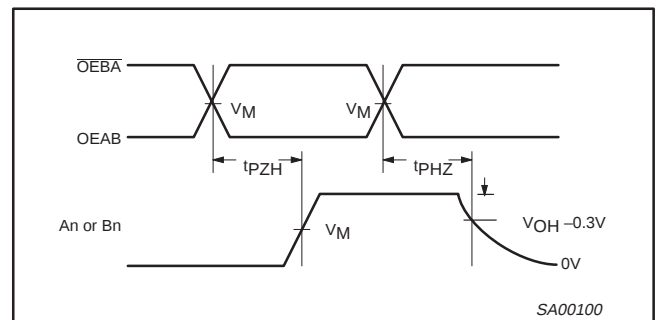
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



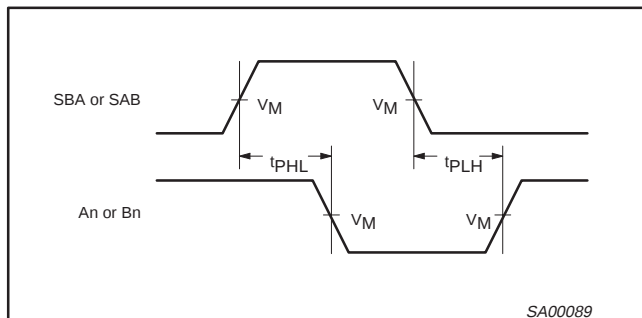
Waveform 4. Data Set-up and Hold Times



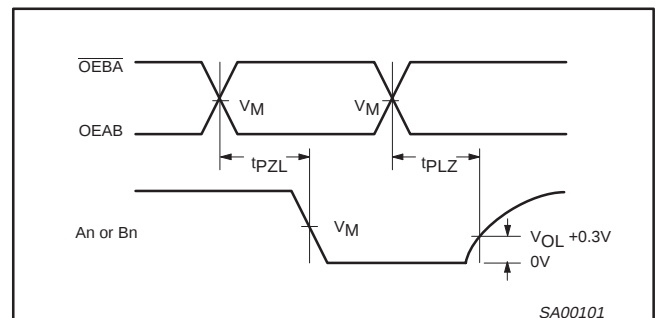
Waveform 2. Propagation Delay, An to Bn or Bn to An



Waveform 5. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level



Waveform 3. Propagation Delay, SBA to An or SAB to Bn

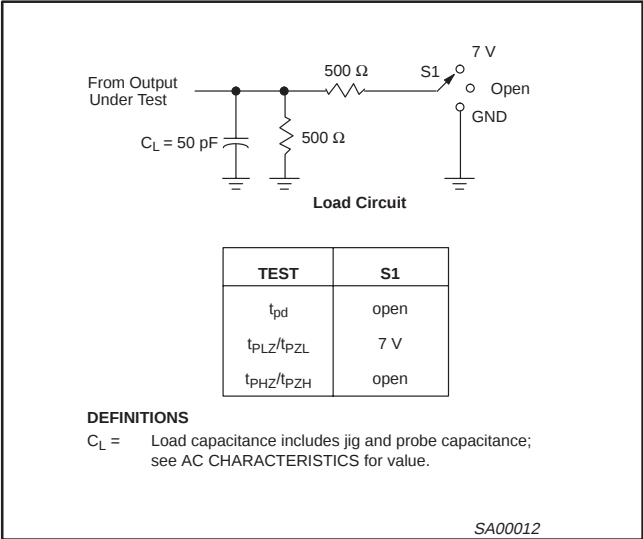


Waveform 6. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

Octal transceiver/register, inverting (3-State)

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TEST CIRCUIT AND WAVEFORM



Octal transceiver/register, inverting (3-State)

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1

Technical drawing of the 74ABT651 DIP24 package. The drawing includes three views: a top view showing the 24 pins and dimensions A, A1, A2, b, b1, c, D, E, e, e1, L, ME, MH, w, Z; a side view showing the package height and dimensions A, A1, A2, b1, c, ME, MH; and an end view showing the package width and dimensions b, E. A scale bar indicates 0, 5, and 10 mm. A note states: '1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.'

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

OUTLINE
VERSION

SOT222-1

REFERENCES

IEC

JEDEC

EIAJ

MS-001

EUROPEAN
PROJECTION

ISSUE DATE

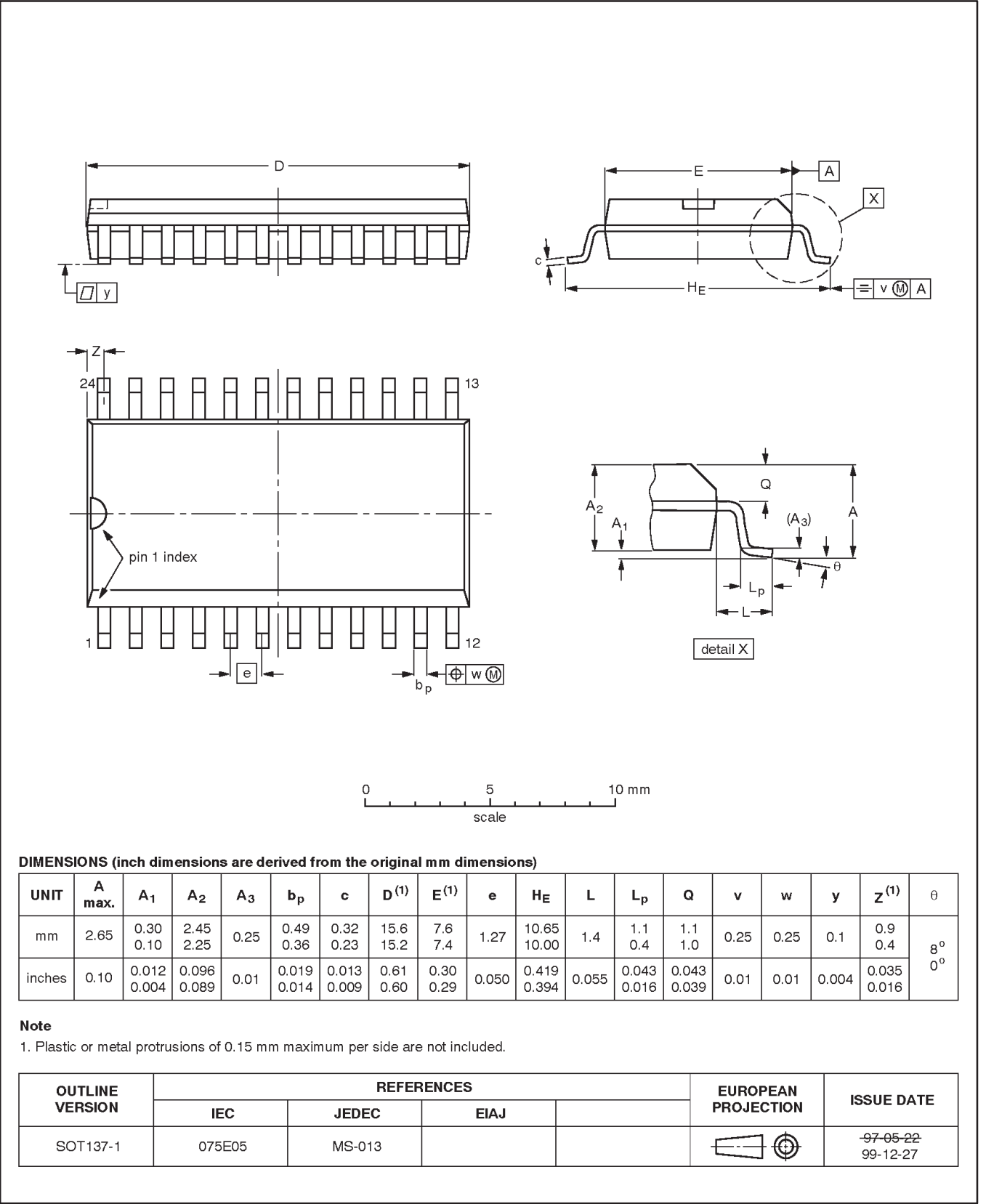
99-04-28
99-12-27

Octal transceiver/register, inverting (3-State)

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

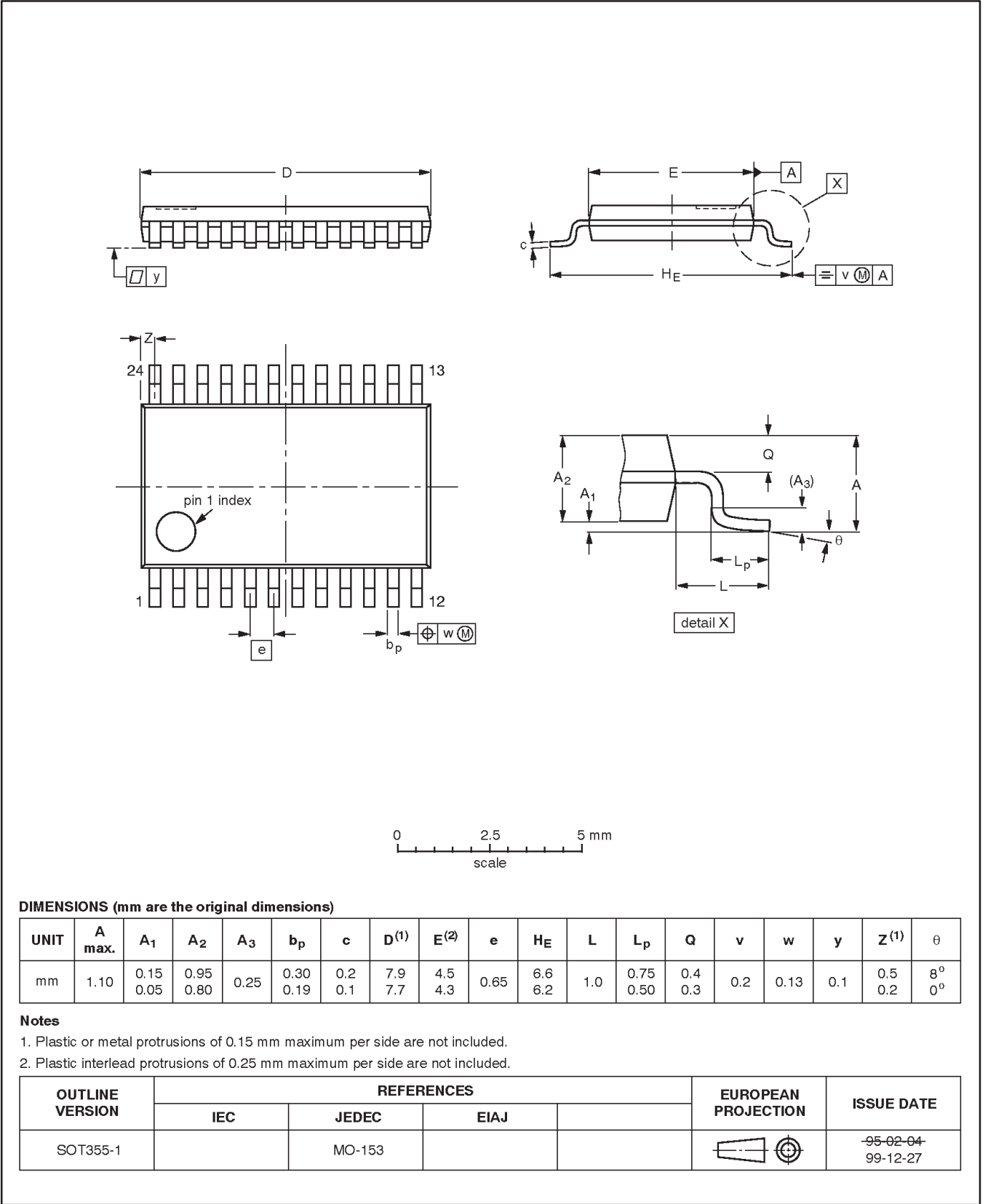


Octal transceiver/register, inverting (3-State)

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



Octal transceiver/register, inverting (3-State)

74ABT651

REVISION HISTORY

Rev	Date	Description
_2	20021216	Product data (9397 750 10849); ECN 853-1783 29290 of 12 December 2002. Supersedes data of 06 September 1995. Modifications: • Ordering information table: remove "North America" column; remove 74ABT651DB package offering.
_1	19950906	Product specification. ECN 853-1783 15703 of 06 September 1995.

Octal transceiver/register, inverting (3-State)

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Let's make things better.