SN74ALVCHG162280
16-BIT TO 32-BIT REGISTERED BUS EXCHANGER
WITH BYTE MASKS AND 3-STATE OUTPUTS

FEATURES

- **Member of the Texas Instruments Widebus™ Family**

- **EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**

- **A-Port Outputs Have Equivalent 50-Ω Series Resistors and B-Port Outputs Have Equivalent 20-Ω Series Resistors, So No External Resistors Are Required**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

- **Packaged in Thin Very Small-Outline Package**

NOTE: For order entry, the DBB package is abbreviated to G. For tape and reel, the DBBR package is abbreviated to GR.

DESCRIPTION

The SN74ALVCHG162280 is a 16-bit to 32-bit registered bus exchanger. This device is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V) V_{CC} operation.

The device provides synchronous data exchange between the two ports, A and B. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select ($\overline{SEL}$) input selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output-enable ($\overline{OE}$) and direction-control (DIR) inputs. DIR is registered to synchronize the bus direction changes with the clock.

Two mask bits are provided for both data bytes. The data (D) outputs are controlled by $\overline{OE}$.

DBB PACKAGE
(TOP VIEW)

V_{CC}	1	80	V_{CC}
GND	2	79	GND
2B7	3	78	1B8
1B7	4	77	2B8
2B6	5	76	1B9
GND	6	75	GND
1B6	7	74	2B9
2B5	8	73	1B10
1B5	9	72	2B10
V_{CC}	10	71	V_{CC}
2B4	11	70	1B11
1B4	12	69	2B11
2B3	13	68	1B12
1B3	14	67	2B12
GND	15	66	GND
2B2	16	65	1B13
1B2	17	64	2B13
2B1	18	63	1B14
1B1	19	62	2B14
V_{CC}	20	61	V_{CC}
GND	21	60	GND
2D2	22	59	1B15
1D2	23	58	2B15
2D1	24	57	1B16
1D1	25	56	2B16
V_{CC}	26	55	V_{CC}
C1	27	54	A16
C2	28	53	A15
A1	29	52	A14
GND	30	51	GND
A2	31	50	A13
A3	32	49	A12
A4	33	48	A11
V_{CC}	34	47	V_{CC}
A5	35	46	A10
A6	36	45	A9
A7	37	44	A8
GND	38	43	GND
CLK	39	42	$\overline{OE}$
$\overline{SEL}$	40	41	DIR

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DESCRIPTION (CONTINUED)

The A-port N-channel output transistors are sized at 450 μm, and the P-channel output transistors are sized at 700 μm. All A-port outputs have equivalent 50-Ω series resistors. The B-port N-channel output transistors are sized at 225 μm, and the P-channel output transistors are sized at 560 μm. All B-port outputs have equivalent 20-Ω series resistors.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The switching characteristics are based on 25-pF (A port) and 80-pF (B and D ports) loads, but are tested with the standard 50-pF load.

The SN74ALVCHG162280 is characterized for operation from 0$°$C to 70$°$C.

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FUNCTION TABLES

A-TO-B STORAGE
($\overline{OE}$ = L, DIR = H)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	A	1B	2B
H	X	X	$1B_0$[1]	$2B_0$[1]
L	$\uparrow$	L	L[2]	L
L	$\uparrow$	H	H[2]	H

(1) Output level before indicated steady-state input conditions were established
(2) Two CLK edges are needed to propagate the data.

B-TO-A STORAGE
($\overline{OE}$ = L, DIR = L)

INPUTS				OUTPUT A
CLK	$\overline{SEL}$	1B	2B	
$\uparrow$	H	X	L	L[1]
$\uparrow$	H	X	H	H[1]
$\uparrow$	L	L	X	L
$\uparrow$	L	H	X	H

(1) Two CLK edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is low and propagates to the second register when $\overline{SEL}$ is high.

C-TO-D STORAGE
($\overline{OE}$ = L)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	C	1D	2D
H	X	X	$1D_0$[1]	$2D_0$[1]
L	$\uparrow$	L	L[2]	L
L	$\uparrow$	H	H[2]	H

(1) Output level before indicated steady-state input conditions were established
(2) Two CLK edges are needed to propagate the data.

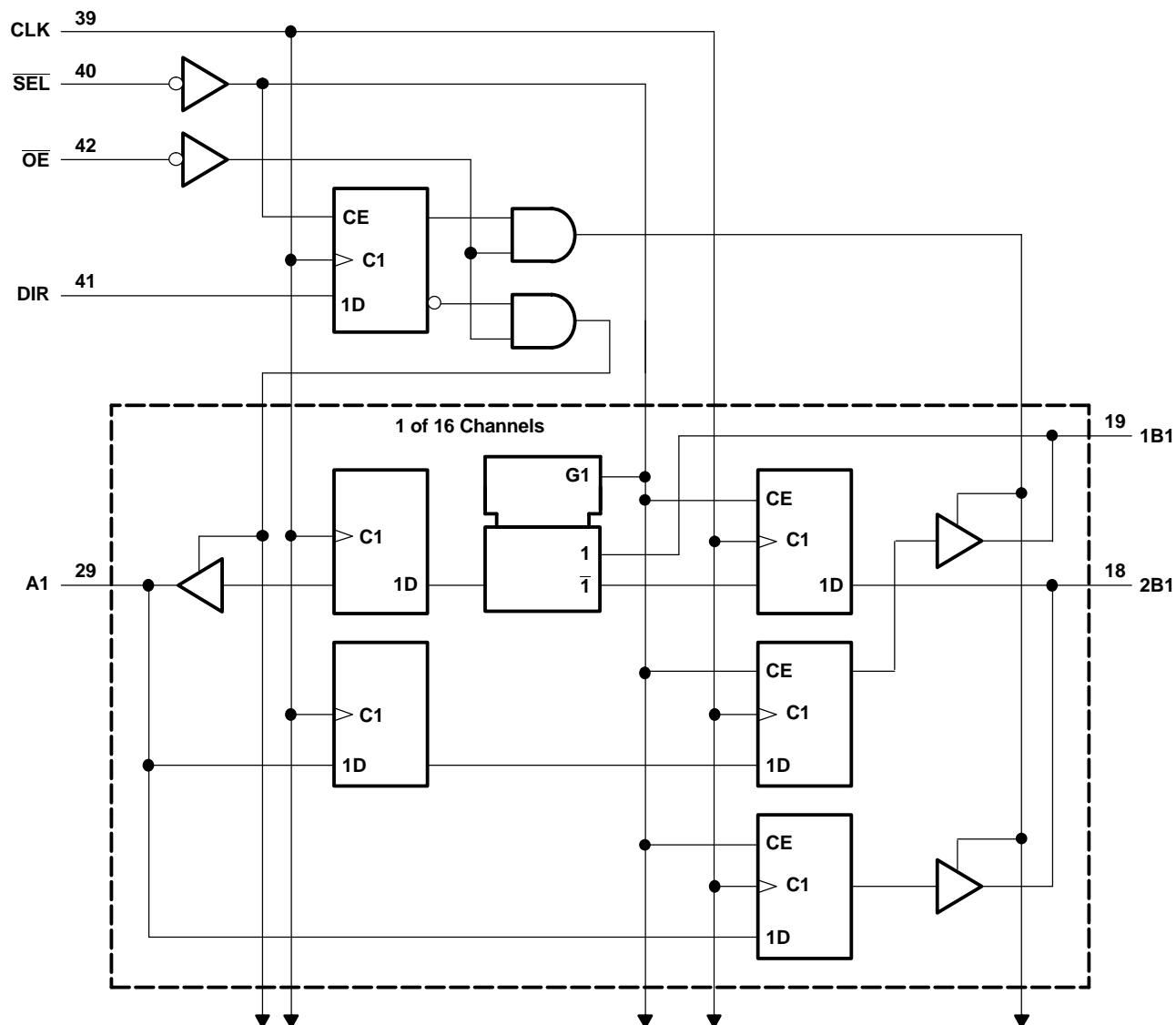### OUTPUT ENABLE

INPUTS			OUTPUTS		
CLK	$\overline{OE}$	DIR	A	1B, 2B	1D, 2D
$\uparrow$	H	X	Z	Z	Z
$\uparrow$	L	H	Z	Active	Active
$\uparrow$	L	L	Active	Z	Active

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LOGIC DIAGRAM, A AND B PORTS (POSITIVE LOGIC)

LOGIC DIAGRAM, C AND D PORTS (POSITIVE LOGIC)
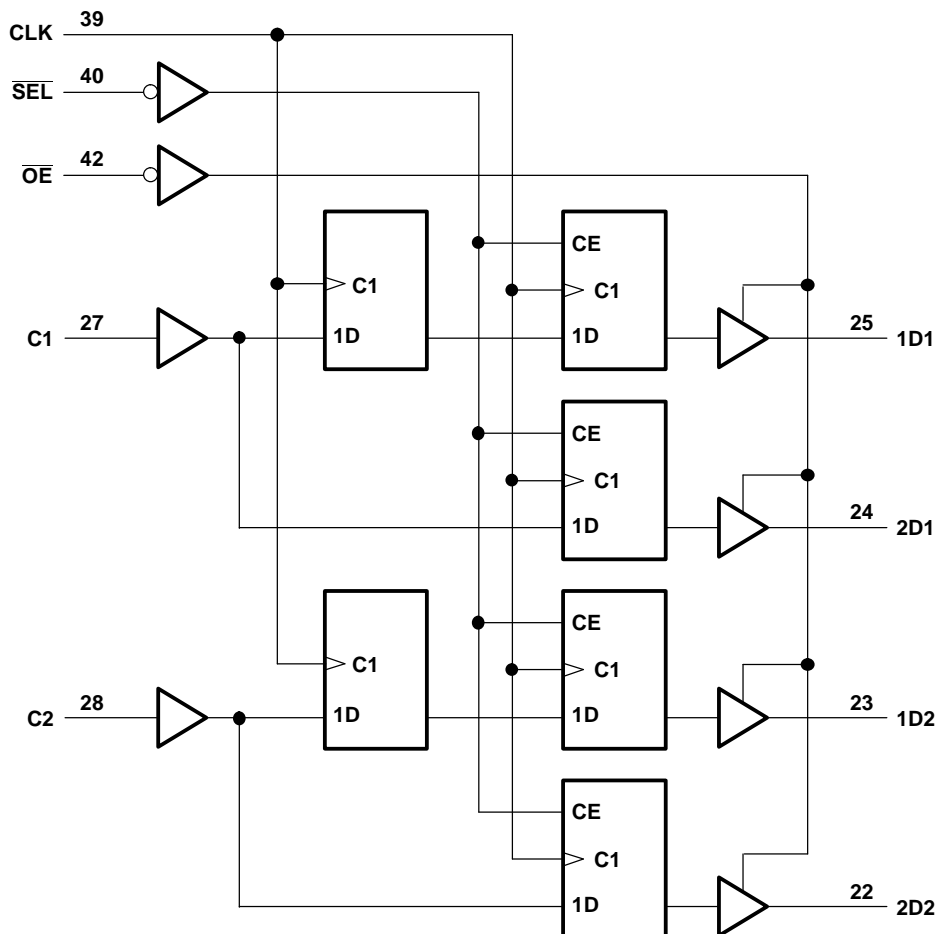
ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range	Except I/O ports[2]	-0.5	V_{CC} + 0.5	V
		I/O ports[2][3]	-0.5	V_{CC} + 0.5	
V_O	Output voltage range[2][3]		-0.5	V_{CC} + 0.5	V
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
θ_{JA}	Package thermal impedance[4]			106	°C/W
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51.

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RECOMMENDED OPERATING CONDITIONS[(1)]

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	3.6	V
V_{IH}	High-level input voltage		V_{CC} = 3 V to 3.6 V	2		V
V_{IL}	Low-level input voltage		V_{CC} = 3 V to 3.6 V		0.8	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	A to B	V_{CC} = 3 V		8	mA
		B to A	V_{CC} = 3 V		6	
I_{OL}	Low-level output current	A to B	V_{CC} = 3 V		8	mA
		B to A	V_{CC} = 3 V		6	
$\Delta t/\Delta v$	Input transition rise or fall rate				10	ns/V
T_A	Operating free-air temperature			0	70	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[(1)]	MAX	UNIT
V_{OH}		I_{OH} = -100 µA		3 V to 3.6 V	V_{CC} - 0.2			V
	A to B	I_{OH} = -8 mA		3 V	2			
	B to A	I_{OH} = -6 mA		3 V	2			
V_{OL}		I_{OL} = 100 µA		3 V to 3.6 V			0.2	V
	A to B	I_{OL} = 8 mA		3 V			0.8	
	B to A	I_{OL} = 6 mA		3 V			0.8	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.8 V		3 V	75			µA
		V_I = 2 V		3 V	-75			
		V_I = 0 to 3.6 V [(2)]		3.6 V			±500	
I_{OZ}[(3)]		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} - 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		4		pF
	C port					8.5		
C_o	D port	V_O = V_{CC} or GND		3.3 V		7		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		8.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

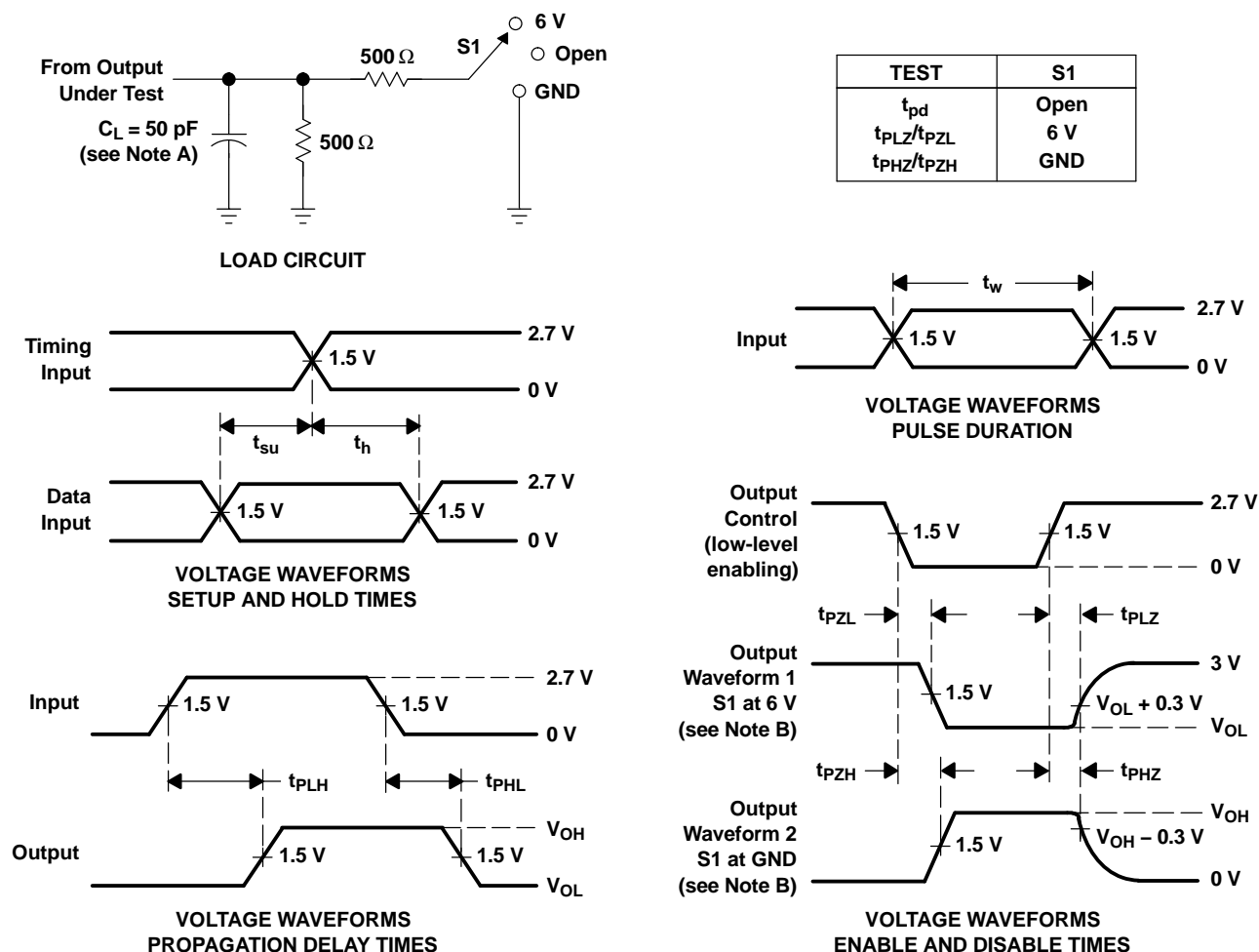over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 3.3 V $\pm$ 0.3 V		UNIT
			MIN	MAX	
f_{clock}	Clock frequency			160	MHz
t_w	Pulse duration, CLK high or low		2.3		ns
t_{su}	Setup time, high or low	A data before CLK↑	1.4		ns
		B data before CLK↑	2		
		C data before CLK↑	1.3		
		DIR before CLK↑	2		
		$\overline{SEL}$ before CLK↑	2		
t_h	Hold time, high or low	A data after CLK↑	0.3		ns
		B data after CLK↑	0.3		
		C data after CLK↑	0.3		
		DIR after CLK↑	0.3		
		$\overline{SEL}$ after CLK↑	0.3		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 25 pF (A port), 80 pF (B and D ports) (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V $\pm$ 0.3 V		UNIT
			MIN	MAX	
f_{max}			160		MHz
t_{pd}	CLK	A	1.5	5	ns
		B	1.5	7.4	
		D	1.5	7.2	
t_{en}	CLK	A	1.5	6.2	ns
		B	1.5	9.4	
	$\overline{OE}$	A	1.5	6	
		B	1.5	9.5	
		D	1.5	7.9	
t_{dis}	CLK	A	1.5	6.4	ns
		B	1.5	7.8	
	$\overline{OE}$	A	1.5	5	
		B	1.5	7.6	
		D	1.5	6.7	

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r ≤ 2.5$ ns, $t_f ≤ 2.5$ ns.
D. The output is measured with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
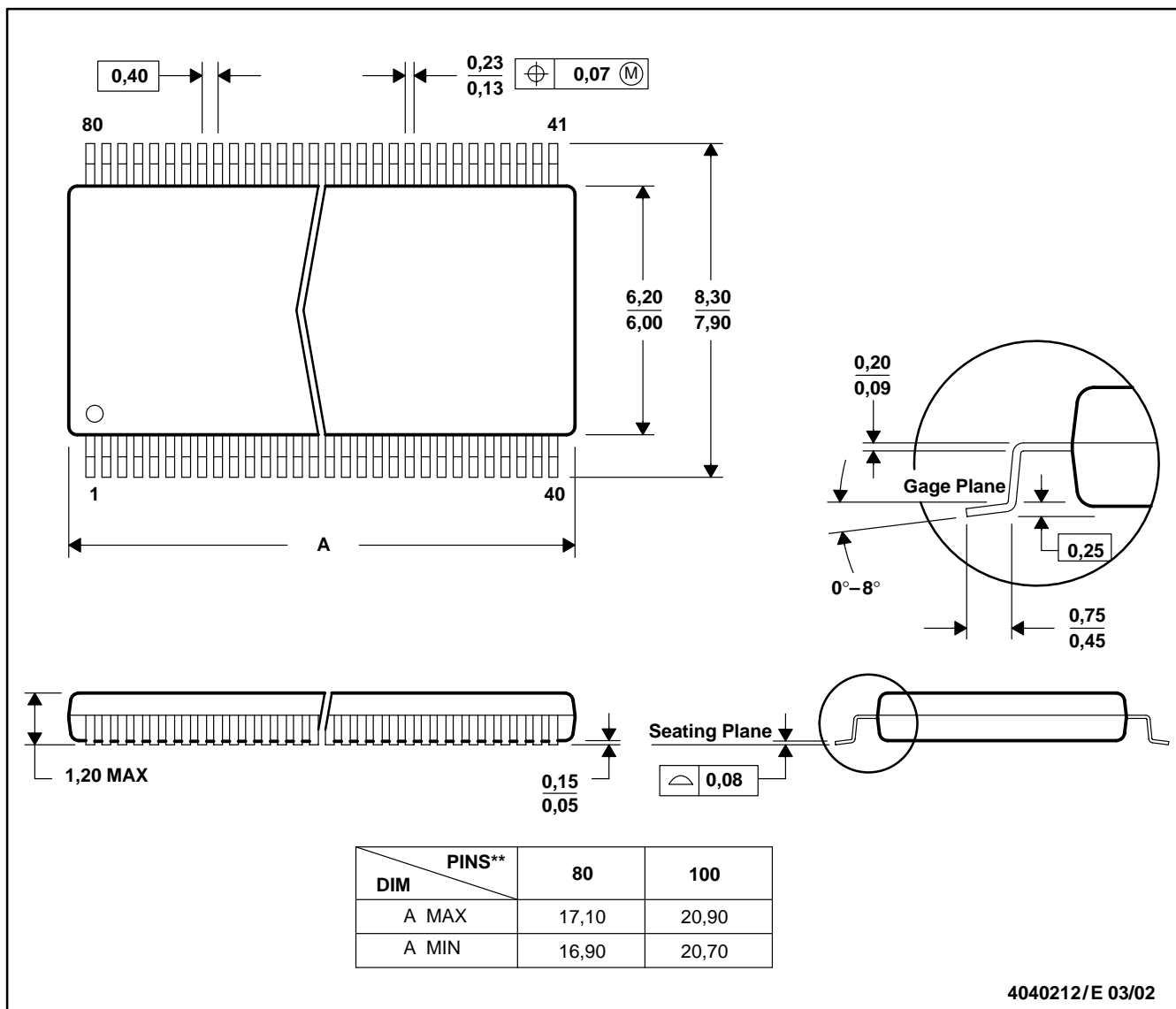G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

DBB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

80 PINS SHOWN

PINS** DIM	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC :   80 Pin – MO-153 Variation FF
100 Pin – MO-194 Variation BB

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