DS2488

1-Wire Dual-Port Link

General Description

The DS2488 is a simple bridge device that with a single dedicated contact on each side of the bridge enables up to 512kbps pass-through communication, power delivery for battery charging, small message exchange, and state reporting between two microcontroller-based subsystems. An example application is true wireless stereo (TWS) earbuds containing a Bluetooth® Audio SoC and the microcontroller operated case that holds and charges the earbuds. In this scenario, the DS2488 would reside in earbuds alongside the SoC, and the charge case microcontroller would communicate with the DS2488 from a single dedicated pin. All of this is enabled with the flexibility of the 1-Wire® interface, which is used to operate each of the two independent I/O ports, IOA and IOB. To enable device operation between two connected controllers, each of these two DS2488 1-Wire interfaces has access to a 64-bit factory-programmed ROM ID, an 8-byte buffer to transmit small messages, and registers for device configuration, status, and control of three open-drain GPIO pins. Through a configuration setting a bidirectional, high-speed 512kbps pass-through mode is enabled, which enables large data transfers between the two connected microcontrollers.

For communication between IOA and IOB, the DS2488 has a maximum operating voltage of 3.63V. But to support a special mode of power delivery from the subsystem connected to the IOA side to the subsystem connected to the IOB side, the device is 5V tolerant and goes into the power delivery state when 4V to 5V (nom) is applied to IOA. In this mode, an additional DS2488 output pin is used to control an external transistor for power delivery to IOB-side electronics, such as a battery charger.

Applications

- True Wireless Stereo Earbuds and Charger Box
- Communication and Control Bridging
- Wearable Devices
- Electronic Locks

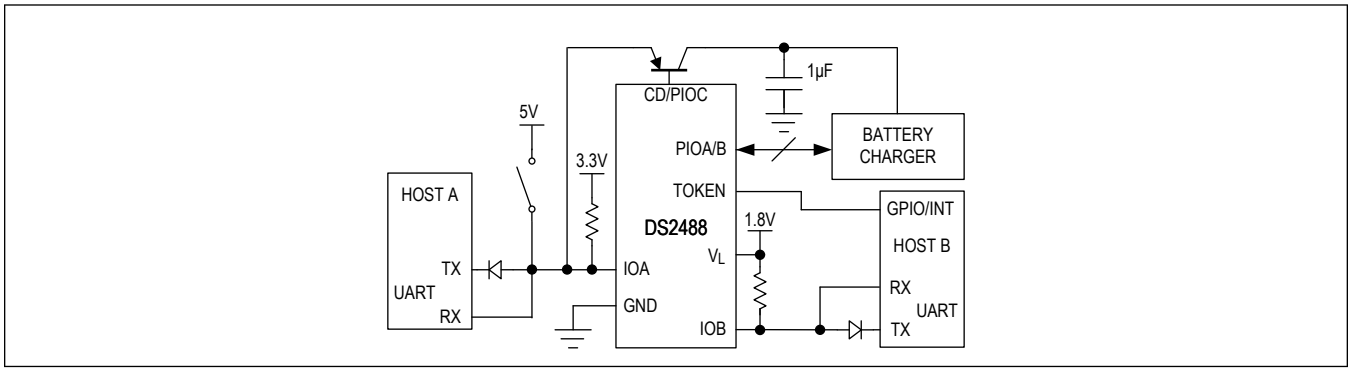
Benefits and Features

- Two-Contact Solution Enables Advance TWS Features
  - Small Message Exchange between a Case and Earbuds
  - High-Speed 512kbps Pass-Through Mode to Transfer Files
  - Earbud Battery Charger Power Delivery
  - Three GPIO Pins for Optional Feature Control or State Detection
- Full Range of Capabilities for Earbud and Charging Case Detection
  - Earbud 64-Bit Identification Number (ROM ID) Readable upon Insertion
  - Operating Power Parasitically Derived from the 1-Wire IOA Line
  - Detect when in or out of a Charging Case
  - Detect a Dead Charging Case Battery
- Minimalist Dual 1-Wire Interface Reduces Cost and Complexity
  - Single Dedicated Contact for Communication and Power
  - Arbitrated Communication between Two Host Controllers at 90kbps
  - Reads and Writes over a Wide, 1.71V to 3.63V Voltage Range
- Ideal for Battery Power Consumer Applications
  - Small, 1.6mm x 0.9mm x 0.33mm WLP with 0.4mm Ball Pitch
  - 1.71V to 3.63V Operating Voltage Range
  - High ESD Immunity of IOA Pin: ±8kV HBM (typ)
  - -40°C to +85°C Operation

***Ordering Information** appears at end of data sheet.*

19-100871; Rev 3; 9/22

Simplified Application Block Diagram



Absolute Maximum Ratings

Any Pin to GND ..... -0.3V to +5.5V
Maximum Current into Any Pin..... -20mA to 20mA
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 11.4mW/°C above +70°C)..... 627mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature ..... +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 WLP

Package Code	Z80D1+1
Outline Number	21-100497
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	87.71C°/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Voltage Low	V_L	IOB power rail when present		1.71		3.63	V
Supply Current for Voltage Low	I_{VL}				6	60	µA
IOA, IOB PINS: GENERAL DATA							
1-Wire Pullup Voltage A	V_{PUPA}	IOA pin only	(*Note 1*)	1.71	3.3	3.63	V
1-Wire Pullup Resistance A	R_{PUPA}	IOA pin only	(*Note 2*)	300		1000	Ω
1-Wire Pullup Resistance B	R_{PUPB}	IOB pin only	(*Note 2*)	300		10000	Ω
Supply Capacitance	C_{SUPPLY}	IOA or V_L first powered (*Note 3*)			2		nF
Input Capacitance A	C_{IOA}	IOA pin only	(*Note 3*)		2		nF
Input Capacitance B	C_{IOB}	IOB pin only			15		pF
Input Load Current A	I_{L_IOA}	(*Note 4*)			10	100	uA
Input Load Current B	I_{L_IOB}			-1		1	µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Comparator Threshold	V_{CMP}	IOA operation only. After POR or SEL = 0.		3.7	4	4.3	V
High-Voltage Detection Maximum Ramp	t_{HVR}	IOA; V_{TH} to V_{CMP} with V_L = 1.8V and DIV1			298		µs
		IOA; V_{TH} to V_{CMP} with V_L = 1.8V and DIV2			646		
		IOA; V_{TH} to V_{CMP} with V_L = 1.8V and DIV4			1330		
		IOA; V_{TH} to V_{CMP} with V_L = 1.8V and DIV8			2610		
High-to-Low Switching Threshold	V_{TL}	IOA; V_{PUP} = V_{PUPA}, IOB; V_{PUP} = V_L (*Note 5*, *Note 6*)			0.65 x V_{PUP}		V
Input Low Voltage	V_{IL}	IOA; V_{PUP} = V_{PUPA}, IOB; V_{PUP} = V_L (*Note 7*)				0.1 x V_{PUP}	V
Low-to-High Switching Threshold	V_{TH}	IOA; V_{PUP} = V_{PUPA}, IOB; V_{PUP} = V_L (*Note 5*, *Note 8*)			0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	(*Note 5*, *Note 9*)			0.3		V
Output Low Voltage	V_{OL}	I_{OL} = 4mA (*Note 10*)				0.4	V
Propagation Delay	$t_{OVL-VDD}$	Pass-through mode only				600	ns
	$t_{OVDD-VL}$					600	
Maximum Data Rate	t_{DR}	Pass-through mode only, R_{PUP} = 680Ω				512	kbps
IOA SENSE							
IOA Weak Pullup/ Pulldown	$R_{WRES-DN}$				5		MΩ
	$R_{WRES-UP}$				0.5		
Input Low	SENSE_V_{IL}					0.2	V
Input High	SENSE_V_{IH}			0.8		V_{PUPA} + 0.3	V
IOA, IOB PINS: 1-Wire INTERFACE							
Recovery Time	t_{REC}	(*Note 11*)	R_{PUPA} = 1000Ω, V_L not powered	5			µs
		(*Note 11*)	R_{PUPB} = 1000Ω, V_L powered	1			
		(*Note 11*)	Directly prior to reset pulse; R_{PUPA} = 1000Ω; V_L not powered	50			
Rising-Edge Hold-Off	t_{REH}	Overdrive speed (*Note 12*)			100		ns
Time Slot Duration	t_{SLOT}	Overdrive speed (*Note 13*)		11			µs
IOA, IOB PINS: 1-Wire RESET, PRESENCE-DETECT CYCLE							
Reset Low Time	t_{RSTL}	System requirement, overdrive speed	V_L powered	48		80	µs
			V_L not powered	48		50	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset High Time	t_{RSTH}	Overdrive speed (*Note 17*)		48			µs
Presence-Detect Sample Time	t_{MSP}	Overdrive speed (*Note 14*)		6		10	µs
Presence Detect Fall Time	t_{FPD}	GBD	Overdrive speed (*Note 18*)		0.15		µs
IO PIN: 1-Wire WRITE							
Write-Zero Low Time	t_{W0L}	Overdrive speed (*Note 15*)		6		15.5	µs
Write-One Low Time	t_{W1L}	Overdrive speed (*Note 15*)		0.25		2	µs
IOA, IOB PINS: 1-Wire READ							
Read Low Time	t_{RL}	Overdrive speed (*Note 16*)		0.25		2 - δ	µs
Read Sample Time	t_{MSR}	Overdrive speed (*Note 16*)		t_{RL} + δ		2	µs
PIOA, PIOB PINS							
GPIO Output Low	$PIOV_{OL}$	$PIOI_{OL}$ = 4mA (*Note 10*)				0.4	V
GPIO Input Low	$PIOV_{IL}$			-0.3		0.2 x V_L	V
GPIO Controller Sample	$PIOV_{IH}$			0.80 x V_L		V_L + 0.3	V
GPIO Switching Hysteresis	$PIOV_{HY}$				0.1 x V_L		V
GPIO Leakage Current	$PIOI_L$	(*Note 21*)		-1		+1	µA
PIO Delay	t_P	GBD			0.2		µs
CD/PIOC PIN							
Output Low	CD_PIOV_{OL}	CD_PIOI_{OL} = 4mA (*Note 10*)				0.4	V
Input Low	CD_PIOV_{IL}			-0.3		0.20 x V_{PUPA}	V
Input High	CD_PIOV_{IH}			0.8 x V_{PUPA}		V_{PUPA} + 0.3	V
CD_PIO Switching Hysteresis	CD_PIOV_{HY}				0.1 x V_{PUPA}		V
Leakage Current	CD_PIOI_L			-1		+1	µA
CD_PIO Delay	t_P	GBD			0.2		µs
TOKEN PIN							
Output Low	$TOKENV_{OL}$	$TOKENI_{OL}$ = 4mA (*Note 10*)				0.4	V
Leakage Current	$TOKENI_L$			-1		+1	µA
Token Frequency	TOK_F	Pass-through mode only			30k		Hz
TIMER							
Timer Period	t_{TP}			89.1	99	108.9	µs
IOA PIN: STRONG PULLUP APPLIED DURING POWER-UP							
Strong Pullup Current	I_{SPU}	(*Note 19*)				500	µA
Strong Pullup Voltage	V_{SPU}	(*Note 19*)		1.71			V
Warmup Time	t_{OSCWUP}	(*Note 1*, *Note 20*)				5	ms

Note 1: Initial power-up from IOA requires strong pullup for t_{OSCWUP} duration.

Note 2: System requirement. Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.

Note 3: Value represents the typical supply capacitance when IOA or V_L is first applied. Once the supply capacitance is charged, it does not affect normal communication. Typically, during normal communication, the parasite capacitance is effectively ~100pF.

Note 4: Internal supply (V_{REG}) will move to IOA parasite power (V_{DD}) if IOA is greater than V_L.

Note 5: IOA V_{TL}, V_{TH}, and V_{HY} are a function of the internal parasite supply voltage (V_{DD}), which is a function of V_{PUPA}, R_{PUPA}, 1-Wire timing, and capacitive loading on IOA. Lower V_{PUPA}, higher R_{PUPA}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY} for the IOA link. V_{TL}, V_{TH}, and V_{HY} are a function of the V_L for the IOB link.

Note 6: Voltage below which, during a falling edge on IO, a logic-zero is detected.

Note 7: The average voltage on IO must be less than or equal to V_{ILMAX} at all times the controller is driving IO to a logic-zero level.

Note 8: Voltage above which, during a rising edge on IO, a logic-one is detected.

Note 9: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic-zero.

Note 10: The I-V characteristic is linear for voltages less than 1V.

Note 11: System requirement. Applies to a single device attached to a 1-Wire line.

Note 12: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.

Note 13: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.

Note 14: System requirement. Interval after t_{RSTL} during which a bus controller can read a logic 0 on IO if there is a DS2488 present. Communication should not begin to after the 2ms power-up for IOA has completed when no V_L is present.

Note 15: System requirement. ε in Figure 7 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the controller to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.

Note 16: System requirement. δ in Figure 7 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus controller. The actual maximum duration for the controller to pull the line low is $t_{RLMAX} + t_F$.

Note 17: An additional reset or communication sequence cannot begin until the reset high time has expired.

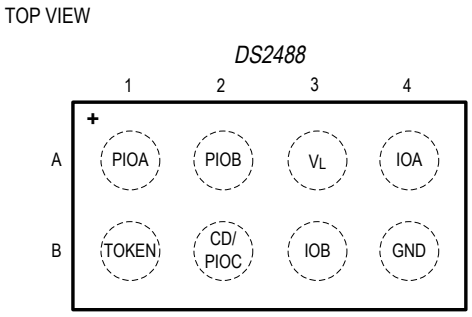
Note 18: Time from $V_{(IO)}$ = 80% of V_{PUP} and $V_{(IO)}$ = 20% of V_{PUP} at the negative edge on IOA or IOB at the beginning of the presence detect pulse.

Note 19: I_{SPU} is the current drawn from IOA during a strong pullup (SPU) operation before 3ms has elapsed during a power-up when V_L has no supply. The pullup circuit on IO during the SPU operation should be such that the voltage at IOA is greater than or equal to V_{SPUMIN}. A low-impedance bypass of R_{PUPA} activated during the SPU operation is the recommended way to meet this requirement.

Note 20: 1-Wire communication should not take place for the max t_{OSCWUP} time following a power-on reset. If powering up on IOA only, SPU is required for this duration. If powering up on IOA only, charge sensing typically occurs at 1.5ms.

Note 21: PIOB must be less or equal to V_L. If PIOB > V_L, I_{VL} will be incurred on PIOB.

Pin Configuration



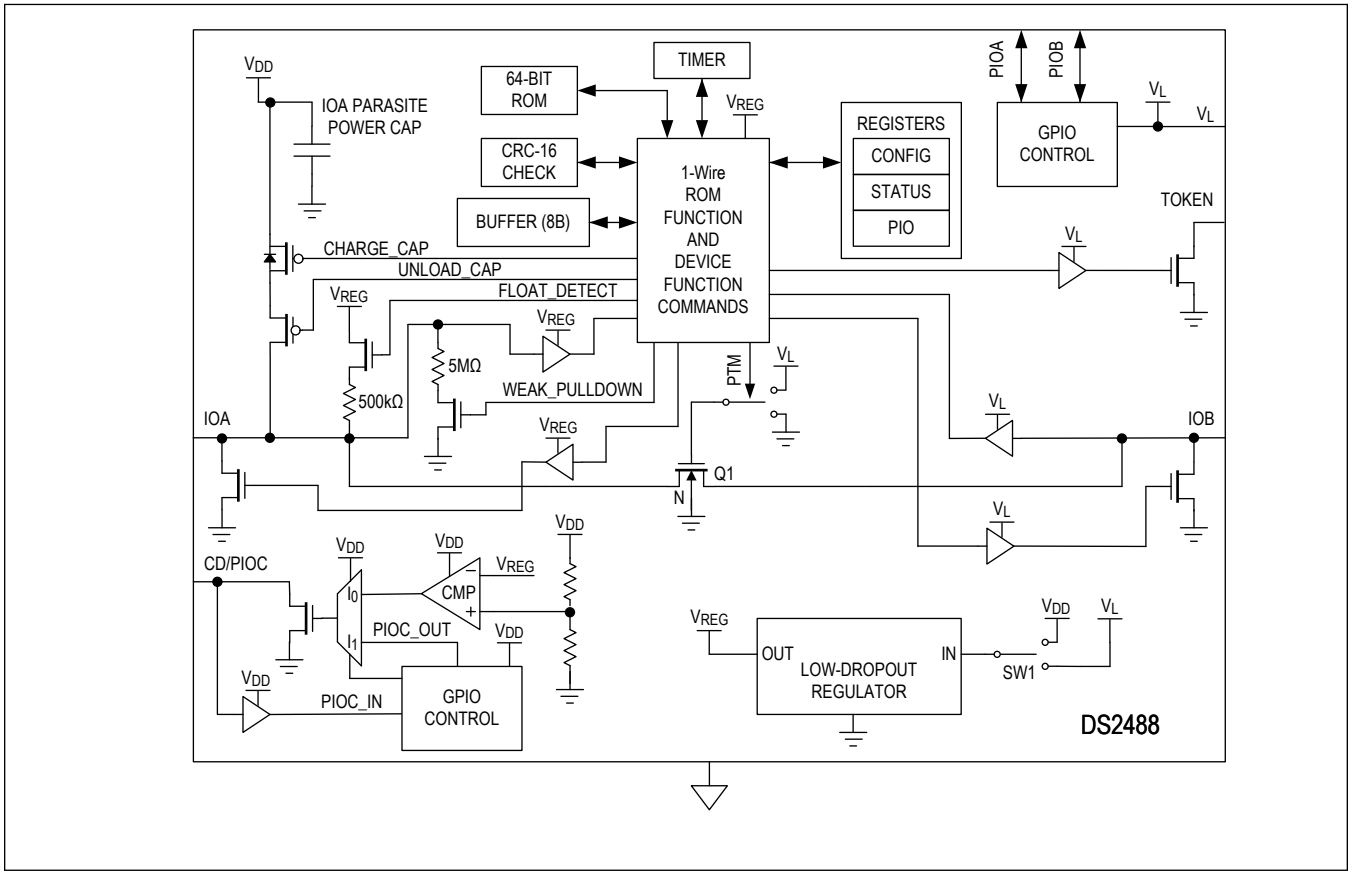
WLP

Pin Description

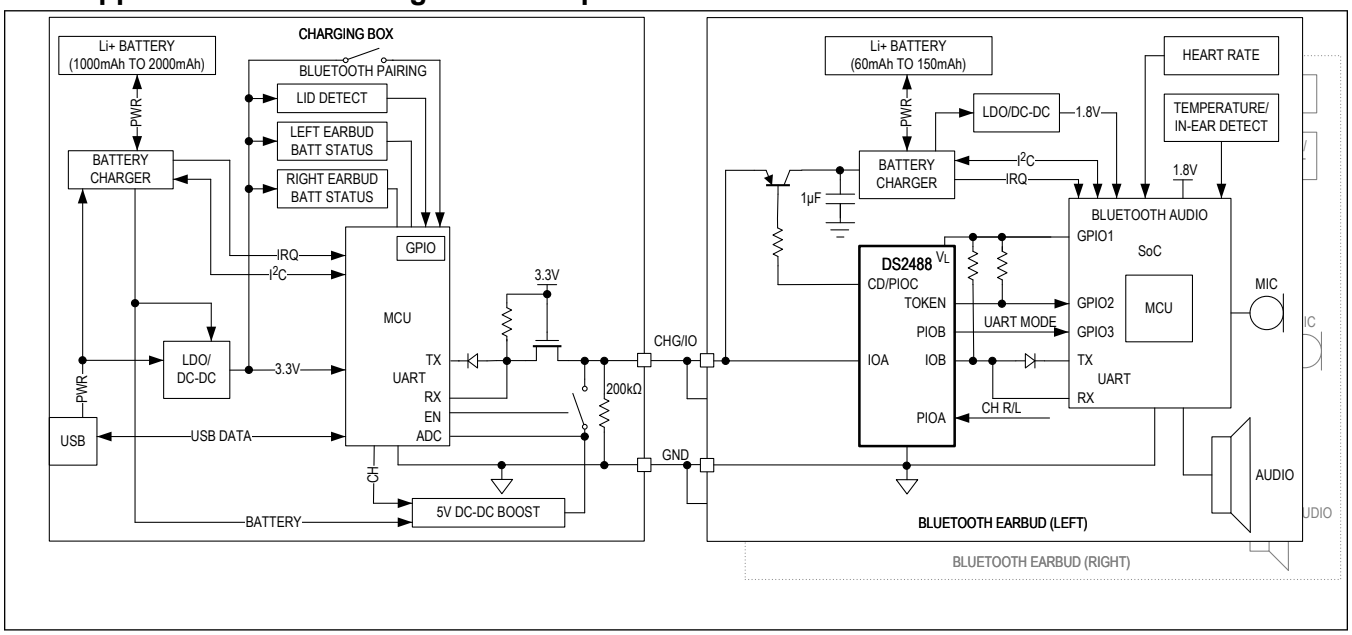
PIN	NAME	FUNCTION	REF SUPPLY	TYPE
A1	PIOA	General-Purpose Input/Output A.	V_L	Input/Output Open-Drain
A2	PIOB	General-Purpose Input/Output B.	V_L	Input/Output Open-Drain
A3	V_L	Voltage Low. This is the low-power supply input. Needed for IOB, PIOA, PIOB, and TOKEN pin operation.	—	Power
A4	IOA	1-Wire Input/Output A. Accessible when the TOKEN pin is logic low. This pin can also be configured in a logic pass-through mode to IOB pin. IOA parasite power required for CD/PIOC pin operation.	V_{PUPA} or V_L (PTM)	Input/Output Open-Drain
B1	TOKEN	Token. This pin indicates which 1-Wire side gets the communication token. Logic low stands for IOA side, while logic high for IOB side. It outputs a low-frequency clock (TOK_F) while in pass-through mode.	V_L	Output Open-Drain
B2	CD/PIOC	Charger Disable (Default) or General-Purpose Input/Output (SEL bit is set to one). Charger disable is floating (i.e., non-conducting) when the IOA pin is nominally below 4V. Otherwise, charger disable is actively low to enable the charger through a transistor when IOA is above 4V.	V_{PUPA}	Input/Output Open-Drain
B3	IOB	1-Wire Input/Output B. This pin can also be configured in a logic pass-through mode to IOA pin.	V_L	Input/Output Open-Drain
B4	GND	Ground.	—	Ground

Functional Diagrams

Detailed Block Diagram



TWS Application Circuit Using UART Peripherals for 1-Wire Communication



Detailed Description

The DS2488 fundamentally operates from two independent 1-Wire peripheral interfaces, IOA and IOB, which operate with a token defined arbitration scheme as detailed in the state machine diagram of Figure 1 and truth table of Table 1. Depending on which side of the link has the token assigned, IOA or IOB, that side has control for 1-Wire communication with the device; see *Pin Description* for token state assignment definition. With control, writes and reads to the DS2488 communication buffer and registers are performed to exchange small messages between IOA and IOB, set configuration parameters, read/write to the three GPIO pins, and set the timeout value of a timer used in conjunction with a high-speed 512kbps pass-through mode between IOA and IOB. Once set into pass-through mode, the timer is reset with each falling edge at IOA or IOB to maintain the mode. This enables simplex (one direction only) or half duplex (devices take turns transmitting and receiving) UART-to-UART communication to pass large amounts of data. See the *Simplified Application Block Diagram* and *TWS Application Circuit* example for the hardware configuration of the UART interface of each subsystem controller to operate under software control, either as a 1-Wire controller or UART transceiver.

Like typical 1-Wire products, the DS2488 has operational modes whereby device power is parasitically captured from the 1-Wire interface. However, this applies only to communication and operation through the IOA interface, not IOB. When communicating 1-Wire commands to the IOB interface, or when operating in the high-speed pass-through mode, an additional supply in (V_L) is required (see the *Power-Supply Description* section. Also, as a 1-Wire product, the DS2488 provides a unique 64-bit registration number (ROM ID) that is factory-programmed into the device. The ROM ID serves an important role in applications such as TWS where two DS2488 devices, one in each earbud, would be multidrop connected to the same 1-Wire connection originating from the charging case controller. For this scenario, the ROM ID is used by the case controller to select the specific DS2488 in the left or right earbud for communication and operation. Additionally, the unique serialization field that is a data component of the 64-bit ROM ID can be used for end-product identification and traceability.

For applications that require power to be sourced from the IOA subsystem side to the IOB side, the device provides a configurable mode that enables a 4V to 5V supply to be switched through an external transistor that is controlled from a DS2488 signal (CD/PIOC). For normal 1-Wire and pass-through mode communication, the DS2488 operating voltage range is 1.71V to 3.63V. However, to support this power delivery mode, the device is 5V tolerant and goes into the power delivery state when 4V to 5V (nom) is detected at IOA. An integrated comparator is used for this detection and control of the CD/PIOC pin.

State Machine Operation

A state machine controls the internal operations per Figure 1. The device starts in the POR state on power-up through V_L or IOA parasite power. Communication is ignored during the POR t_{OSCWUP} time as the device initializes. The warmup delay only occurs on power-up. State transitions are made on the internal 30kHz oscillator. State transitions take multiple clocks, especially high-voltage detection, and enable pass-through mode. The timer function runs on a 10kHz divide of the oscillator. After the POR warm-up, if SEL = 0 (default), the device checks for high voltage on the IOA link. If high voltage is detected, the charge function is activated, and IOB link is handed the token for communication. The IOB link generates a presence detect when IOA passes the token to IOB. If high voltage is not detected, IOB does not have the token and the state machine checks the config bits QM/PTM/PULLUP and branches accordingly. If the config mode bits are not set and IOA is high, IOA is handed the token for communication. The IOA channel does not issue a presence detect when it has the token to avoid contention with the charging function. IOA communication stays active until IOA times out low, either from the IOA controller pulling low or the weak pulldown on a floating IOA. The IOA weak pulldown is normally active, except during charge sensing, pass-through mode, and the IOA PULLUP mode. If IOA is not connected or times out low, IOB is given the token for communication until IOA goes high. When IOA goes high, the device loops back to the SEL = 0, the IOA high-voltage charge-sense function.

The timer is used to monitor the IOA pin for transitioning into IOB '1-Wire Operation' state. A falling edge on IOA resets the timer. If the timer expires and confirms that a logic low is still present, then the IOB link is passed the token (i.e., no other falling-edge transition occurred). While IOB link has the token, the IOA controller continues to pull low. However, if the IOA controller drives high before the timer expires, then the logic state will exit to the appropriate state (e.g., IOA link state "Idle logic high") when the timer expires. See Table 1 for more details on the states.

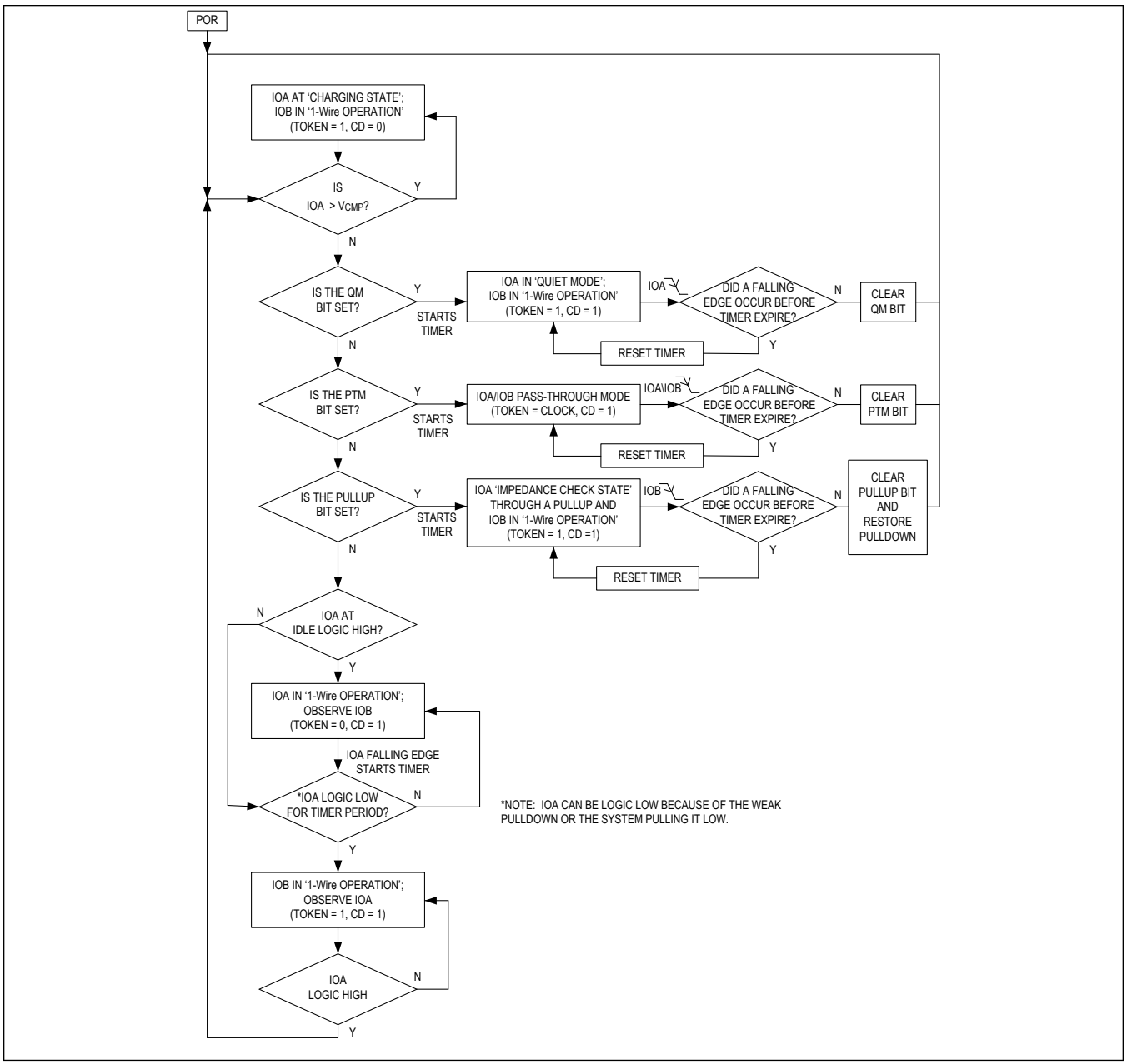


Figure 1. State Diagram

IOA/IOB Arbitration Truth Table

Table 1. IOA/IOB Arbitration Truth Table

EARBUD POSITION	IOA PIN STATE	IOB PIN STATE	ACCESS TOKEN SIDE	TOKEN PIN	WEAK PULLUP	POWER STATE	IOAS BIT STATUS	CMPS BIT STATUS	PTM	TIMER
In box	+5V voltage	Idle logic high	IOB	'1'	Off	V_{PUPA} or V_L	'1'	'1'	May be enabled, but waits	N/A
In box	Logic low	Idle logic high	IOB	'1'	Off	V_L	'0'	'0'	May be enabled, but waits	Only in 1-Wire, verifies IOA logic low
In dead box	Low impedance	Idle logic high	IOB	'1'	On	V_L	'0'	'0'	Disabled	Repeats verifying IOB transitions
Not in box	High impedance	Idle logic high	IOB	'1'	On	V_L	'1'	'0'	Disabled	Repeats verifying IOB transitions
In box	Idle logic high	Don't care	IOA	'0'	Off	V_{PUPA} or V_L	'1'	'0'	Disabled	Repeats verifying IOA high
In box	Idle logic high	Don't care	IOA/IOB	Clock output	Off	V_L	'1'	'0'	Enabled (Active)	PTM, repeats verifying IOA/ IOB transitions
In box	Idle logic high	Don't care	IOB	'1'	Off	V_{PUPA} or V_L	'1'	'0'	Disabled	QM, repeats verifying IOA transitions

Power-Supply Description

In pass-through mode, the device requires V_L power. Outside of pass-through mode, the core derives power from the higher of IOA parasite power or V_L. The IOA and PIOC/CD pads are always powered by IOA parasite power. The IOB, TOKEN, PIOB, and PIOA pads are always powered by V_L.

Pass-Through Operation

When in pass-through mode (timer enabled), the DS2488 turns on an nMOS pass-through device to allow bidirectional UART communication between IOA and IOB. IOA high-side to IOB low-side level translation is achieved by limiting the gate of the nMOS to the low-side V_L supply. The IOA pullup voltage, V_{PUPA} must be greater than or equal to V_L in pass-through mode. The DS2488 requires external pullup resistors from IOA V_{PUPA} and IOB V_L to pull the lines high when a low is not being driven. Internal circuitry assists logic-state transitions for the IOA link by removing the internal parasitic capacitance in PTM and turning off the IOA weak pulldown.

64-Bit ROM ID

Each DS2488 contains a unique ROM ID that is 64 bits long. The ROM ID provides absolute traceability for each device. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 2 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 8-bit, 1-Wire CRC is available in *Application Note 27*.

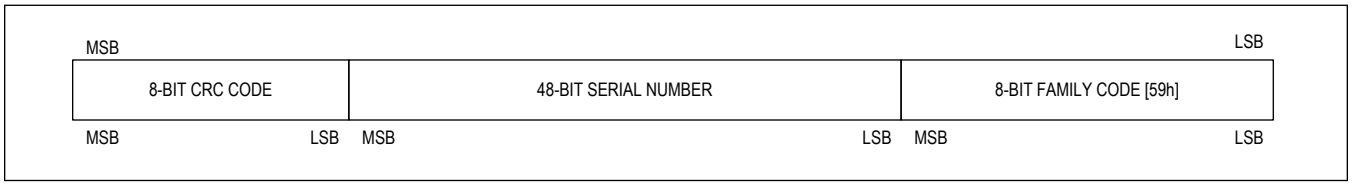


Figure 2. ROM ID

Device Function Commands

After a 1-Wire Reset/Presence cycle and ROM function command sequence are successful, a device function command can be accepted. The commands generally follow the Figure 3 flow.

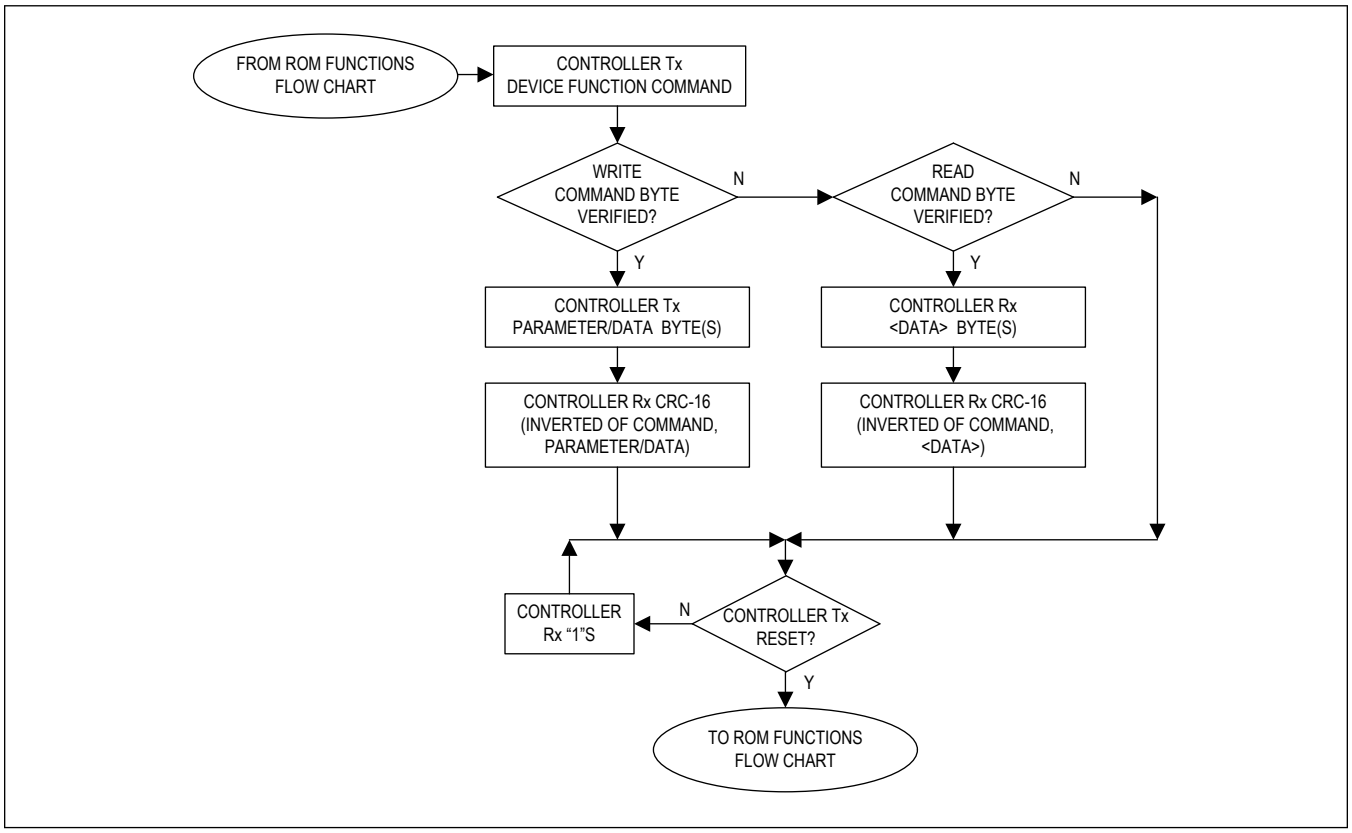


Figure 3. Device Function Command Flow

There are nine device function commands that are summarized in Table 2 and are described in detail in subsequent sections. Within the Figure 3 flow diagram, the data transfer is verified when writing and reading by a CRC of 16-bit type (CRC-16). The CRC-16 is computed as described in *Application Note 27*.

Table 2. Device Function Command Summary

COMMAND	CODE	DESCRIPTION	TYPE
Write Configuration	11h	General Configuration	Global
Read Configuration	22h	General Configuration	Global
Write Buffer	33h	Write Buffer	Memory
Read Buffer	44h	Read Buffer	Memory
Read Status	55h	Read Status	General
PIO Write	66h	PIO Write conducting or float	Access
PIO Read	77h	PIO Read logic state	Access
Write Timeout Value	88h	Write to the Timeout Value register	General
Read Timeout Value	99h	Read the Timeout Value register	General

Write Configuration (11h)

The Write Configuration command is used to set the configuration register.

Table 3. Write Configuration Command

WRITE CONFIGURATION	
Command Code	11h
Parameter Byte(s)	Write Configuration
Usage	The write configuration sets the global configuration for the device. The SEL bit is used to select between CD or PIOC. Default is comparator functionality for detecting when a charging supply is detected on the IOA pin or when IOA is a 1-Wire link. The CD pin is an output for external power switching control to a transistor. Additionally, a pass-through mode (PTM bit) with level shifting is available for when simplex or half-duplex UART communication is between the IOA and IOB pins. Pass-through mode allows communication up to 512kbps and remains active as long as IOA/IOB activity is detected within a timer period. Some applications need interrupt support for when the buffer has been written. The BUFAPE/BUFBPE config bits enable the buffer write status flags, BUFA/BUFB, to turn on the PIOA/PIOB pulldowns when the buffer is written.
Command Restrictions	Pass-through mode requires a V_L supply to be present.
Device Operation	Setting the configuration register.

Table 4. Write Configuration Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	PULLUP	QM	PTM	BUFBPE	BUFAPE	SEL

Bit 0: Select (SEL). When set to 1, PIOC pin function is operational. When set to 0 (default), CD pin function is operational.

Bit 1: BUFA Port Enable (BUFAPE). When set to 1, the PIOA pin outputs the invert state of the BUFA flag in the status register. When set to 0 (Default), the PIOA pin is normal access.

Bit 2: BUFB Port Enable (BUFBPE). When set to 1, the PIOB pin outputs the invert state of the BUFB flag in the status register. When set to 0 (Default), the PIOB pin will be normal access.

Bit 3: Pass-Through Mode (PTM). When set to 1, PTM is enabled and the timer begins to monitor IOA/IOB pins for activity (i.e., falling-edge transitions) and outputs a clock on the TOKEN pin. The timer resets on any falling-edge activity to maintain PTM. If no activity occurs, then the device automatically returns to normal 1-Wire operation states and the PTM bit is cleared to 0 when the timer expires. When set to 0 (Default), pass-through mode is disabled.

Bit 4: Quiet Mode (QM). When set to 1, QM is enabled and the timer begins to monitor the IOA pin for activity (i.e., falling-edge transitions) and outputs logic high on the TOKEN pin. The timer is reset on any IOA pin falling-edge activity to the timeout value so as to maintain QM. If no other falling-edge IOA activity occurs, then the device automatically returns to normal 1-Wire operation states, and the QM bit is cleared to 0 when the timer expires. This bit defaults to 0.

Bit 5: Pullup (PULLUP). When set to 1, a weak pullup resistor from the IOA link to V_{REG} is enabled. When set to 0 (Default), the pullup resistor is disconnected from V_{REG} and the weak pulldown to ground is connected. In this way, the IOA pin is not floating when not connected to any equipment. The write config CRC-16 may read invalid or FF when setting PULLUP = 1, and should be ignored. This is due to the resulting TWS state transition.

Table 5. Write Configuration Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 11h (Write Configuration)
Tx: Parameter (Write Configuration)

Table 5. Write Configuration Sequence (continued)

Rx: CRC-16 (inverted of Command, Parameter)
Reset

Read Configuration (22h)

The Read Configuration command is used to read the configuration register.

Table 6. Read Configuration Command

READ CONFIGURATION	
Command Code	22h
Parameter Byte(s)	None
Usage	Read configuration register to confirm settings.
Command Restrictions	None.
Device Operation	Read configuration register.

Table 7. Read Configuration Data Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	PULLUP	QM	PTM	BUFBPE	BUFAPE	SEL

Bit 0: Select (SEL). Read bit state.

Bit 1: BUFA Port Enable (BUFAPE). Read bit state.

Bit 2: BUFB Port Enable (BUFBPE). Read bit state.

Bit 3: Pass-Through Mode (PTM). Read bit state.

Bit 4: Quiet Mode (QM). Read bit state.

Bit 5: Pullup (PULLUP). Read if pullup resistor is connected (1) or disconnected (0).

Table 8. Read Configuration Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 22h (Read Buffer)
Rx: Read Configuration
Rx: CRC-16 (inverted, Command, and data)
Reset

Write Buffer (33h)

The Write Buffer command is used to write a temporary value to the volatile buffer. The buffer is used to transfer bytes to/from the 1-Wire IOA or IOB link.

Table 9. Write Buffer Command

WRITE BUFFER	
Command Code	33h
Parameter Byte(s)	Byte Length (BLEN)
Usage	Write to temporary buffer from either 1-Wire IOA or IOB link. The buffer is 8 bytes long. Any number from 0 to 8 bytes can be written. The buffer length is referred to as BLEN.
Command Restrictions	If BLEN > 8d, then nothing will be written and the CRC-16 will be skipped. Invalid values of BLEN do not disturb the buffer. IOA or IOB link can only write to the buffer if they have the token.
Device Operation	Loads buffer. When IOA link writes the buffer, BUFA flag is set and BUFB flag is cleared. When IOB link writes the buffer, BUFB flag is set and BUFA flag is cleared. If BLEN = 0, then nothing will be written and both the BUFA/BUFB flags are cleared and the device outputs the CRC-16 of the command and parameter byte.

Table 10. Write Buffer Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	BLEN			

Bits 3:0: Byte Length (BLEN). Data length to write, 0 to maximum length number of 8.

Table 11. Write Buffer Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 33h (Write Buffer)
Tx: Parameter (BLEN)
Tx: Data (0 to 8 bytes are written)
Rx: CRC-16 (inverted of Command, Parameter, Data)
Reset

Read Buffer (44h)

The Read Buffer command is used to read the buffer from the 1-Wire IOB link or from the 1-Wire IOA link.

Table 12. Read Buffer Command

READ BUFFER	
Command Code	44h
Parameter Byte(s)	None
Usage	Read buffer from 1-Wire IOA link or 1-Wire IOB link.
Command Restrictions	If BLEN = 0, the command returns the byte length 0 and the CRC-16 of the command and byte length.
Device Operation	Read buffer.

Table 13. Read Buffer Length Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	BLEN			

Bits 3:0: Byte Length (BLEN). These bits represent the number of bytes to be read.

Table 14. Read Buffer Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 44h (Read Buffer)
Rx: Byte Length (BLEN)
Rx: Data (0 to 8d bytes)
Rx: CRC-16 (inverted, Command, Byte Length, and Data)
Reset

Read Status (55h)

The Read Status command indicates which interface wrote the buffer last, and also the logical state of the IOA/IOB input buffers, high-voltage comparator state, token state, timer reset, and power source.

Table 15. Read Status Command

READ STATUS	
Command Code	55h
Parameter Byte(s)	None
Usage	Used for receive status info. Provides a means to know if IOA link should read out buffer or if IOB link should read out buffer. Also used to check the logical state of the IOA/IOB links and if the comparator has detected charging voltage on IOA link.
Command Restrictions	None
Device Operation	Output status. $\overline{TRST}$ flag is set after the status register is read.

Table 16. Status Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PSW	$\overline{TRST}$	TOKS	CMPS	IOBS	IOAS	BUFB	BUFA

Bit 0: Buffer A Flag (BUFA). Indicates the buffer was written from the IOA link.

Bit 1: Buffer B Flag (BUFB). Indicates the buffer was written from the IOB link.

Bit 2: IOA State (IOAS). Logic state of the IOA pin.

Bit 3: IOB State (IOBS). Logic state of an AND gate with the IOB and V_L pins as the inputs.

Bit 4: Comparator State (CMPS). Output state of the comparator. This can be used to detect charging voltage when 1 and no charging voltage when 0 on the IOA pin.

Bit 5: Token State (TOKS). Logic state of the TOKEN pin. Toggles when in PTM.

Bit 6: Timer Reset ($\overline{TRST}$). In logic-low state, this indicates the timer has begun again with the timeout value. This flag is synchronously set after a status read so a read status must be performed to first set the bit, followed by a second read status to see if the bit remains set (the timer is running), or clears (the timer is not running yet, or started since previous read status).

Bit 7: Power Source (PSW). Indicates when set that the V_L pin is being used as the power source. When 0, the power source is parasitically derived by the IOA link.

Table 17. Read Status Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 55h (Read Status)
Rx: Status Byte
Rx: CRC-16 (inverted, Command, Status Byte)
Reset

PIO Write (66h)

The PIO Write command controls the open-drain PIO drive state if a special function is not active on the pin. See write config bits SEL, BUFBPE, and BUFAPE for a description of the special functions. To switch the output transistor on, the corresponding bit value is 0. To switch the output transistor off (nonconducting), the bit must be 1. This way, the bit transmitted as the new PIO output state arrives in its true form at the PIO pin. The actual PIO transition to the new state occurs with a delay of $t_{REH}+t_P$ from the rising edge of the MS bit of the inverted PIO byte, as shown in Figure 4.

Table 18. PIO Write Command

PIO WRITE	
Command Code	66h
Parameter Byte(s)	PIO Output byte
Usage	Set the output value for the PIO pins.
Command Restrictions	To protect the transmission against data errors, the controller must set the upper nibble to the one's complement of the lower nibble in the PIO Output byte. Only if the transmission was error-free will the PIO status change.
Device Operation	Sets PIO Output state. PIOAS has no effect as long as configuration bit BUFAPE = 1. PIOBS has no effect as long as configuration bit BUFBPE = 1. PIOCS has no effect as long as configuration bit SEL = 0.

Table 19. Parameter: PIO Output Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	$\overline{\text{PIOCS}}$	$\overline{\text{PIOBS}}$	$\overline{\text{PIOAS}}$	0	PIOCS	PIOBS	PIOAS

Bit 0: PIOA Output State (PIOAS). Set this bit to 0 for conducting (logic low) or set this bit to 1 (default) for nonconducting (high impedance or logic high with external pullup).

Bit 1: PIOB Output State (PIOBS). Set this bit to 0 for conducting (logic low) or set this bit to 1 (default) for nonconducting (high impedance or logic high with external pullup).

Bit 2: PIOC Output State (PIOCS). Set this bit to 0 for conducting (logic low) or set this bit to 1 (default) for nonconducting (high impedance or logic high with external pullup).

Table 20. PIO Write Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 66h (PIO Write)
Tx: Parameter (PIO Ouput byte)
Rx: CRC-16 (inverted of Command, Parameter)
Reset

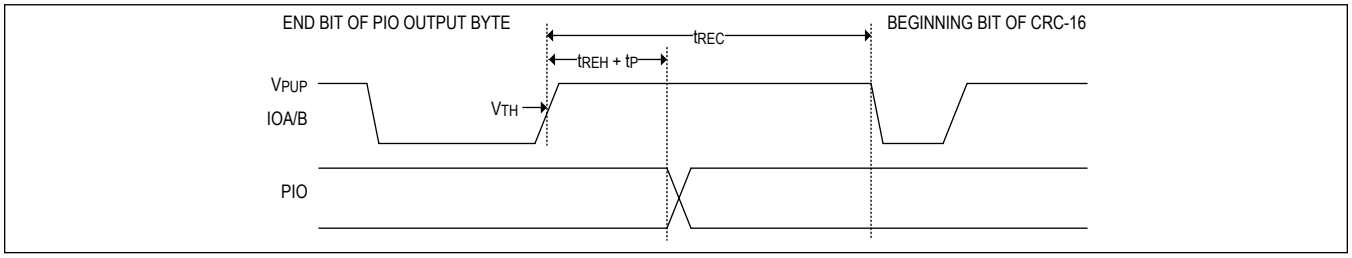


Figure 4. PIO Output Timing

PIO Read (77h)

The PIO Read command reads the input logic state of the PIO pins. V_L must be active to read the PIOA and PIOB input logic state. The IOA parasite supply must be active to read the PIOCS input logic state. PIO input buffers read high if the associated supply is not active. The PIO input buffers are normally off to prevent crowbar current, and are turned on briefly to read the input logic state.

Table 21. PIO Read Command

PIO READ	
Command Code	77h
Parameter Byte(s)	None
Usage	Read input logic state of the PIO pins.
Command Restrictions	To protect the transmission against data errors, the controller should expect the upper nibble be one's complement of the lower nibble in the PIO Input byte.
Device Operation	Reads PIO logic level. If the CD pin is set in the configuration register, then PIOCL bit will represent this logic level.

Table 22. PIO Input Byte

BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
1	$\overline{\text{PIOCL}}$	$\overline{\text{PIOBL}}$	$\overline{\text{PIOAL}}$	0	PIOCL	PIOBL	PIOAL

Bit 0: PIOA Level (PIOAL). Provides the logic state of the PIOA pin.

Bit 1: PIOB Level (PIOBL). Provides the logic state of the PIOB pin.

Bit 2: PIOC Level (PIOCL). Provides the logic state of the PIOC or CD pin.

Table 23. PIO Read Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 77h (PIO Read)
Rx: PIO Input byte
Rx: CRC-16 (inverted of Command, PIO Input byte)
Reset

Write Timeout Value (88h)

The Write Timeout Value command is used to set the timer duration.

Table 24. Write Timeout Value Command

WRITE TIMEOUT VALUE	
Command Code	88h
Parameter Byte(s)	Timeout Value
Usage	Used to set the timer duration for IOA/IOB arbitration states.
Command Restrictions	If the attempted value to be written is 00h for TVAL, then the command is invalid. Nothing is written and the CRC-16 will be skipped. The TVAL is not disturbed.
Device Operation	Sets the timer end count.

Table 25. Write Configuration Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TVAL							

Bits 7:0: Timeout Value (TVAL). Sets the end value for the timer. Defaults to FFh. Timer timeout value has the following meaning:

Timer Duration = TVAL x 100µs

Table 26. Write Timeout Value Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 88h (Write Timeout Value)
Tx: Parameter (TVAL)
Rx: CRC-16 (inverted of Command, Parameter)
Reset

Read Timeout Value (99h)

The Read Timeout Value command is used to read the timer duration.

Table 27. Read Timeout Value Command

READ TIMEOUT VALUE	
Command Code	99h
Parameter Byte(s)	None
Usage	Read timer duration register to confirm settings.
Command Restrictions	None.
Device Operation	Read timeout value register.

Table 28. Read Configuration Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TVAL							

Bits 7:0: Timeout Value (SVAL). Read the timeout value as specified:

Timer Duration = TVAL x 100µs

Table 29. Read Timeout Value Sequence

Reset
Presence Pulse
<ROM Select>
Tx: Command 99h (Read Timeout Value command)
Rx: Read Timeout Value
Rx: CRC-16 (inverted, Command and Timeout Value)
Reset

1-Wire Bus System

The 1-Wire bus is a system that has a single bus controller and one or more peripherals. In all instances, the DS2488 is a peripheral device. The bus controller is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus controller.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus can drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. Both 1-Wire ports (IOA and IOB) are open drain with an internal circuit equivalent as shown in Figure 5.

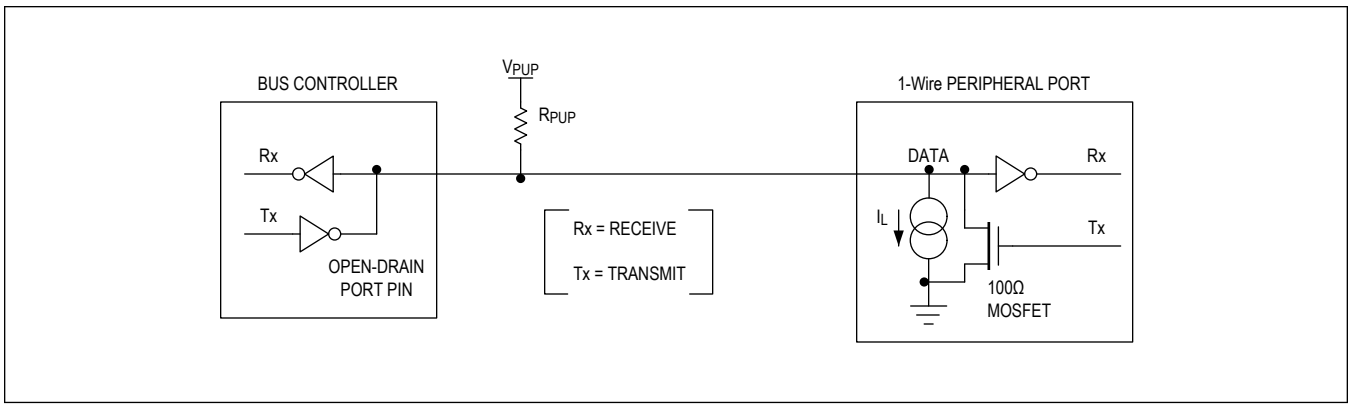


Figure 5. Hardware Configuration

A multidrop bus consists of a 1-Wire bus with multiple peripherals attached. The DS2488 supports overdrive communication speed of 90.9kbps (max). The value of the pullup resistor primarily depends on the network size and load conditions. The DS2488 requires a pullup resistor.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 15.5µs (overdrive speed), one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS2488 through either IOA or IOB 1-Wire ports is as follows:

- Initialization
- ROM Function command
- Device Function command
- Transaction/data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus controller followed by presence pulse(s) transmitted by the peripheral(s). The presence pulse lets the bus controller know that the DS2488 is on the bus and is ready to operate. For more details, see the following *1-Wire Signaling and Timing* section.

1-Wire Signaling and Timing

The DS2488 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus controller initiates all falling edges. The DS2488 can communicate at overdrive speed when not in pass-through mode.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 7 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS2488 when determining a logic level, not triggering any events.

Figure 6 shows the initialization sequence required to begin any communication with the DS2488. A reset pulse followed by a presence pulse indicates that the DS2488 is ready to receive data, given the correct ROM and device function command. If the bus controller uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. The DS2488's t_{RSTL} is no longer than 80µs.

After the bus controller has released the line, it goes into receive mode. Now, the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in the case of a special driver chip, through the active circuitry. Now, the 1-Wire bus is pulled to V_{PUP} through the pullup resistor. When the threshold V_{TH} is crossed, the DS2488 waits and then transmits a presence

pulse by pulling the line low. To detect a presence pulse, the controller must test the logical state of the 1-Wire line at t_{MSP}.

Immediately after t_{RSTH} has expired, the DS2488 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to a minimum 48µs at overdrive speed to accommodate other 1-Wire devices.

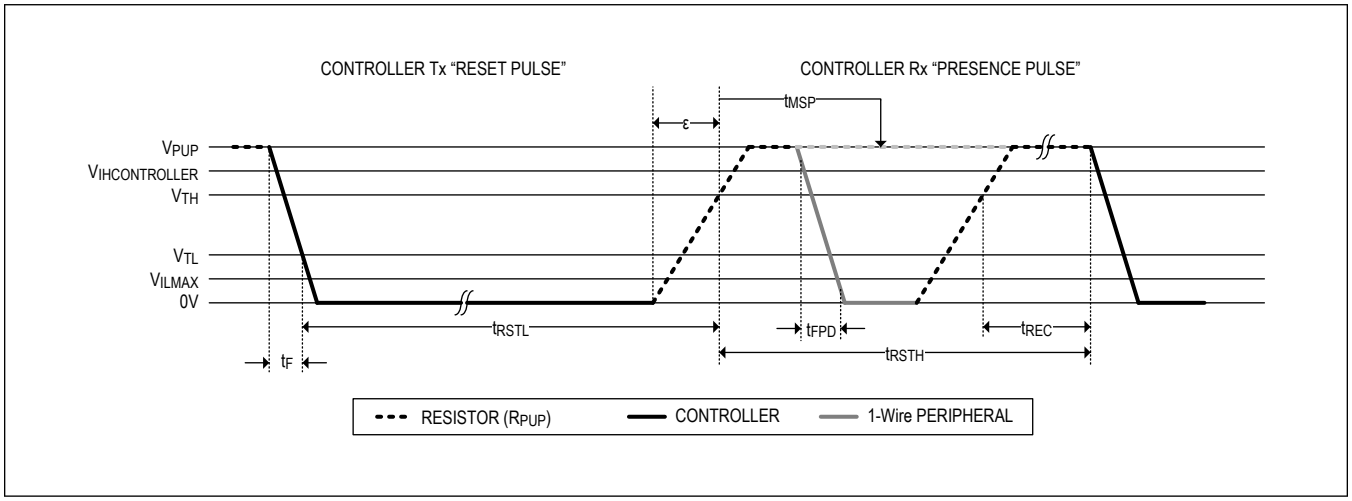


Figure 6. Initialization Procedure: Reset and Presence Pulse

Read/Write Time Slots

Data communication with the DS2488 takes place in time slots that carry a single bit each. Write time slots transport data from bus controller to peripheral. Read time slots transfer data from peripheral to controller. Figure 7 illustrates the definitions of the write and read time slots.

All communication begins with the controller pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS2488 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Controller to Peripheral

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS2488 needs a recovery time t_{REC} before it is ready for the next time slot.

Peripheral to Controller

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS2488 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS2488 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS2488 on the other side define the controller sampling window (t_{MSRMIN} to t_{MSRMAX}), in which the controller must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the controller should read close to, but no later than t_{MSRMAX}. After reading from the data line, the controller must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS2488 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS2488 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time, such as the special 1-Wire line drivers, can be used.

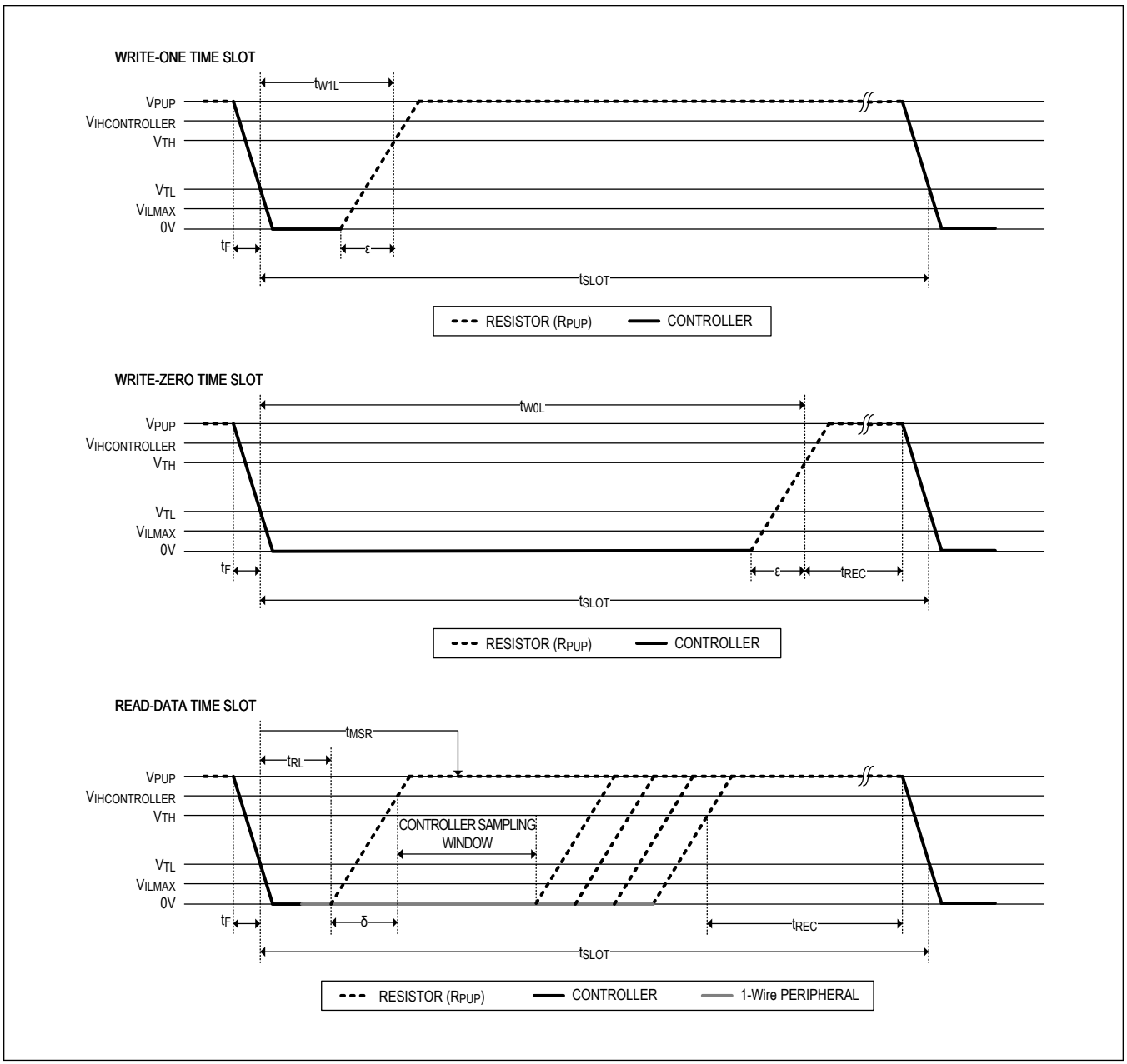


Figure 7. Read/Write Timing Diagrams

1-Wire ROM Commands

Once the bus controller has detected a presence, it can issue one of the five ROM function commands that the DS2488 supports. All ROM function commands are 8 bits long. For operational details, see Figure 8. A descriptive list of these ROM function commands follows in the subsequent sections and the commands are summarized in Table 30.

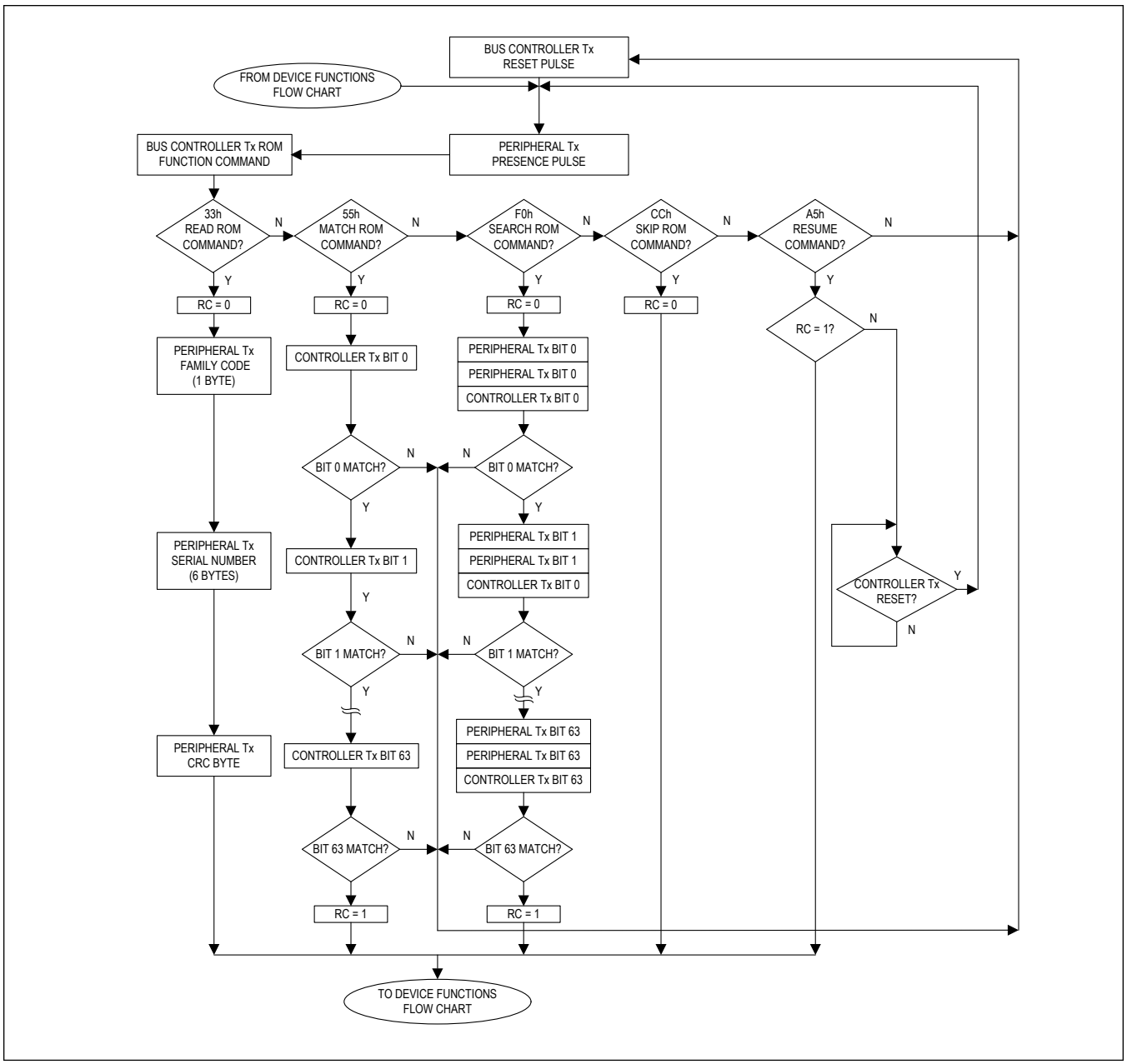


Figure 8. ROM Function Flow

Table 30. 1-Wire ROM Commands Summary

ROM FUNCTION COMMAND	CODE	DESCRIPTION
Search ROM	F0h	Search for a device
Read ROM	33h	Read ROM from device (single drop)
Match ROM	55h	Select a device by ROM number
Skip ROM	CCh	Select only device on 1-Wire
Resume	A5h	Selected device with RC bit set
Overdrive Skip ROM	3Ch	Put all devices in overdrive
Overdrive Match ROM	69h	Put the device with the ROM in overdrive

Search ROM [F0h]

When a system is initially brought up, the bus controller might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the controller can use a process of elimination to identify the ID of all peripheral devices. For each bit in the ID number, starting with the least significant bit, the bus controller issues a triplet of time slots. On the first slot, each peripheral device participating in the search outputs the true value of its ID number bit. On the second slot, each peripheral device participating in the search outputs the complemented value of its ID number bit. On the third slot, the controller writes the true value of the bit to be selected. All peripheral devices that do not match the bit written by the controller stop participating in the search. If both of the read bits are zero, the controller knows that peripheral devices exist with both states of the bit. By choosing which state to write, the bus controller branches in the search tree. After one complete pass, the bus controller knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* for a detailed discussion, including an example.

Read ROM [33h]

The Read ROM command allows the bus controller to read the DS28E38's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single peripheral on the bus. If more than one peripheral is present on the bus, a data collision occurs when all peripherals try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus controller to address a specific DS2488 on a multidrop bus. Only the DS2488 that exactly matches the 64-bit ROM sequence responds to the subsequent device function command. All other peripherals wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus controller to access the device functions without providing the 64-bit ROM ID. If more than one peripheral is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple peripherals transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the device function commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Improved Network Behavior

In a 1-Wire environment, line termination is possible only during transients controlled by the bus controller (1-Wire driver).

1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a peripheral device to lose synchronization with the controller and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS2488 uses a 1-Wire front-end that is less sensitive to noise. The IOA/IOB 1-Wire front-end has hysteresis, and a rising-edge hold-off delay.

- On the low-to-high transition, if the line rises above V_{TH} but does not go below V_{TL}, the glitch is filtered (Figure 9, Case A.)
- The rising-edge hold-off delay (nominally 100ns), t_{REH}, filters glitches that go below V_{TL} before t_{REH} has expired (Figure 9, Case B). Effectively, the device does not see the initial rise, and the t_{REH} delay resets when the line goes below V_{TL}.
- If the line goes below V_{TL} after t_{REH} has expired, the glitch is not filtered and is taken as the beginning of a new time slot (Figure 9, Case C.)

Independent of the time slot, the falling edge of the presence pulse has a controlled slew rate to reduce ringing. The falling delay is specified by t_{FPD}.

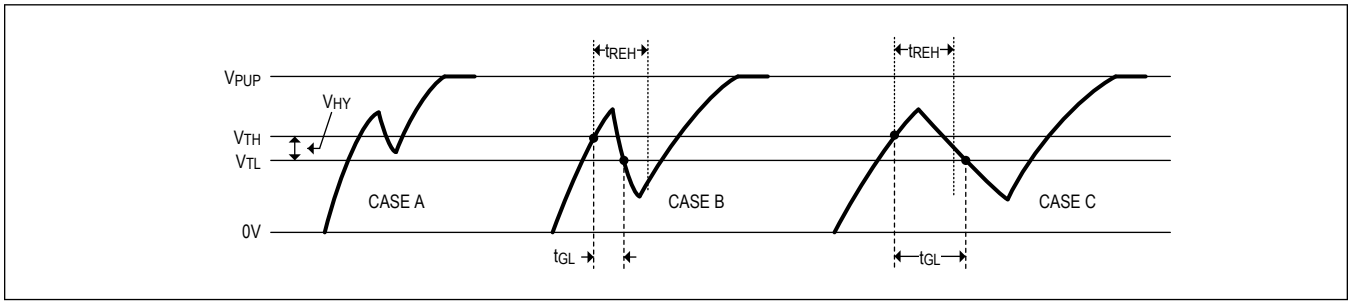


Figure 9. Noise Suppression Scheme

Oscillator Divisor

In some cases, it may be convenient to slow down the internal clock cycle time. One good example would be if an application has a load switch with a slow rise time to power the battery charger. The default high-voltage detection maximum ramp (t_{HVR}) may be too fast and sample the IOA pin early before properly reaching the V_{CMP} threshold, thus causing the device to remain out of the "charge state" with the CD pin nonconducting.

To overcome this, the DS2488 factory setting of the internal oscillator is alterable. This directly affects the timing of the charging state, timer duration, token frequency, and PTM, but not the 1-Wire timing. The default after POR is the 30kHz internal oscillator (DIV1). This oscillator can be divided into volatile memory by 2, 4, or 8. The setting can be adjusted by sending a 1-Wire sequence to IOA or the IOB link. This must be done after each POR of the device.

Table 31 shows the 1-Wire sequence options to set the oscillator division configuration:

Table 31. Oscillator Division Configuration 1-Wire Sequences

SETTING OPTION	1-Wire SEQUENCE
DIV2	RP CC DD 01 3D 75 F9 C3 [CE] [C5] [FF] [FF] RP CC AA 85 41 02 [7E] [5F]
DIV4	RP CC DD 01 3D 75 F9 C3 [CE] [C5] [FF] [FF] RP CC AA 85 42 0 1 0 0 0 0 0 <DELAY 2ms> 0 [7E] [AF]
DIV8	RP CC DD 01 3D 75 F9 C3 [CE] [C5] [FF] [FF] RP CC AA 85 43 0 1 0 0 0 0 0 <DELAY 2ms> 0 [7F] [3F]

RP = 1-Wire reset cycle with presence pulse

XX = Transmit byte (hex)

X = Single transmit bit (bin)

[XX] = Receive byte (for example the CRC returned by the DS2488)

<DELAY Xms> = Delay required by the 1-Wire sequence

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
DS2488X+T	-40°C to +85°C	8 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/20	Initial release	—
1	9/20	Release for intro; updated *Electrical Characteristics*, figures, IOA pullup/down behavior	3–6, 8, 11, 15
2	7/22	Updated *Electrical Characteristics* table	4
3	9/22	Updated *Electrical Characteristics* table and *Detailed Description*	4, 29, 30